Intel® ISP1100 Internet Server
Technical Product Specification

June 8, 2000
Revision 1.1
Order Number: A15097-002

The Intel® ISP1100 Internet Server may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel® ISP1100 Internet Server Specification Update.

Revision History

Revision	Revision History	Date
1.1	Updated TPS document to clarify product functionality	June 8, 2000
1.0	First Release of the Intel® ISP1100 Internet Server Technical Product Specification	Jan. 25, 2000

Preface

This Technical Product Specification (TPS) specifies components of the Intel® ISP1100 Internet Server. These components include the serverboard, riser card, front panel board, system BIOS, chassis, and power supply. Certifications, reliability, and serviceability of the system also are discussed.

Intended Audience

This TPS provides detailed, technical information about the Intel® ISP1100 Internet Server and its internal components. This information is provided to ISPs, vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware and losing data.

WARNING

Warnings indicate conditions that, if not observed, can cause personal injury.

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Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
Ω	Ohms
µA	0.000001 amperes
µF	Microfarad
A	Amperes (amps)
AC	Alternating Current
ACPI	Advanced Configuration Power Interface
AGP	Accelerated Graphics Port
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
BIOS	Basic Input Output System
Byte	8-bit quantity
C	Centigrade
CD	Compact Disk
CD-ROM	Compact Disk Read Only Memory
CE	Community European
cfm	Cubic feet per minute
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DCD	Data Carrier Detect
DEMKO	Danishe Elektriske Materiellkontroll (Danish Board of Testing and Approval of Electrical Equipment)
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
EDO	Extended Data Out
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	European Standard (Norme Européenne or Europäische Norm)
ESD	Electrostatic Discharge
EU	European Union
F	Fahrenheit
FC-PGA	Flip Chip Pin Grid Array
FCC	Federal Communications Commission (USA)
FD	Floppy Disk
FET	Field Effect Transistor
FP	Front Panel
FPC	Front Panel Controller
FRU	Field Replaceable Unit

Term	Definition
GB	Gigabyte (1024 MB)
Hz	Hertz (cycles per second)
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IDE	Integrated Drive Electronics
ISA	Industry Standard Architecture
KB	Kilobyte (1024 bytes)
Kg	Kilograms
kV	Kilovolts
LED	Light Emitting Diode
LVD	Low Voltage Differential
mA	Milliamps
MB	Megabyte (1024 KB)
MBE	Multi-bit Error
MIF	Management Information database
mm	Millimeters
ms	Milliseconds
MTBF	Mean Time Between Failure
MTTR	Mean Time To Repair
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NIC	Network Interface Card
NMI	Non-Maskable Interrupt
NVRAM	Non-Volatile Random Access Memory
OCP	Over-Current Protection
OEM	Original Equipment Manufacturer
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
PAC	PCI/AGP Controller
PCI	Peripheral Component Interconnect
Pf	Pico farad (10^{-12})
PFC	Power Factor Correction
PIIX4E	PCI-ISA IDE Xcelerator controller
PIO	Programmed Input/Output
PLD	Programmable Logic Device
POST	Power-On Self Test
PPGA	Plastic Pin Grid Array
PXE	Preboot Execution Environment
RAM	Random Access Memory
RPM	Revolutions Per Minute
RTC	Real-Time Clock
RxD	Receive Data
SBE	Single-bit Error
SCL	Serial Clock
SCSI	Small Computer Systems Interface

Term	Definition
SDA	Serial Data
SE	Single Ended
SEEPROM	Serial Electrically Erasable Programmable Read Only Memory
SEL	System Event Log
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SIO	Super I/O
SMB	System Management Bus
SMC	Standard Microsystems Corporation
SMBIOS	System Management BIOS
SMI	System Management Interrupt
SMM	System Management Module
TTL	Transistor-Transistor Logic
TxD	Transmit Data
UART	Universal Asynchronous Receiving/Transmitting
UL	Underwriter's Laboratories
USB	Universal Serial Bus
V	Volt
VA	Volt amperes
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference (by data processing and electronic office equipment)
Vdc	Volts direct current
Vin	Volts in
VRM	Voltage Regulator Module
Vrms	Volts root-mean-square
W	Watts
Wdc	Watts direct current
WOL	Wake on LAN
WOR	Wake on Ring
ZIF	Zero Insertion Force

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1 Introduction

This document describes the chassis and system level features of the Intel® ISP1100 Internet Server. This system is a high-density rackmount server primarily consisting of a 1U chassis and the TR440BX serverboard.

Table 1 provides a list and brief description of the Intel® ISP1100 Internet Server's key features.

Table 1: Intel® ISP1100 Internet Server key features

Feature	Description
1U chassis	1.70" (height) x 16.75" (width) x 22" (depth)
Weight	Approximately 23 lbs. at maximum configuration
Power supply	Single 125W power supply
Cooling	Five system fans
Rackmounting	Two midmount brackets or sliding rails (optional)
Hard disk bay	Support for two 1" IDE or SCSI hard drives; SCSI support requires a third-party controller and a 68-pin Wide SCSI cable (optional)
3.5" drive bay	Single standard 3.5" diskette drive included with system or slim-line CD-ROM/diskette drive combo accessory kit (optional)
Microprocessor	Single Intel® Pentium® III or Celeron™ processor in PGA370 socket
Memory capacity	Up to 1 GB of registered or unbuffered PC-100 SDRAM DIMMs
LAN support	Integrated dual Intel® Pro/100+ Server (82559) Ethernet controllers featuring PXE 2.0 option ROM for network installation and booting of operating systems
Add-in card support	Passive PCI riser (32-bit/33MHz) supports a low-profile and a full-length PCI card
System management	Heceta 2 hardware monitoring ASIC with Web-based management software
BIOS	Intel/AMI BIOS with extensions to enhance server management capabilities

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2 Chassis Description

This section describes the features of the Intel® ISP1100 Internet Server chassis.

2.1 External Chassis Features

2.1.1 Chassis Dimensions

The chassis is 1.70 inches high by 16.75 inches wide by 22.00 inches deep (measured from the front of the bezel to the deepest portion of the rear bulkhead). The chassis is designed to be mounted in a relay-style rack using the two right-angle midmount brackets provided with the base system. It can also be installed in a standard 19" rack using a sliding rails kit (optional).

Table 2: Chassis dimensions

Height	1.70" (1U)
Width	16.75" from side to side; 19" from front flange to flange
Depth	20.50" from front flange to deepest rear panel; 22" including bezel; rear-step is 1.25"
Weight	23lbs. maximum configuration

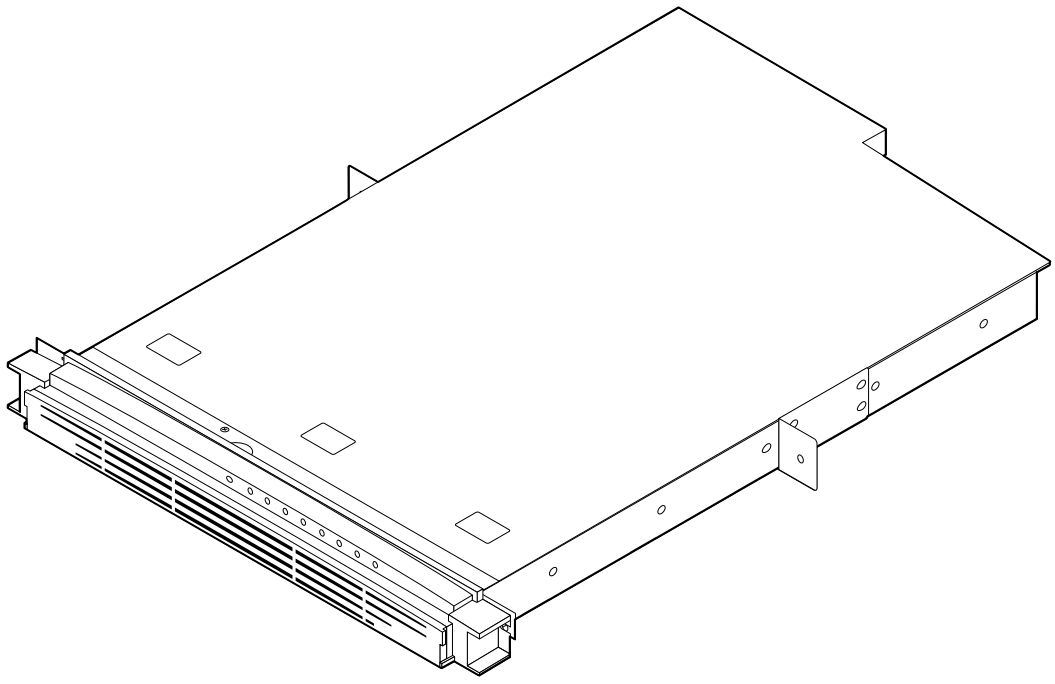


Figure 1: Isometric view of chassis

2.1.2 Colors of Chassis

The primary exterior of the chassis is unpainted. The bezel is a molded black (GE701) plastic.

2.1.3 Front View of Chassis

The front bezel is a multiple-part plastic molding that contains the buttons, the LED indicator light pipes, and a door that spans the full width of the bezel and folds down.

See Section 5 for a complete description of the buttons and LEDs.

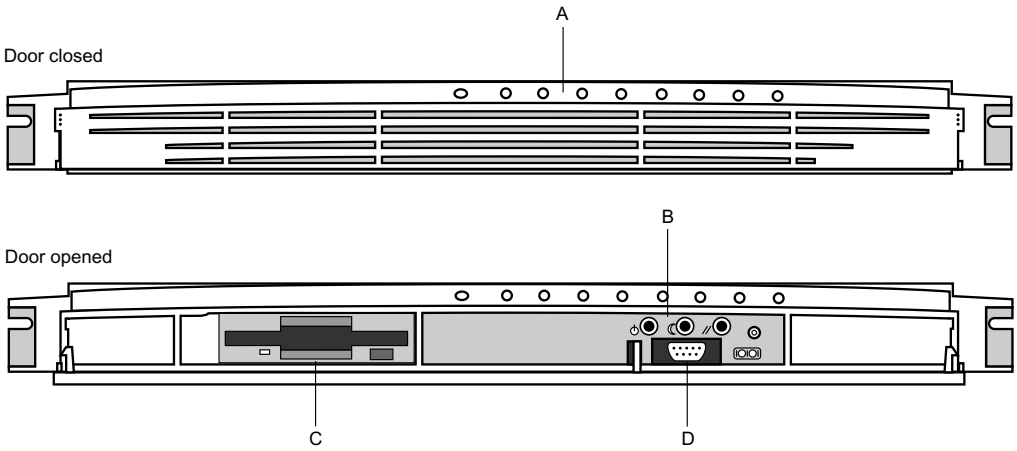


Figure 2: Front view of chassis

2.1.4 Rear View of Chassis

The input/output connectors are accessible at the back panel of the chassis as shown in Figure 3. The built-in interfaces on the TR440BX serverboard are mapped in the figure below. See Section 3.16.1 for detailed descriptions of the rear panel I/O connectors.

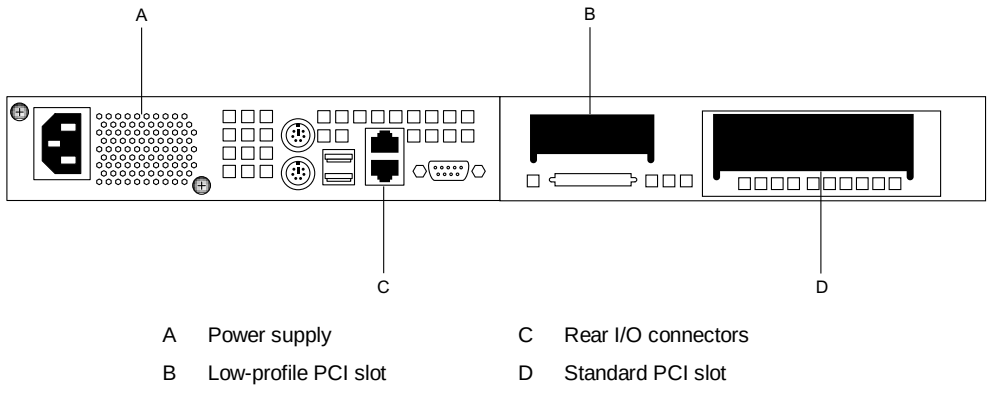


Figure 3: Rear view of chassis

2.2 Internal Chassis Features

2.2.1 Power System

The Intel® ISP1100 Internet Server chassis uses a single auto-ranging, power factor corrected power supply. The power supply uses a standard IEC 320 power cord.

The power supply design and specifications are controlled by Intel document number 753752. The power supply rating is described in Table 3.

Table 3: 125W power supply output summary

DC Power	+3.3VDC at 6.0A Max.
	+5 VDC at 13A Max.
	+12 VDC at 3.0A Max.
	-12 VDC at 0.2A
	5V Standby 1A
Total power from supply	125W
AC line voltage	90-135,180-265VAC PFC: auto sense
AC line frequency	40 / 63 Hz

2.2.1.1 Power Supply Mechanical Outline

The power supply is 3.30" by 1.60" by 9.60". The output cable bundle is separated into a cable with an ATX connector for the serverboard, and a peripheral cable for the two hard drives, a slim-line CD-ROM drive, and a standard 3.5" diskette drive.

2.2.1.2 Power Supply Fan Requirements

The power supply relies on cooling provided by two 40mm fans mounted in the chassis in front of the power supply. These fans are controlled by a two-speed circuit that is controlled by either a front panel mounted thermostat or by server management software.

2.2.1.3 AC Power Line

The system is specified to operate, automatically switching, from 100-120VAC, 200-240VAC, at 50 or 60Hz. The power supply incorporates Power Factor Correction (PFC) as a standard feature. The system is tested to meet these line voltages, and has been tested (but not specified) at +10% and -10% of the voltage ranges, and ± 3Hz on the line input frequency.

The system is specified to operate without error with line source interruptions not to exceed 20 milliseconds at nominal line conditions and full power supply output load.

The system is not damaged by AC surge ring wave to 2.5kV/500A. This ring wave is a 100kHz damped oscillatory wave with a specified rise-time for the linear portion of the initial half-cycle of 0.5µsec. Additionally, the system will not be damaged by a unidirectional surge waveform of 2.0kV /3000A, with a 1.2µsec rise time and 50µsec duration. Further details on these waveforms can be obtained in ANSI/IEEE STD C62.45-1987.

2.2.1.4 DC Connector Requirements

Figure 4 shows the connector's pinouts, which uses a Molex 39-29-9202 part. This mates with the power supply connector, Molex 39-01-2200.

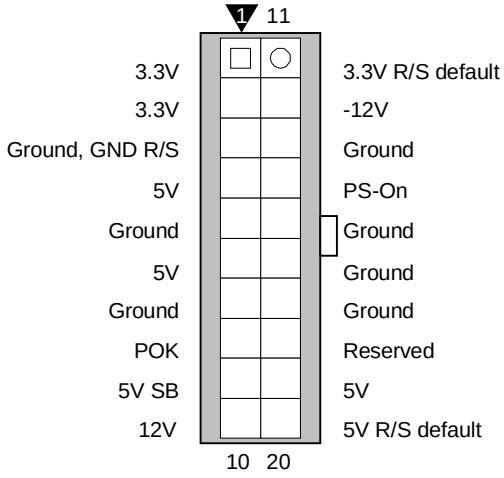


Figure 4: DC connector pinout

2.2.1.5 Power Supply Wiring Requirements

The wiring length and the desired wire color-coding are specified in Figure 5.

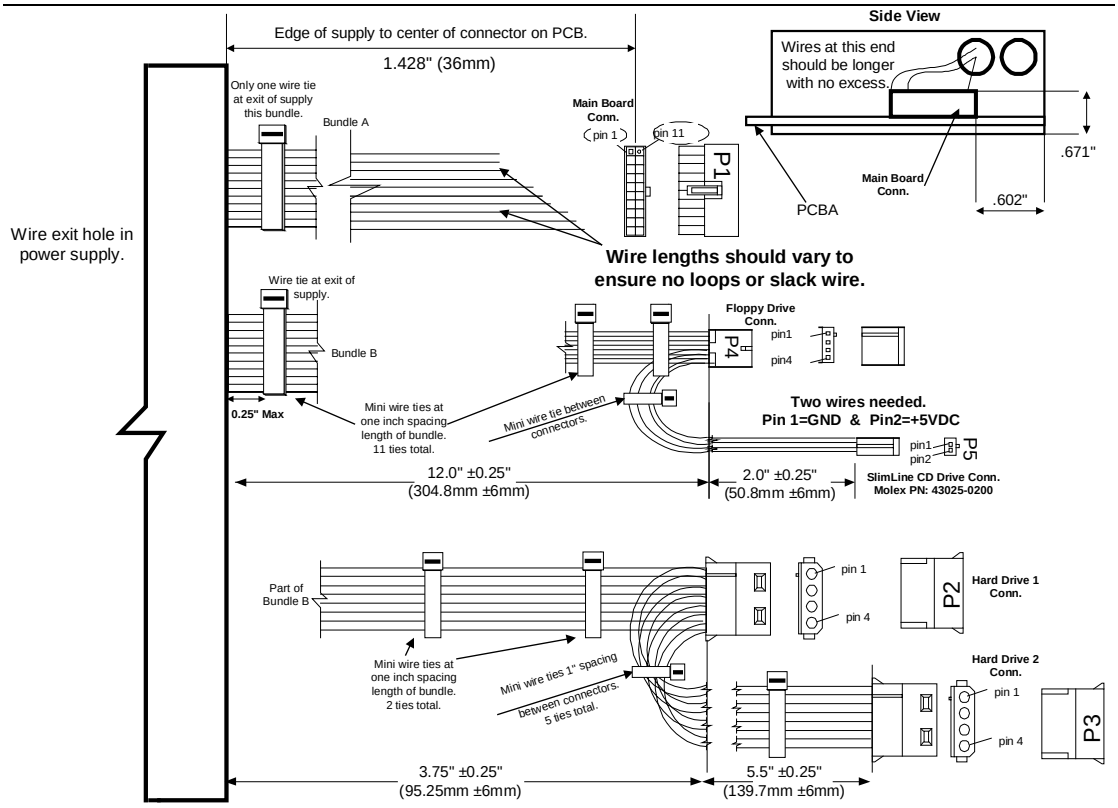


Figure 5: DC output wire harness

Table 4: Serverboard power connector (P1)

Pin	Signal Name	18 AWG Wire	Pin	Signal Name	18 AWG Wire
1	+3.3 VDC	Orange	11*	3.3VDC 3.3V default sense	Orange 22AWG Brown 22AWG
2	+3.3 VDC	Orange	12	-12 VDC	Blue
3*	Ground GND default sense	Black 22AWG Brown 22AWG	13	Ground	Black
4	+5 VDC	Red	14	PS-ON	Green
5	Ground	Black	15	Ground	Black
6	+5 VDC	Red	16	Ground	Black
7	Ground	Black	17	Ground	Black
8	PWOK	Gray	18	Reserved	White
9	+5 VSB	Purple	19	+5 VDC	Red
10	+12 VDC	Yellow	20*	+5VDC 5V default sense	Red 22AWG Brown 22AWG

* = 2 wires at one pin indicate double crimping

Table 5: Hard drive power connectors (P2, P3)

Pin	Signal Name	18 AWG Wire
1	+12 VDC	Yellow
2	Ground	Black
3	Ground	Black
4	+5 VDC	Red

Table 6: Diskette drive power connector (P4)

Pin	Signal Name	22 AWG Wire
1*	+12 VDC	Red
2*	Ground	Black
3	Ground	Black
4	+12 VDC	Yellow

* = Indicates double crimping

Table 7: Slim-line CD-ROM drive power connector (P4)

Pin	Signal Name	22 AWG Wire
1	Ground	Black
2	+5 VDC	Red

2.2.2 System Cooling

Five 40mm fans provide cooling for the system. Two of the fans are dedicated to cooling the power supply. Two of the fans provide cooling for the processor, memory and serverboard. The fifth fan cools the full-length PCI slot. A two-speed control circuit powers the fans. The control circuit is driven by a sensor that is located on the front panel

to monitor the incoming air temperature, and by a general-purpose output from the PIIX4E. The fans have a tachometer output that can be sampled through the PIIX4E. The fans can be replaced by removing the top cover, unplugging the fan connector from the serverboard, lifting the fan out of the fan bracket, and then reversing the procedure with a replacement fan.

2.2.3 System Peripheral Bays

2.2.3.1 CD-ROM and Diskette Drive Bay

The left side of the system (viewed from the front) contains the CD-ROM and diskette drive peripherals. Opening the door in the bezel exposes these peripherals. There are two options: a single 3.5" diskette size peripheral or a slim-line CD-ROM and slim-line diskette drive combination. Separate sets of mounting brackets are required for each option.

2.2.3.2 Internal 3.5" Hard Drive Bay

Space is provided for two 3.5", 1-inch thick hard drives. The drives mount to a bracket that snaps in place in the front-right side of the chassis. A pair of LEDs on the front panel indicates drive activity. Each drive can be accessed and replaced by removing the top cover.

2.2.4 System Interconnection

2.2.4.1 System Internal Cables

Table 8 lists all possible internal cables within the system. An *italicized* item is optional accessory kit and is not supplied with the base system. See Figure 6 for drawings of these cables.

Table 8: System internal cables

Cable Purpose	Qty	Description
IDE hard drives	1	Standard 40-pin IDE cable with 3 connectors; connects from primary IDE connector on the serverboard to two IDE hard drives
Diskette drive	1	Standard 34-pin diskette cable with 2 connectors; connects from standard diskette drive connector on the serverboard to one standard 3.5" diskette drive
Front panel	1	50-pin flex cable; connects from front panel connector on the serverboard to the front panel board
Slim-line CD-ROM drive	1	Standard 40-pin IDE cable with 2 connectors; connects from secondary IDE connector on the serverboard to one slim-line CD-ROM
Slim-line diskette drive	1	26-pin flex cable; connects from high-density diskette drive connector on the serverboard to one slim-line diskette drive
SCSI hard drives	1	Standard 68-pin Wide SCSI cable with 3 connectors and an LVD/SE terminator; connects from 3rd-party SCSI controller located in either the low-profile PCI slot or in the standard full-length PCI slot to two SCSI hard drives

2.2.4.2 System Cable Drawings

Figure 6 shows drawings of all the internal cables within the system and the locations of their folds. Where applicable, the darker line indicates pin 1.

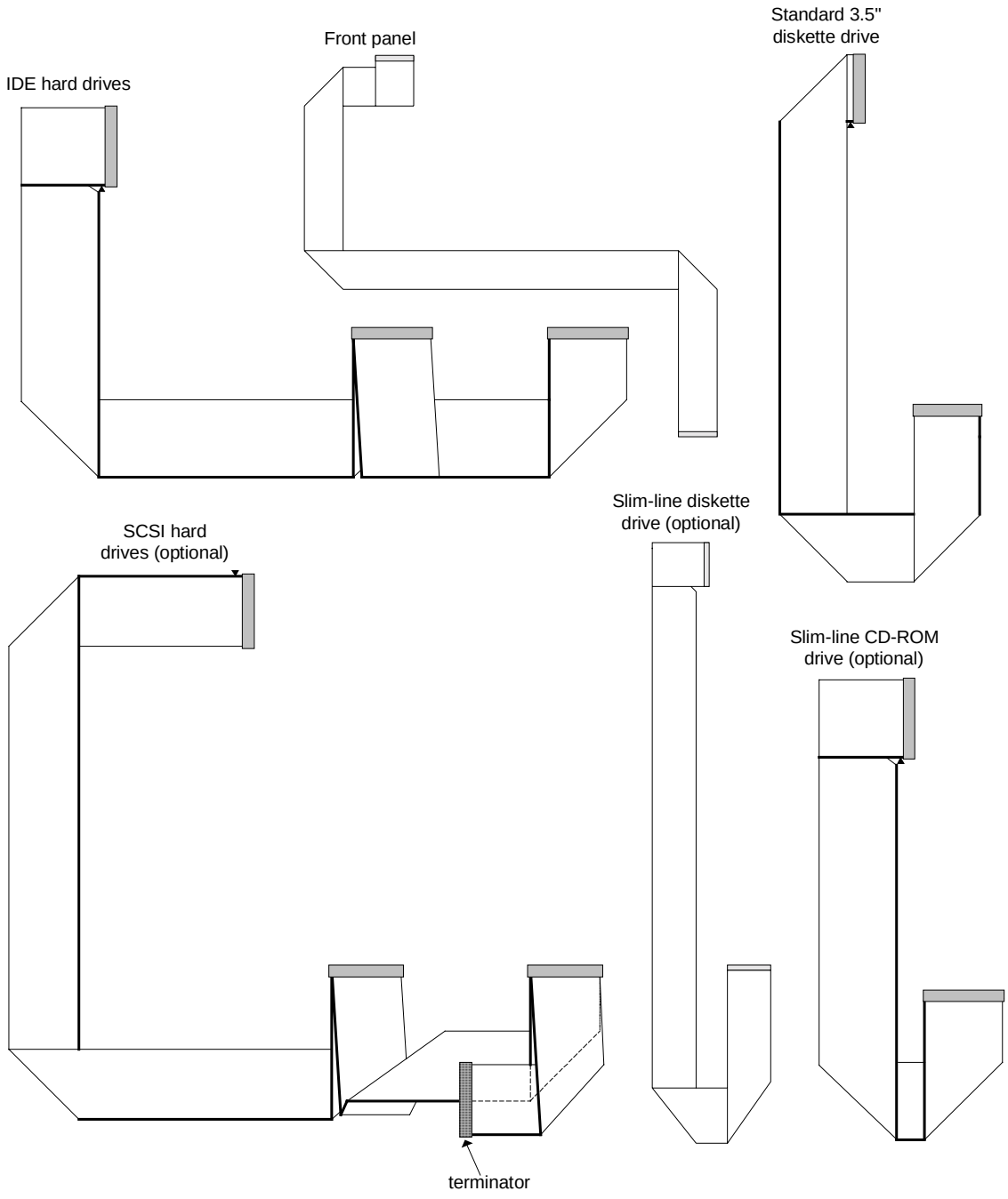


Figure 6: Internal cables

2.3 System Configuration

Table 9 lists the base configuration of the Intel® ISP1100 Internet Server.

Table 9: Standard configuration

Description	Qty
TR440BX serverboard	1
Dual-slot PCI riser card	1
Front panel board	1
125W power supply	1
System fans	5
Hard drive trays	2
3.5” diskette drive with bracket	1
Hard drive IDE cable	1
3.5” diskette drive cable	1
Front panel flex cable	1
Midmount brackets	2

Table 10 lists optional accessories.

Table 10: Optional accessories

Accessory and Spares Kits	Comments
Full Length SCSI Cable Kit	Accessory kit for full length SCSI cable
Slimline CDROM/Floppy Kit	Slimline CD/Floppy accessory kit
Rail Kit	Rail kit
Standard Spares Kit	Spares kit contains server-board, riser, power supply, and front panel
Miscellaneous Spares Kit	Contains custom cables
Accessory Front Mount	Front mount kit
Spare ISP1100 Bezel	Black bezel & titanium forehead label
Spare ISP1100 Packaging	Contains spare packaging

3 TR440BX Serverboard Description

3.1 Overview

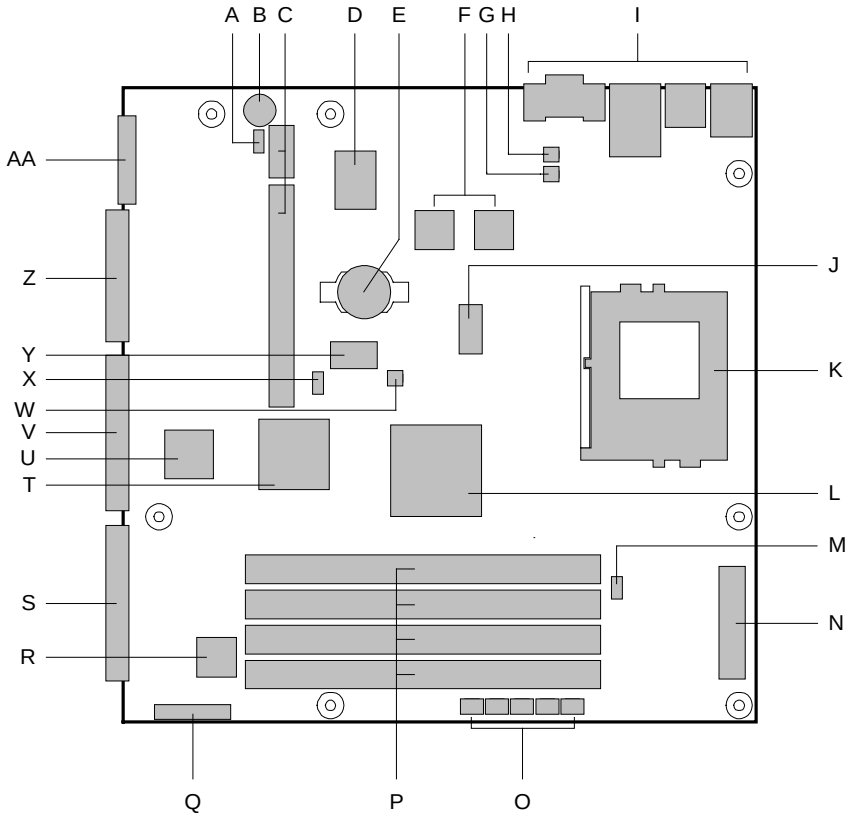
The TR440BX serverboard's features are summarized in Table 11.

Table 11: TR440BX features summary

Form Factor	microATX (9.6 inches by 9.6 inches)
Processor	Supports an Intel® Pentium® III or Celeron™ processor in a PGA370 socket
Memory	• Four 168-pin dual inline memory module (DIMM) sockets • Supports unbuffered and registered SDRAM DIMMs • Supports up to 1 GB of ECC, SPD SDRAM with registered or unbuffered DIMMs
Chipset	Intel® 82440BX AGPset, consists of: • Intel® 82443BX PCI/AGP controller (PAC) • Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)
I/O Control	SMSC FDC37B807 I/O controller
Peripheral Interfaces	• Two integrated Intel® Pro/100+ Server (82559) Ethernet controllers • One standard diskette drive interface • One high-density diskette drive interface for slim-line diskette drive • Two IDE interfaces with Ultra DMA/33 support • Two serial ports (1 rear, 1 front) • Two USB ports • Two PS/2 interfaces for keyboard and mouse • LED panel interface
Expansion Capabilities	• One PCI bus slot in combination with a 2x11 riser sideband connector supports a passive dual-slot PCI riser card (32-bit/33 MHz)
BIOS	• Intel/AMI BIOS • Intel® E28F008S585 8-Mbit boot block flash memory • Supports SMBIOS, Advanced Configuration and Power Interface (ACPI), and Plug and Play (see Section 13.2 for specification compliance levels)
Other Features	• Speaker • Hardware monitor • Wake on Ring • Wake on LAN • SCSI LED connector

3.2 Serverboard Layout

Figure 7 shows the location of the major components on the serverboard.



A	Wake on LAN connector	O	System fans connectors
B	Speaker	P	DIMM sockets
C	PCI riser sideband & PCI bus connector	Q	Front panel connector
D	SMSC I/O controller	R	Front panel controller
E	Battery	S	Primary IDE connector
F	Intel® Pro/100+ Server (82559) Ethernet controllers	T	Intel® 82371EB PIIX4E
G	SCSI LED connector	U	Gluechip
H	Wake on Ring connector	V	Secondary IDE connector
I	Back panel I/O connectors	W	Password clear jumper
J	Clock generator	X	BIOS Setup configuration jumper
K	PGA370 processor socket	Y	Flash memory
L	Intel® 82443BX PAC	Z	Diskette drive connector
M	Heceta 2 hardware monitor controller	AA	High-density diskette drive connector
N	Power supply connector		

Figure 7: Serverboard components

Figure 8 is a block diagram of the TR440BX serverboard.

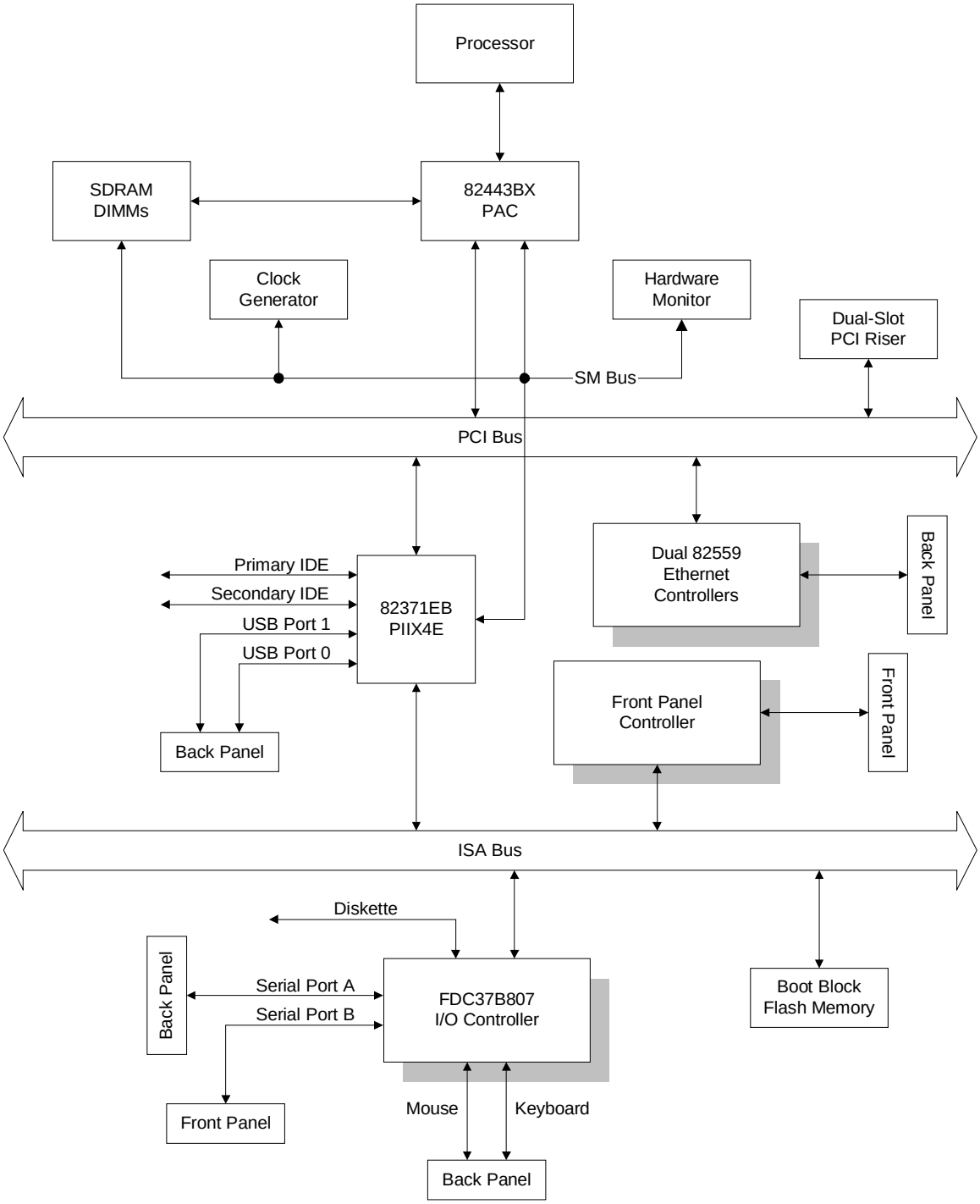


Figure 8: Serverboard block diagram

3.3 Processor

The serverboard supports a single Intel® Pentium® III or a Celeron™ processor. The host bus speed (66 MHz or 100 MHz) is automatically selected. The processor connects to the serverboard through the PGA370 socket connector. The processor must be secured by pushing the Zero-Insertion-Force (ZIF) socket's lever down. Table 12 lists processors supported by TR440BX.

Table 12: Processors supported by the TR440BX serverboard

Processor Type	L2 Cache Size	FSB Speed	Speed
Celeron™	128 KB	66 MHz	566 MHz[1]
			533 MHz
			500 MHz
			466 MHz
			433 MHz
			400 MHz
			366 MHz
Pentium® III	256 KB	100 MHz	750 MHz
			700 MHz
			650 MHz
			600E MHz
			550E MHz
			500 MHz

1 – Coppermine-128KB; other Celeron processors are based on the Mendocino core.

NOTE

The serverboard supports Pentium® III processors with a 100 MHz host bus and Celeron™ processors with a 66 MHz host bus. Processors with a 100 MHz host bus should be used only with 100 MHz SDRAM; the serverboard may not operate reliably if a processor with a 100 MHz host is paired with 66 MHz SDRAM. However, processors with a 66 MHz host can be used with either 66 MHz or 100 MHz SDRAM.

3.4 Memory

The serverboard has four DIMM sockets. Using the serial presence detect (SPD) data structure, programmed into an EEPROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Minimum memory size is 16 MB; maximum memory size is 1 GB. Memory can be installed in one, two, three or four sockets. Memory size can vary between sockets. Slot vacancy between DIMMs is permitted. Mixing of DIMM size is allowed as long as they are all unbuffered or all registered DIMMs.

The serverboard supports the following memory features:

- 168-pin SPD DIMMs with gold-plated contacts.
- 66 MHz or 100 MHz unbuffered or registered SDRAM, 72-bit ECC, 3.3V only memory.

- Single- or double-sided DIMMs in the sizes listed in Table 13.
- Unbuffered DIMMs of the following sizes: 16 MB, 32 MB, 64 MB, 128 MB and 256 MB for a maximum memory size of 1 GB.
- Registered DIMMs of the following sizes: 64MB, 128Mb and 256MB for a maximum memory size of 1 GB. Only non-stacked DIMMs are supported because of a serverboard space constraint.

Table 13: Supported memory sizes and configurations

DIMM Size	Configuration	DRAM Technology	DRAM Depth	DRAM Width	Single-sided DIMM Size x 64 bit	Double-sided DIMM Size x 64 bit
16 MB	2 Mbit x 72	16 Mb	2 Mb	8 bit	2 MB x 8 B = 16 MB	
32 MB	4 Mbit x 72	16 Mb	2 Mb	8 bit		4 MB x 8 B = 32 MB
32 MB	4 Mbit x 72	16 Mb	4 Mb	4 bit	4 MB x 8 B = 32 MB	
64 MB	8 Mbit x 72	16 Mb	4 Mb	4 bit		8 MB x 8 B = 64 MB
32 MB	4 Mbit x 72	64 Mb	4 Mb	16 bit	4 MB x 8 B = 32 MB	
64 MB	8 Mbit x 72	64 Mb	4 Mb	16 bit		8 MB x 8 B = 64 MB
64 MB	8 Mbit x 72	64 Mb	8 Mb	8 bit	8 MB x 8 B = 64 MB	
128 MB	16 Mbit x 72	64 Mb	8 Mb	8 bit		16 MB x 8 B = 128 MB
128 MB	16 Mbit x 72	64 Mb	16 Mb	4 bit	16 MB x 8 B = 128 MB	
64 MB	8 Mbit x 72	128 Mb	8 Mb	16 bit	8 MB x 8 B = 64 MB	
128 MB	16 Mbit x 72	128 Mb	8 Mb	16 bit		16 MB x 8 B = 128 MB
128 MB	16 Mbit x 72	128 Mb	16 Mb	8 bit	16 MB x 8 B = 128 MB	
256 MB	32 Mbit x 72	128 Mb	16 Mb	8 bit		32 MB x 8 B = 256 MB

When ECC memory is installed, the BIOS supports both ECC and non-ECC mode. ECC mode is enabled in the BIOS Setup program. The BIOS automatically detects if ECC memory is installed and provides the BIOS Setup option for selection ECC mode. If any non-ECC memory is installed, the BIOS Setup option for ECC mode does not appear and ECC operating is not available.

Table 14 describes the effect of using BIOS Setup to put each memory type in each supported mode.

Table 14: Memory error detection mode established in BIOS Setup program

DIMM Type	ECC Disabled	ECC Enabled
ECC	No error detection	Single-bit error correction, multiple-bit error detection
Non-ECC	No error detection	N/A

NOTE

All memory components and DIMMs used with the TR440BX serverboard must comply with the PC SDRAM Specifications. These include: the PC SDRAM Specification (memory component specific), the PC Unbuffered SDRAM Specifications, and the PC Serial Presence Detection Specification. See Section 13.2 for information about these specifications.

Processors with 100 MHz host bus speed must be paired with 100 MHz SDRAM. Processors with 66 MHz host bus speed can be paired with either 66 MHz or 100 MHz SDRAM.

3.5 Chipset

The Intel® 82440BX AGPset consists of the Intel® 82443BX PAC and the Intel® 82371EB PIIX4E bridge chip. The PAC provides an optimized DRAM controller. The PAC's Accelerated Graphics Port (AGP) interface is not used. The I/O subsystem of the 82440BX is based on the PIIX4E, which is a highly integrated PCI ISA IDE Xcelerator Bridge.

3.5.1 Intel® 82443BX PAC

The Intel® 82443BX PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, the PCI bus, and main memory. The PAC features:

- Processor interface control
  - Support for processor host bus frequency of 66 MHz and 100 MHz
  - 32-bit addressing
  - Desktop optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for:
  - +3.3 V only DIMM DRAM configurations
  - Up to four double-sided DIMMs
  - 100-MHz or 66-MHz SDRAM (depending on the processor installed)
  - DIMM serial presence detect via SMBus interface
  - 16-, 64- and 128-Mbit devices with 2 KB, 4 KB, and 8 KB page sizes
  - x 4, x 8, and x 16 DRAM widths
  - Symmetrical and asymmetrical DRAM addressing
  - ECC SEC/DED
- PCI bus interface
  - Complies with the PCI specification Rev. 2.1, +5V 33-MHz interface (see Section 13.2 for specification information)
  - Asynchronous coupling to the host-bus frequency
  - PCI parity generation support
  - Data streaming support from PCI-to-DRAM
  - Support for four PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - Support for concurrent host and PCI transactions to main memory
- Data buffering
  - DRAM write buffer with read-around-write capability
  - Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1-to-DRAM read buffers
- Power management functions
  - Support for system suspend/resume
  - Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

3.5.2 Intel® 82371EB (PIIX4E)

The PIIX4E is a multifunctional PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunctional PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Support for PCI Rev 2.1 Specification
  - Full ISA bus support
- USB Controller
  - Two USB ports (see Section 13.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for Universal Host Controller Interface (UHCI) Design Guide (see Section 13.2 for specification information)
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers at up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake on Ring and Wake on LAN
  - Support for ACPI Revision 1.0 (see Section 13.2 for specification information)
- Real-Time Clock
  - 256-byte battery-backed CMOS SRAM
  - Date alarm
  - 16-bit counters/timers based on 82C54

3.5.3 USB

The serverboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel I/O connectors. The serverboard fully supports UHCI and uses UHCI-compatible software drivers. See Section 13.2 for information about the USB and UHCI specifications.

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

3.5.4 IDE Support

The serverboard has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 74.

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The TR440BX supports PCMCIA ATA Type II flash card technology through its IDE interfaces. No special driver is needed for a PCMCIA ATA Type II flash drive. Most popular operating systems see it as a standard IDE drive.

3.5.5 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multi-century calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25ºC with 3.3VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

The recommended method of accessing the date in systems with Intel serverboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel serverboards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For more information on a proper date access in systems with Intel serverboards, please visit:
http://support.intel.com/support/year2000/

3.6 I/O Controller

The FDC37B807 I/O controller from SMSC is an ISA Plug and Play-compatible, multifunctional I/O device that provides the following features (see Section 13.2 for Plug and Play specification information):

- Two serial ports
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Three-mode diskette drive support (driver required)
- FIFO support on both serial and diskette drive interfaces
- PS/2† -style mouse and keyboard interfaces
- Support for serial IRQ packet protocol
- Intelligent power management, including:
  - Shadowed write-only registers for ACPI compliance
  - Programmable wake up event interface

The BIOS Setup program provides configuration options for the I/O controller.

3.6.1 Serial Ports

The serverboard has two 9-pin D-Sub serial port connectors: one located on the back panel and one located on the front panel under the bezel cover. The front panel serial port connector is connected in parallel with the serial port B D-Sub connector located on the rear of the chassis. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), or COM3 (3E8h).

3.6.2 Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077-diskette drive controller and supports both PC-AT† and PS/2 modes. In the BIOS Setup program, the diskette driver interface can be configured for the following capacities and sizes:

- 360 KB, 5.25-inch
- 720 KB, 3.5-inch
- 1.25/1.44 MB, 3.5-inch
- 1.2 MB, 5.25-inch
- 1.2 MB, 3.5-inch (driver required)
- 2.88 MB, 3.5-inch

NOTE

The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required for this type of drive (three-mode).

3.6.3 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power on/reset. A power on/reset password can be specified in BIOS Setup.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

NOTE

The mouse and keyboard can be plugged into either of the PS/2 connectors. Turn off power to the computer before connecting or disconnecting a keyboard or mouse.

3.7 Hardware Monitor

The Heceta 2 system monitor controller is provided on the serverboard. This device may be used to monitor internal temperature, voltage and fan speed. Temperature is monitored through a sensor internal to the Heceta 2, monitoring the ambient temperature of the area of the board in which the Heceta 2 device is located. The Heceta 2 monitors +5V, +3.3V, +12V, and –12V, +1.5V, and the processor core voltage. The Heceta 2 may be used to monitor the speed (the tachometer output) of a fan. The five system fans' tachometer outputs are multiplexed to the Heceta 2 device to allow individual monitoring. Using software through the PIIX4E chip controls, each fan tachometer outputs is routed to the Heceta 2 chip. The multiplexer control bits (FAN_MUXCTL0 and FAN_MUXCTL1) are connected to the PIIX4E outputs GPO0 and GPO13, respectively. Table 15 below shows the fan tachometer mapping.

Table 15: Fan tachometer MUX control mapping

FAN_MUXCTL0	FAN_MUXCTL1	Heceta FAN1_TACH input	Heceta FAN2_TACH input
0	0	Fan 1 (J35)	Fan 4 (J38)
0	1	Fan 2 (J34)	Fan 5 (J37)
1	0	Fan 3 (J33)	NONE
1	1	NONE	NONE

The Heceta 2 is set up and interfaced with through the PIIX4E's SMBUS interface. Out of band or absolute thresholds can be set for the monitored functions using the SMBUS interface. Threshold faults are available by polling the Heceta 2 via the SMBUS interface. The Heceta 2 updates its information approximately every 1 second.

For more details on programming and reading of Heceta 2, see Section 13.2 for information specification.

3.8 SCSI Hard Drive LED Connector

The SCSI hard drive LED connector is a 1 x 2-pin connector that allows add-in SCSI controller applications to use the same LED as the IDE controller. This connector can be connected to the LED output of the add-in controller card. See Section 3.16.2.1 for the location and pinouts of the SCSI hard drive LED connector.

3.9 Intel® Pro/100+ Server (82559) Ethernet Controllers

Two Intel Pro/100+ Server (82559) Ethernet controllers provide two 10/100Base-T interfaces, which are accessible from the back panel. See Section 3.16.1 for location and pinouts of the LAN connectors.

The LAN connectors on the back panel do not provide LEDs to indicate transmit/receive activity and speed. Instead, these indicators are routed to four LEDs on the front panel. See Section 5.4 for LED definitions.

Wake on LAN features are supported by the TR440BX software and the SMBUS interface of the Intel 82559s. See Section 6 (BIOS specification) for information regarding Alert on LAN and Wake on LAN. Also see the next section for information on Wake on LAN.

⚠ CAUTION

For Wake on LAN, the 5V standby line for the power supply must be capable of delivering +5V ± 5% at 720mA. Failure to provide adequate standby current when implementing Wake on LAN can damage the power supply.

3.10 Wake on LAN

Wake on LAN (WOL) enables remote wakeup of the computer through a network. If a PCI add-in network interface card (NIC) with remote wakeup capabilities is desired, the remote wakeup connector on the NIC must be connected to the on-board Wake on LAN technology connector.

The integrated LAN controllers or the add-in NIC monitor network traffic at the MII interface; upon detecting a Magic Packet†, the LAN controllers or NIC assert a wakeup signal that powers up the computer.

To access this feature, use the optional Wake on LAN connector on the serverboard. See Section 3.16.2.2 for the location and pinouts of the Wake on LAN connector.

3.11 Wake on Ring and Resume on Ring

Wake on Ring enables the computer to wake from sleep or soft-off mode when a call is received on a telephony device, such as a faxmodem. The TR440BX serverboard provides three methods for implementing Wake on Ring.

- An external modem connected to Serial Port A (rear) can toggle the super I/O controller's Ring Indicator pin which should be enabled to cause a wakeup event.
- The 2-pin Wake on Ring header may be shorted to cause a wakeup event.
- A PCI modem may implement a Wake on Ring circuit that uses PCI PME# to cause a wakeup event.

This section describes two technologies that enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) being used. .

NOTE

Wake on Ring and Resume on Ring requires the support of an operating system that provides full ACPI functionality.

3.11.1 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from ACPI S5 state
- Requires two calls to access the computer:
  - First call powers up the computer
  - Second call enables access (when the appropriate software is loaded)
- Detects incoming calls differently for external and internal modems:
  - For external modems, the serverboard hardware monitors the Ring Indicator (RI) input of serial port A and B.
  - For internal modems, a cable must be routed from the modem to the Wake on Ring connector

See Section 3.16.2.2 for the location and pinouts of the Wake on Ring connector.

3.11.2 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming calls similarly for external and internal modems; does not use the Wake on Ring connector
- Requires modem interrupt be unmasked for correct operation

3.12 SMI and NMI Routing

There are numerous SMI sources. All SMI sources are routed to the PIIX4E. Software must configure the PIIX4E SMI source pins to control whether or not SMIs will be propagated through to the processor via its H_SMI input or not. For details on the fault conditions that cause SMI to occur, consult the data sheets of the SMI source ICs. The SMI routing on TR440BX is described in Table 16 below. Note that some PIIX4E inputs have several sources. Schematic signal names are in parenthesis.

Table 16: SMI and NMI routing table

SMI Source	PIIX4E Input Pin
BX Chipset PCI SERR# - used for ECC Errors (P_SERR#)	EXT_SMI#
LAN PCI SERR# (P_SERR#)	EXT_SMI#
All PCI Slot's SERR# (P_SERR#)	EXT_SMI#
Gluechip's EXTSMI# output – used for +5VSB errors	GPI13
Gluechip's EXTSMI# output – through buffer to (P_SERR#)	EXT_SMI#
LAN-1 PCI PME# (P_PME#)	GPI1
LAN-2 PCI PME# (P_PME#)	GPI1
All two PCI slot's PME# (P_PME#)	GPI1

SMI Source	PIIX4E Input Pin
Super I/O Serial Interrupt SMI – used for watchdog timer (SER_IRQ)	SER_IRQ
Super I/O PME# (SIO_RIA#) – originally from WOR header or ext. modem	RIAB
Wake on LAN header – used for Wake on LAN (WOL#)	LID

The Gluechip's EXT_SMI# output is also connected to the PIIX4E GPI13 pin to provide a status of the Gluechip's EXT_SMI# signal.

All NMI generation on TR440BX is under software control. Writes to PIIX4E GPO17 are routed to the PIIX4E IOCHK# input which may be configured to cause an NMI to occur. Thus software may cause an NMI to occur by pulsing GPO17 active.

The TR440BX BIOS SMI handler will detect SMI events, log the events, and elevate selected events to NMI level.

3.13 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the serverboard can turn off the system power through software control. See Section 13.2 for information about the microATX specification.

To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct command from the operating system, the BIOS turns off power to the computer.

With Last State enabled in the BIOS (see Table 78), if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

3.14 Speaker

A 47 Ω inductive speaker is mounted on the serverboard. The speaker provides audible error code (beep code) information during the Power-On Self-Test (POST). See Section 8.5 for beep codes.

3.15 Fan Support

The board has five fan connectors. Table 17 describes the functions of the fan connectors.

Table 17: Fan connectors description

Connector	Function
Fan 1 (J35)	Supports fan speed sensing for fans with tachometer outputs. Connector supports variable fan speed.
Fan 2 (J34)	Supports fan speed sensing for fans with tachometer outputs. Connector supports variable fan speed.
Fan 3 (J33)	Supports fan speed sensing for fans with tachometer outputs. Connector supports variable fan speed.
Fan 4	Supports fan speed sensing for fans with tachometer outputs.

Connector	Function
(J38)	Connector supports on/off fan control or variable fan speed via a fuse stuffing option.
Fan 5	Supports fan speed sensing for fans with tachometer outputs.
(J37)	Connector supports on/off fan control or variable fan speed via a fuse stuffing option.

3.16 Connectors

This section describes the serverboard's connectors. The connectors can be divided into three groups, as shown in Figure 9.

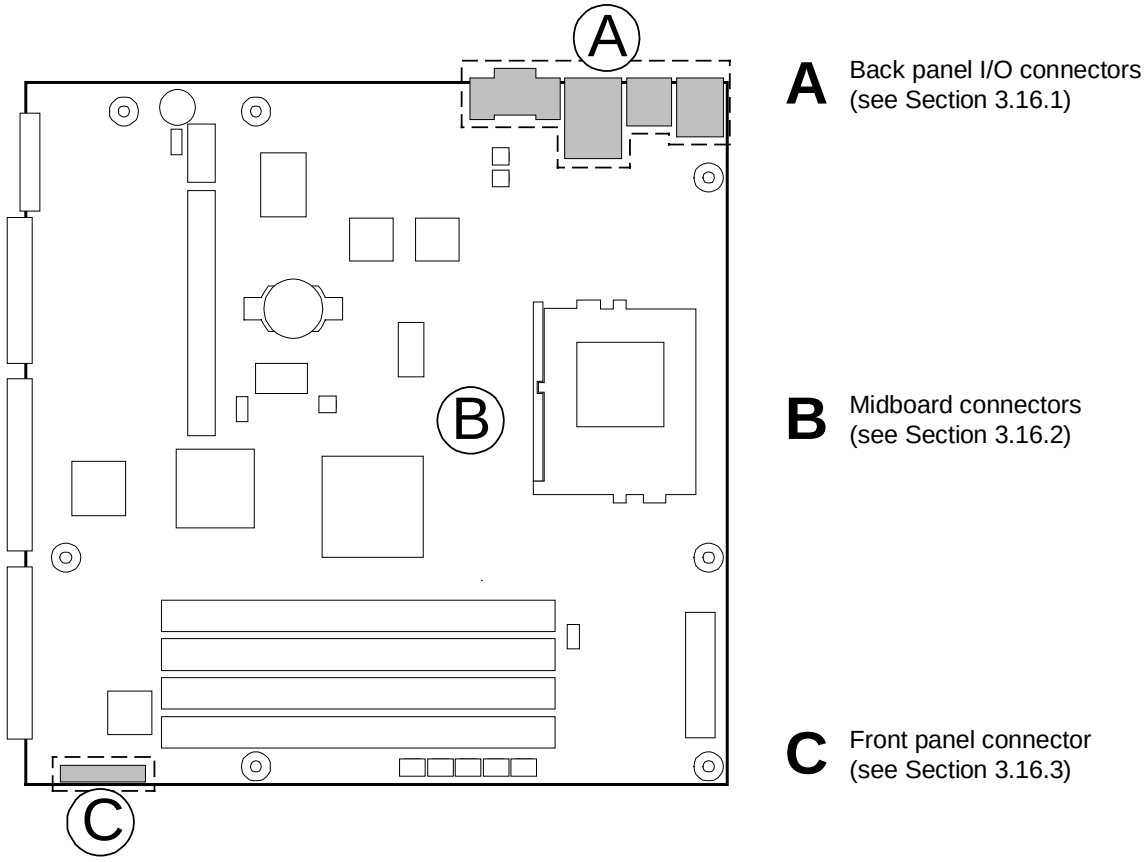


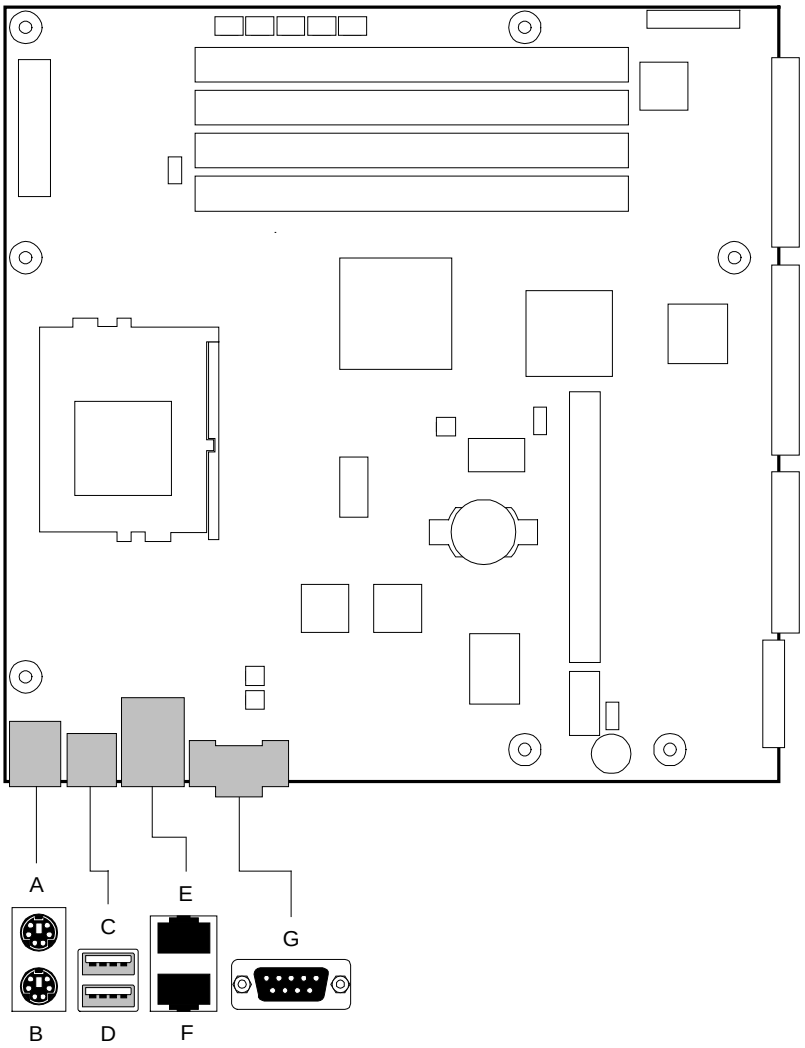
Figure 9: Connector groups

⚠ CAUTION

Only the back panel connectors of this serverboard have overcurrent protection. The internal serverboard connectors are not overcurrent protected, and should connect only to devices inside the computer chassis, such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

3.16.1 Back Panel I/O Connectors

Figure 10 shows the location of the back panel I/O connectors.



A	PS/2 keyboard or mouse connector	E	LAN #2 connector
B	PS/2 keyboard or mouse connector	F	LAN #1 connector
C	USB port 0 connector	G	Serial port A connector
D	USB port 1 connector		

Figure 10: Back panel I/O connectors

Table 18: PS/2 keyboard/mouse connectors (J8)

Pin	Signal Name
1	Keyboard or Mouse Data
2	Not connected
3	Ground
4	Fused +5 V
5	Keyboard or Mouse Clock
6	Not connected

Table 19: USB stacked connector (J7)

Pin	Signal Name	Pin	Signal Name
1	Fused +5 V	5	Fused +5 V
2	3.3 V differential USB signal USB_D-	6	3.3 V differential USB signal USB_D-
3	3.3 V differential USB signal USB_D+	7	3.3 V differential USB signal USB_D+
4	Ground	8	Ground

Note: J7 (top) is port #1 and J7 (bottom) is port #2.

Table 20: LAN RJ45 connectors (J6-A, J6-B)

Pin	Signal Name	Pin	Signal Name
1	TX+	1	TX+
2	TX-	2	TX-
3	RX+	3	RX+
4	Return	4	Return
5	Return	5	Return
6	RX-	6	RX-
7	Return	7	Return
8	Return	8	Return

Note: J6-A (bottom) is LAN #1 and J6-B (top) is LAN #2.

Table 21: Serial port A connector (J5)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	SIN # (Serial Data In)
3	SOUT # (Serial Data Out)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

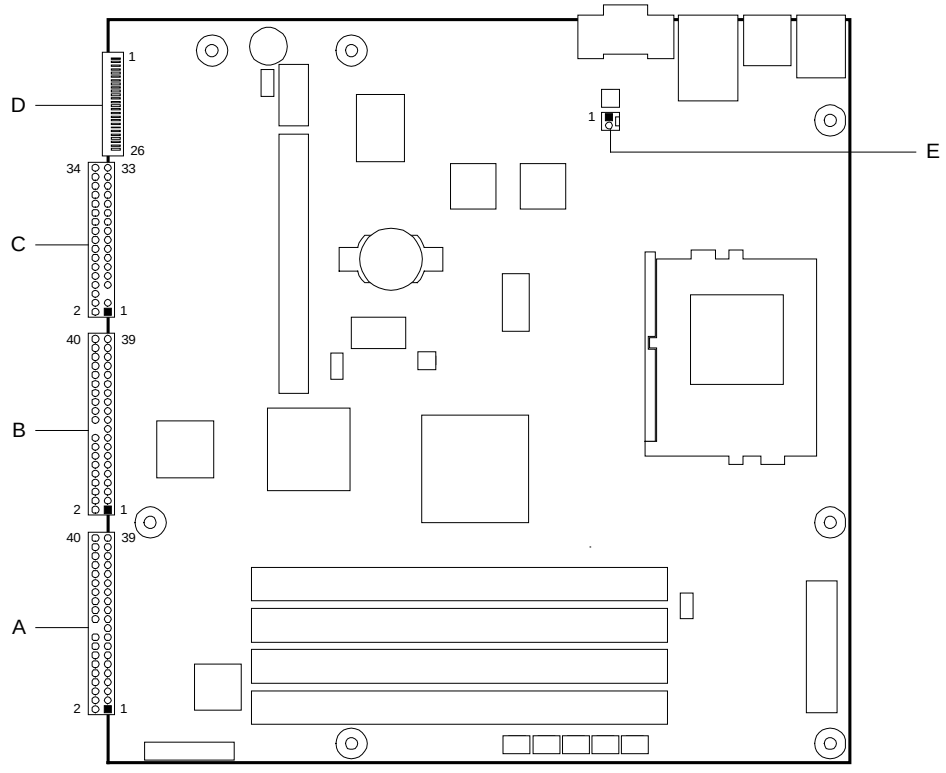
3.16.2 Midboard Connectors

The midboard connectors are divided into three functional groups:

- Peripheral interfaces (see Section 3.16.2.1)
  - SCSI LED
  - Diskette Drive
  - IDE
- Hardware management and Power (see Section 3.16.2.2)
  - Fans
  - Power
  - Wake on Ring
  - Wake on LAN
- Add-in board (see Section 3.16.2.3)
  - PCI bus
  - PCI riser sideband connector

3.16.2.1 Peripheral Interfaces

Figure 11 shows the locations of the peripheral interface connectors.



A Primary IDE connector
B Secondary IDE connector
C Diskette drive connector
D High-density diskette drive connector
E SCSI LED connector

Figure 11: Peripheral connectors

Table 22: SCSI LED connector (J11)

Pin	Signal Name
1	SCSI activity
2	Not Connect

Table 23: Diskette drive connector (J17)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 24: High-density diskette drive connector (J41)

Pin	Signal Name	Pin	Signal Name
1	FDHEAD# (Side 1 Select)	2	Ground
3	FDRDATA# (Read Data)	4	Ground
5	FDWPD# (Write Protect)	6	Ground
7	FDTRK0# (Track 0)	8	Ground
9	FDWE# (Write Enable)	10	Ground
11	FDWD# (Write Data)	12	Ground
13	FDSTEP# (Step Pulse)	14	DENSEL
15	FDDIR# (Stepper Motor Direction)	16	+5 V Fused
17	FDM00# (Motor Enable A)	18	No connect
19	No connect	20	No connect
21	DSKCHG# (Diskette Change)	22	+5 V Fused
23	FDDS0# (Drive Select A)	24	+5 V Fused
25	FDINDX# (Index)	26	+5 V Fused

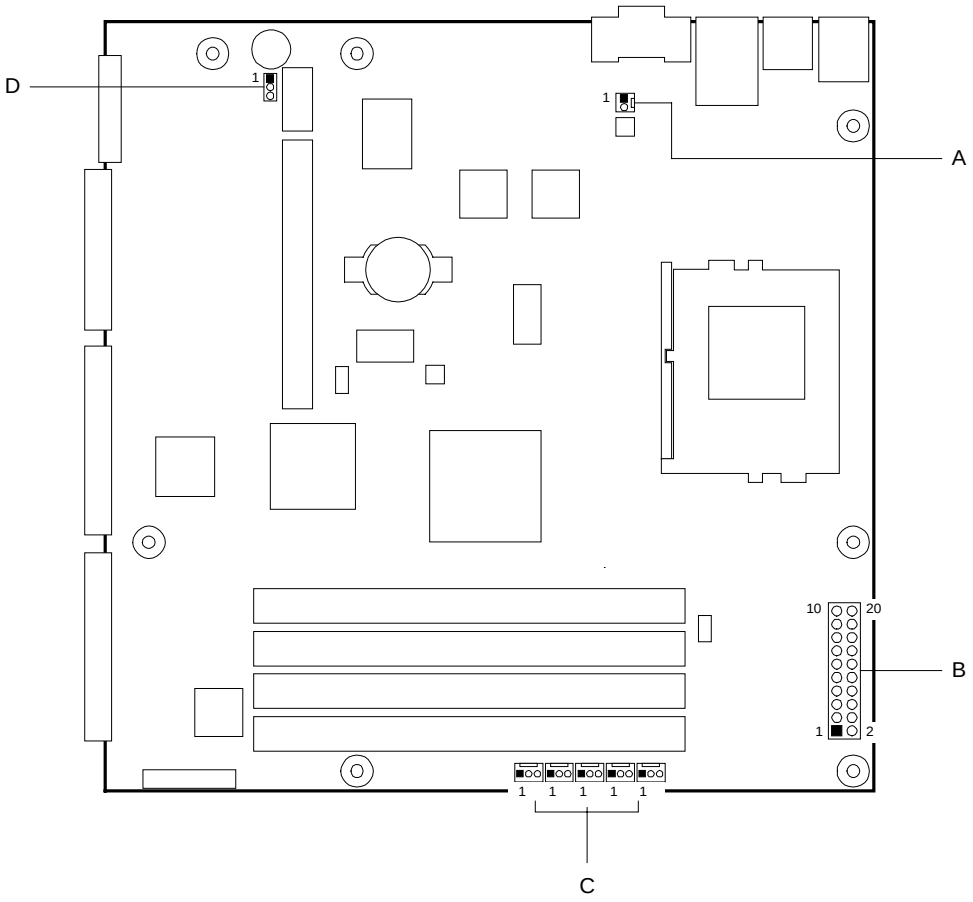
Table 25: IDE connectors (J27-primary, J23-secondary)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key (NC)
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pull-up)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	Reserved
35	DAG0 (Address 0)	36	DAG2Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Hard Disk Activity#	40	Ground

Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

3.16.2.2 Hardware Management and Power

Figure 12 shows the locations of the hardware management and power connectors.



A Wake on Ring connector
B Power supply connector
C System fans connectors
D Wake on LAN connector

Figure 12: Hardware management and power connectors

Table 26: Power connector (J30)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB (Standby for real-time clock)	19	+5 V
10	+12 V	20	+5 V

Table 27: System fans connectors (J33, J34, J35, J37, J38)

Pin	Signal Name
1	Ground
2	+12 V
3	Fan Tachometer Output

Table 28: Wake on Ring connector (J14)

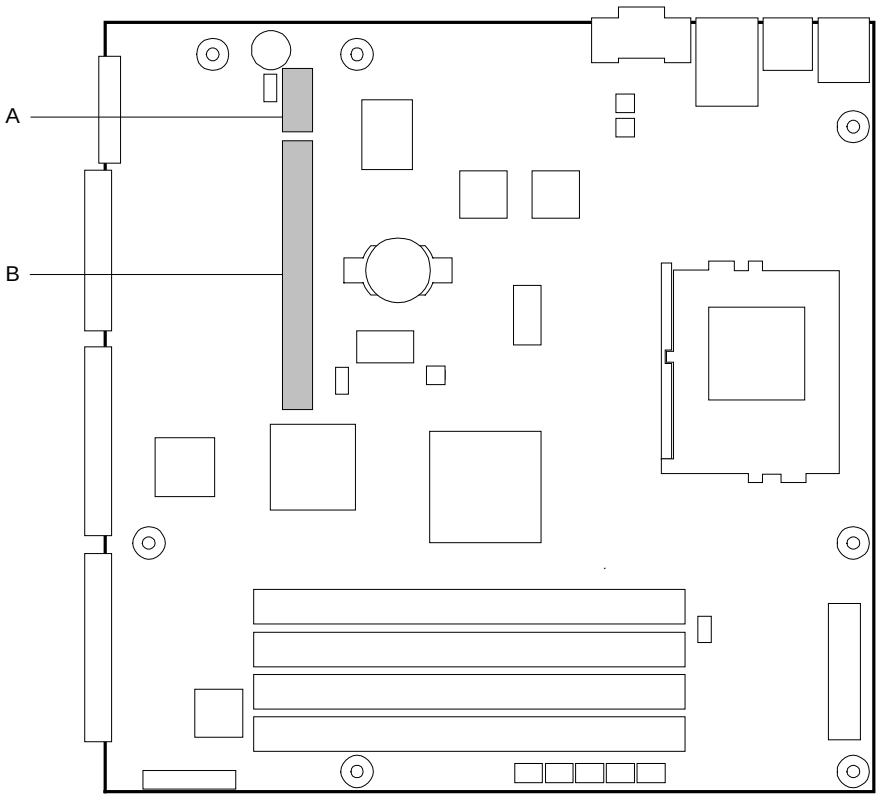
Pin	Signal Name
1	Ground
2	RINGA#

Table 29: Wake on LAN connector (J9)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

3.16.2.3 Add-in Board

Figure 13 shows the location of the PCI riser sideband and PCI bus connector.



A PCI riser sideband connector

B PCI bus connector

Figure 13: PCI riser sideband and PCI bus connectors

Table 30: PCI riser sideband connector (J13)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground	B1	CK_PCI_S3_33M	A7	SMB_CLK	B7	AD17
A2	NC	B2	Ground	A8	+12 V	B8	Ground
A3	Ground	B3	P_REQ[1]#	A9	NC	B9	SMB_DATA
A4	NC	B4	Ground	A10	+5 V	B10	+3.3 V
A5	Ground	B5	P_GNT[1]#	A11	+5 V	B11	+3.3 V
A6	NC	B6	Ground				

Table 31: PCI bus connector (J20)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TRST#	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	TCK	A33	+3.3 V	B33	C/BE2#
A3	TMS	B3	Ground	A34	FRAME#	B34	Ground
A4	TDI	B4	TDO	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved1	B9	PRSNT1#	A40	SDONE	B40	PERR#
A10	+5 V	B10	Reserved2	A41	SBO#	B41	+3.3 V
A11	Reserved3	B11	PRSNT2#	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V AUX	B14	Reserved5	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V	B59	+5 V
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

3.16.3 Front Panel Connector

Figure 14 shows the location of the front panel connector.

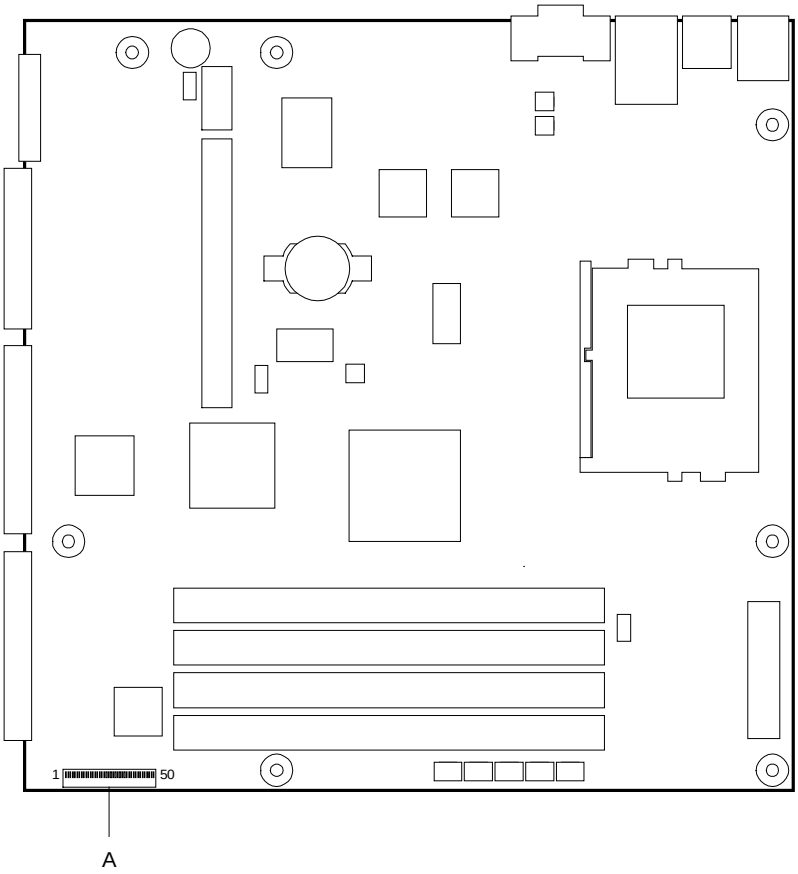


Figure 14: Front panel connector

Table 32: Front panel I/O connector (J32)

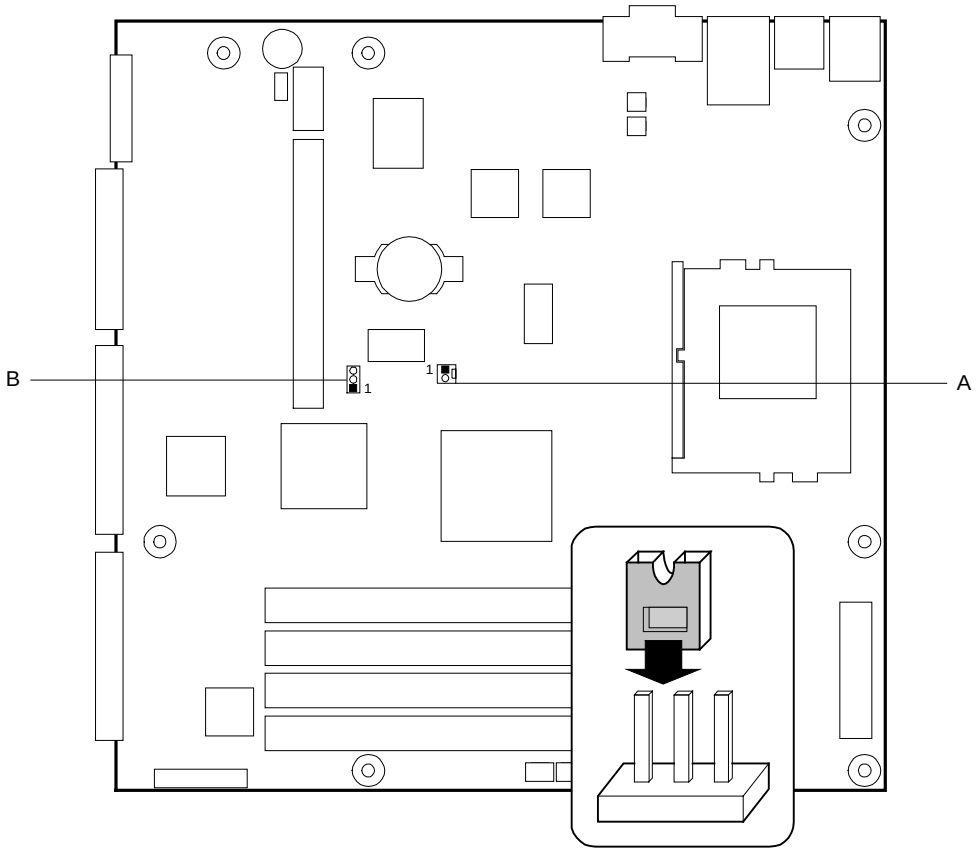
Pin	Signal Name	Pin	Signal Name
1	GND	2	+5V Power
3	D1	4	D0
5	D2	6	GND
7	D3	8	D4
9	D5	10	GND
11	D6	12	D7
13	GND	14	Reserved
15	Reserved	16	Reserved
17	DSR2	18	Reserved
19	CS2	20	FP_TYPE_BIT1
21	CS1	22	RI2
23	LED_GREEN_BLINK	24	Reserved
25	LED_YELLOW_BLINK	26	Reserved
27	LED_HDD	28	RESET_SW#
29	+5V Standby Power	30	POWERON_SW#
31	+3.3V	32	THERM_TRIP#
33	SLEEP_SWITCH#	34	NMI
35	Reserved	36	Reserved
37	LAN1_ACTLED	38	LAN2_ACTLED
39	LAN1_LINKLED	40	LAN2_LINKLED
41	LAN1_SPEEDLED	42	LAN2_SPEEDLED
43	PROG_LED1	44	PROG_LED2
45	SIN2#	46	SOUT2#
47	RTS2	48	CTS2
49	DTR2	50	DCD2

3.17 Jumper Blocks

Figure 15 shows the locations of the password clear and BIOS Setup configuration jumpers.

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.



A Password clear jumper

B BIOS Setup configuration jumper

Figure 15: BIOS Setup configuration and password override jumpers

Table 33: BIOS Setup configuration jumper settings (J22)

Function / Mode	Jumper	Configuration
Normal	1 - 2	The BIOS uses current configuration information and passwords for booting.
Configure	2 - 3	After the POST runs, Setup runs automatically and clears CMOS.
Recovery	None	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

Table 34: Password clear jumper settings (J39)

Function / Mode	Jumper	Configuration
Normal	None	Do nothing.
Clear passwords	1 - 2	Clear passwords.

NOTE

Password override can be monitored via GPI(15) on the PIIX4E at I/O address 0x432 bit 7. This bit is intended to enable the software to determine if the password set needs to be overridden because the password has been forgotten.

3.18 Mechanical Form Factor

Figure 16 gives the dimensions of the TR440BX and locations of the screw holes.

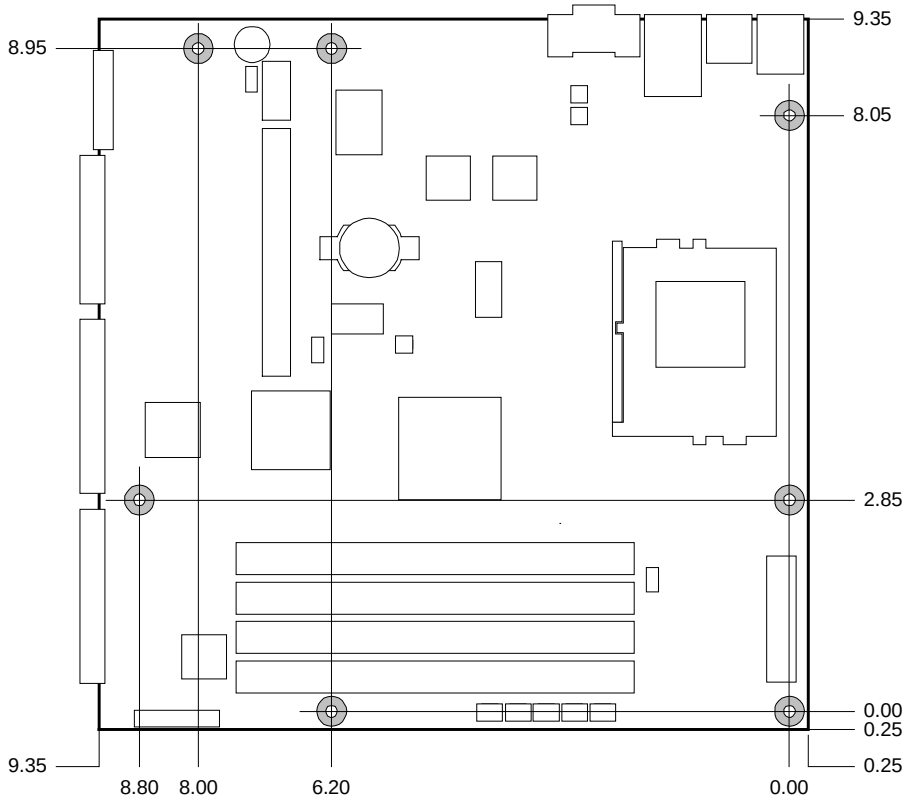
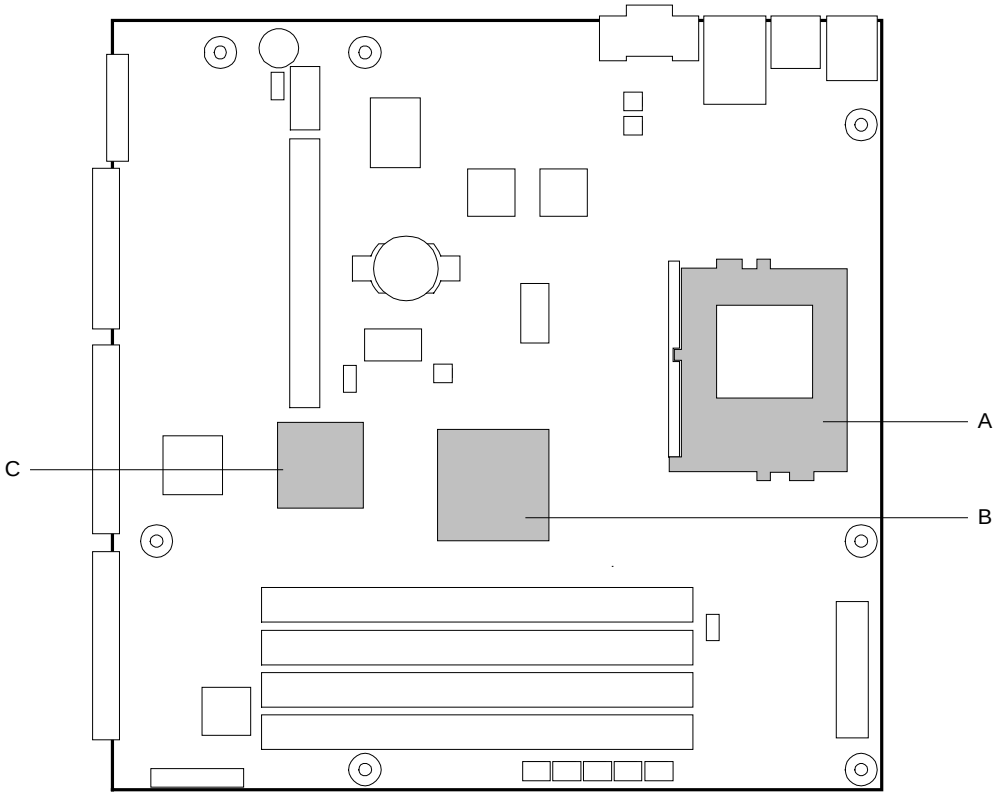


Figure 16: Serverboard dimensions

3.19 Thermal Considerations

Figure 17 shows the locations of the thermally sensitive components. Table 35 provides maximum component case temperatures for serverboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the serverboard.



A PGA370 socket

B Intel® 82443BX PAC

C Intel® 82371EB PIIX4E

Figure 17: Thermally-sensitive components

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5°C to 10°C could cause components to exceed maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 10.4.

Table 35: Thermal considerations for components

Component	Speed	Maximum Temperature
Celeron™ processor	566[1] MHz	85°C (thermal case)
	533 MHz	85°C (thermal case)
	500 MHz	85°C (thermal case)
	466 MHz	85°C (thermal case)

Component	Speed	Maximum Temperature
	433 MHz	85°C (thermal case)
	400 MHz	85°C (thermal case)
	366 MHz	85°C (thermal case)
Pentium® III processor	750 MHz	85°C (thermal case)
	700 MHz	85°C (thermal case)
	650 MHz	85°C (thermal case)
	600E MHz	85°C (thermal case)
	550E MHz	85°C (thermal case)
	500 MHz	85°C (thermal case)
Intel® 82443BX PAC		105°C
Intel® 82371EB PIIX4E		85°C

1 – Coppermine-128KB; other Celeron processors are based on the Mendocino core.

3.20 Power Requirements

Table 36: TR440BX serverboard power requirements

Volts	+3.3V	+5V	+12V	-12V	+5Vs/b
Amps	5.46	11.82	2.88	0.2	1.0
Avg	5.5	12	3	0.2	1.0
Watts	18.15	60	36	2.4	5.0
Tolerance	-3%/+5%	-4%/+5%	+/-5%	+/-10%	-4%/+5%

Total TR440BX board power requirement = 121.55 Watts

3.21 DC Voltage Regulation

Table 37 shows the DC output voltages that shall remain within the regulation ranges shown measured at the load end of the output connectors under all line, load, and environmental conditions including Transients and Ripple & Noise.

Table 37: DC output voltage regulation

Output Voltage	Range	Min.	Nom.	Max.	Unit
+3.3VDC	-3% / +5%	+3.2	+3.30	+3.465	Volts
+ 5 VDC	-4% / +5%	+4.8	+5.00	+5.25	Volts
+12 VDC*	± 5%	+11.40	+12.00	+12.60	Volts
-12 VDC	± 10%	-10.80	-12.00	-13.20	Volts
+ 5 VSB	-4% / +5%	+4.8	+5.00	+5.25	Volts

* At +12V/12sec surge, 12V output regulation can go to ±10%.

3.22 PCI Configuration Space Map

Table 38: PCI configuration space map

Bus # (hex)	Device # (hex)	Function # (hex)	Description
00	00	00	Intel® 82443BX (PAC)
00	01	00	Intel® 82443BX PCI/AGP bridge
00	07	00	Intel® 82371EB (PIIX4E) PCI/ISA bridge
00	07	01	Intel® 82371EB (PIIX4E) IDE bus master
00	07	02	Intel® 82371EB (PIIX4E) USB
00	07	03	Intel® 82371EB (PIIX4E) power management
00	0C	00	PCI LAN 1
00	0D	00	PCI LAN 2
00	0E	00	PCI bus connector 1
00	0F	00	PCI bus connector 2

3.23 Interrupts

Table 39: Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	PIIX4E PCI Interrupt B
6	Diskette Drive
7	LPT1*
8	Real Time Clock
9	Reserved for PIIX4E system management bus, on-board LAN
10	PIIX4E PCI Interrupt D
11	PIIX4E PCI Interrupt A
12	On-board Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

3.24 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connector and on-board PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD. (This is not an absolute requirement.)

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either on-board or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the serverboard and therefore share the same interrupt. Table 40 lists the PIRQX signals and shows how the signals are connected to the PCI bus connectors and to on-board PCI interrupt sources.

Table 40: Serverboard PCI connector interrupt routing map

PIIX4E PIRQ Signal Name	PCI Bus Connector 1* (J20)	PCI LAN 1	PCI LAN 2
PIRQA	INTA		
PIRQB	INTB	INTA	INTA
PIRQC	INTC		
PIRQD	INTD		

* Note: For PCI interrupt routing map of PCI slots on the riser card, see Section 4.1.2.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3.25 LED Definitions and Control

The PIIX4E is configured to use four general-purpose outputs for LED control. GPO30:29 controls the first two LEDs – power on/sleep (green) and system fault (amber). The LEDs may be toggled by writing to bits 6:5 of the PIIX4E GPO I/O register 0x437. The GPO values are inverted before being used by the Gluechip 2 to drive the LEDs. Thus, on reset or power-on, the LEDs default to a blinking amber. Once the BIOS has determined that

the system is OK, the LED should be changed to solid green by writing 00b to bits 6:5 of register 0x437. See Table 41 for the LED functionality.

Table 41: LED programming chart

PIIX4E Register Addr 0x437, Bits 6:5	LED State Power On/Sleep	LED State System Fault
00	Solid Green (Power On)	Off
01	Blinking Green (Sleep)	Off
10	Off	Solid Amber
11	Off	Blinking Amber*

* = Reset and power-on default value

Two additional user-programmable LEDs are controllable via the PIIX4E. These LEDs are reserved for user functions and can be accessed in much the same way as above. GPO28 and GPO8 control the two user-programmable LEDs; both are green. The LEDs may be toggled by writing to bit 4 of the PIIX4E GPO I/O register 0x437 and bit 0 of PIIX4E GPO I/O register 0x435. The GPO values are reset to zero on reset or power-on. Once the BIOS or a driver is installed and running, the LEDs can be programmed to light as desired. See the Table 42 below for the LED functionality.

Table 42: User-programmable LEDs programming chart

PIIX4E Register Addr 0x437, Bit 4 (GPO28)	PIIX4E Register Addr 0x435, Bit 0 (GPO8)	LED State User Prog #1	LED State User Prog #2
0	0	Off*	Off*
0	1	Off	On (Green)
1	0	On (Green)	Off
1	1	On (Green)	On (Green)

* = Reset and power-on default value

3.26 System Management Bus (SMB)

The TR440BX serverboard supports a simple I^2C compatible Bus to provide a method to manage system resources. To implement this feature, the PIIX4E bridge device becomes the master controller and communicates with several other devices in the system. Some of the functions the processor can monitor though the SMB bus are:

- Fan Speed
- Temperatures
- Voltage rails
- LAN controllers
- DIMM presence and size
- Clock chip enabling.

To facilitate communication with all the devices an address map has been defined in Table 43. For more information on individual devices and their respective register mapping, please see their respective datasheets.

Table 43: SMB bus ID table

Device	Master/Slave	I^2C Address
PIIX4E	Master Controller	N/A
LAN controller 1	Slave	:84
LAN controller 2	Slave	:85
PCI riser expansion connector	Slave	Undefined **
Memory DIMM 0	Slave	:50
Memory DIMM 1	Slave	:51
Memory DIMM 2	Slave	:52
Memory DIMM 3	Slave	:53
Clockchip	Slave	:D2
Heceta 2 system management chip	Slave	:2D

** Note: At the writing of this document, the PCI riser expansion board did not have an I^2C bus ID assigned.

4 PCI Riser Board

4.1 Introduction

A PCI riser board is used in the Intel® ISP1100 Internet Server system to facilitate the installation of two PCI add-in boards while installed in the 1U chassis. It provides two PCI-compatible connectors mounted in opposite directions parallel to the serverboard. The pinout of the connectors is exactly the same as a standard PCI compatible connector. To provide the additional signals needed to support the second PCI connector on the riser board, an additional 22-pin edge card connector (see Section 3.16.2.3) is installed on the serverboard. This additional connector supplies the extra power/ground, clocks, request/grant and interrupt signals needed for the second PCI connector.

4.2 PCI Riser Board Expansion Connector

This connector is provided to allow a backplane riser card to be plugged in to support two PCI connectors from a single PCI expansion slot location. Table 44 shows the pin definitions.

Table 44: PCI riser board edge connector (J3)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground	B1	CK_PCI_S3_33M	A7	SMB_CLK	B7	AD17
A2	No connect	B2	Ground	A8	+12 V	B8	Ground
A3	Ground	B3	P_REQ[1]#	A9	NC	B9	SMB_DATA
A4	No connect	B4	Ground	A10	+5 V	B10	+3.3 V
A5	Ground	B5	P_GNT[1]#	A11	+5 V	B11	+3.3 V
A6	No connect	B6	Ground				

4.3 Riser Board PCI Bus Connectors

The riser card provides two 32-bit/33MHz PCI bus connectors. Table 45 provides the pin definitions.

Table 45: Riser board PCI bus connectors (J1, J2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TRST#	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	TCK	A33	+3.3 V	B33	C/BE2#
A3	TMS	B3	Ground	A34	FRAME#	B34	Ground
A4	TDI	B4	TDO	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A9	Reserved1	B9	PRSNT1#	A40	SDONE	B40	PERR#
A10	+5 V	B10	Reserved2	A41	SBO#	B41	+3.3 V
A11	Reserved3	B11	PRSNT2#	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V AUX	B14	Reserved5	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V	B59	+5 V
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

4.4 Riser Board PCI Interrupt Routing Map

Table 46 lists the PIRQX signals and shows how the signals are connected to the PCI bus connectors.

Table 46: Riser board PCI connector interrupt routing map

PIIX4E PIRQ Signal Name	PCI Bus Connector 1	PCI Bus Connector 2
PIRQA	INTA	INTC
PIRQB	INTB	INTD
PIRQC	INTC	INTA
PIRQD	INTD	INTB

Figure 18 shows the PCI riser board.

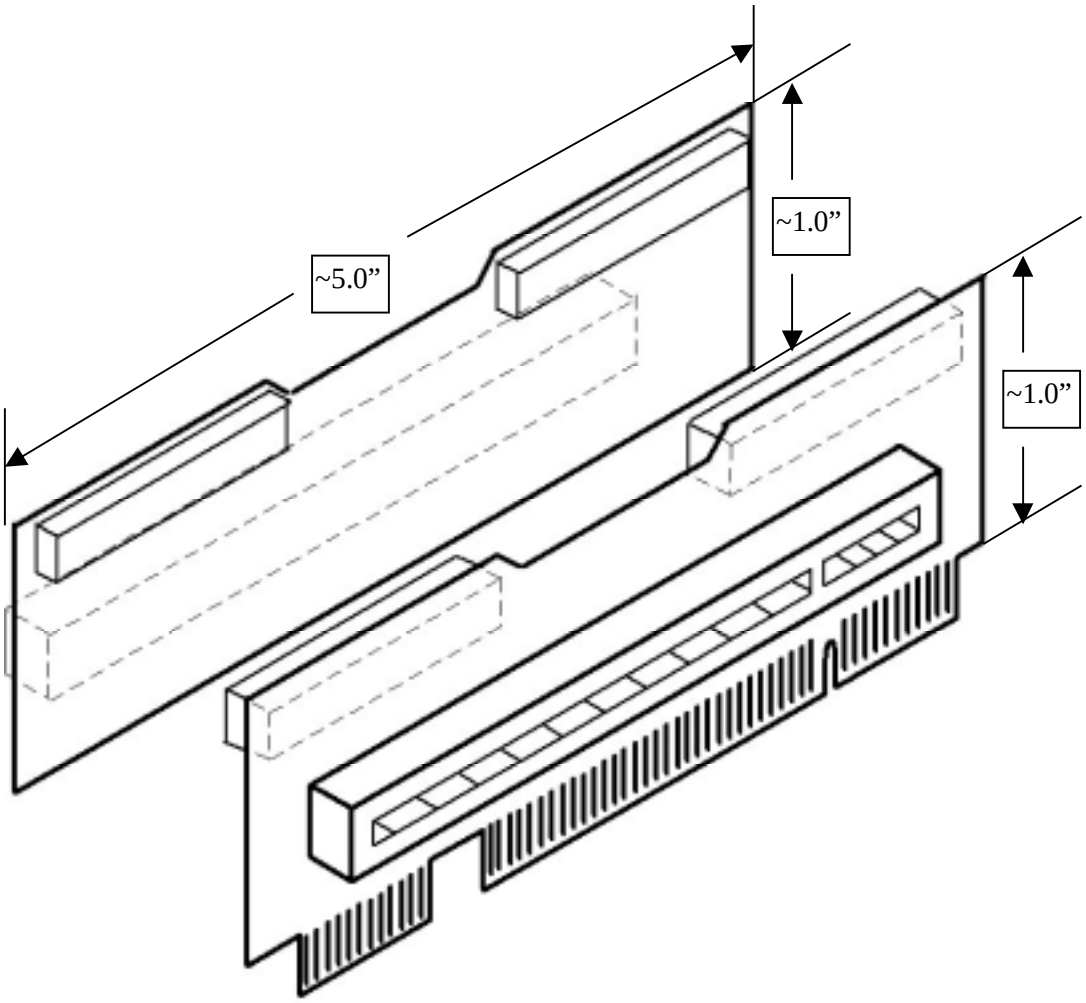


Figure 18: PCI riser board

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5 Front Panel Board

5.1 Introduction

The front panel board provides nine LED indicators, four system control switches, and serial port B. The board is connected to the TR440BX serverboard via a high-density connector.

5.2 Front Panel Switches

Figure 19 depicts the layout of the front panel board.

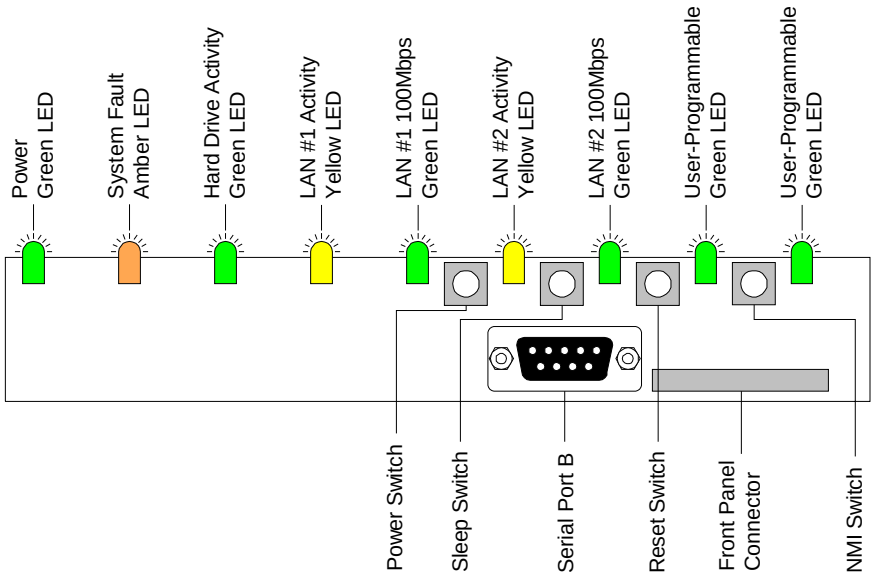

Figure 19: Front panel board

Table 47: Front panel switches

Switch	Reference Designator	Description
Power	S5	The Power switch is monitored to sense when to power on the system for normal operation. This switch is also used to turn the power off to the TR440BX serverboard. User must press and hold the switch for 4 seconds to turn power off.
Sleep	S6	This switch is used to place the TR440BX system in the sleep state.
Reset	S7	This switch is used to issue a system reset to the entire system and thus cause a reboot to occur.
NMI (PIIX4E_SERR#)	S8	This switch (when depressed) will cause an NMI to be issued to the system. It is used to dump the system state when the system is hung.

5.3 Front Panel Serial Port B Connector

Since serial port B is not populated on the TR440BX serverboard, the signals for it are routed to the serial port on the front panel. See Table 48 for signal definitions.

Table 48: Front panel serial port B connector (J2)

Pin	Signal Name	Description
1	DCD	Data Carrier Detect
2	SIN #	Serial Data In
3	SOUT #	Serial Data Out
4	DTR	Data Terminal Ready
5	Ground	Ground
6	DSR	Data Set Ready
7	RTS	Request to Send
8	CTS	Clear to Send
9	RI	Ring Indicate

5.4 Front Panel LED Indicators

Table 49 defines the LED indicators on the front panel board.

Table 49: Front panel LEDs

LED	Color	Reference Designator	Description
Power On	Green	DS1	This LED indicates if the system is powered on. A blinking green LED indicates the system is in sleep mode.
System Fault	Amber	DS2	This LED lights when the system has detected a system fault state.
Hard Disk	Green	DS3	The hard disk LED indicates when any access to the hard drive has taken place. This LED shows activity from any one of three sources: Hard Disk 1, Hard Disk 2, or an external SCSI drive that is connected to the internal SCSI activity connector (see Section 3.16.2.1).
LAN #1 Activity/Link	Yellow	DS4	This LED lights when a successful 10/100Mb link has occurred to an Ethernet port. Once the LED is lit, it blinks at a variable rate to indicate network activity on this channel.
LAN #1 Speed	Green	DS5	This LED lights when the LAN #1 controller has detected and is configured to run at 100 Mbps operation. For 10 Mbps operation, the LED will not light.
LAN #2 Activity/Link	Yellow	DS6	This LED lights when a successful 10/100Mb link has occurred to an Ethernet port. Once the LED is lit, it blinks at a variable rate to indicate network activity on this channel.
LAN #2 Speed	Green	DS7	This LED lights when the LAN #2 controller has detected and is configured to run at 100 Mbps operation. For 10 Mbps operation, the LED will not light.
User Prog1	Green	DS8	This LED lights when a user-defined event has occurred and an appropriate software driver must be installed for this event to take place. If not programmed, the LED will not light even if an event takes place.
User Prog2	Green	DS9	This LED lights when a user-defined event has occurred and an appropriate software driver must be installed for this event to take place. If not programmed, the LED will not light even if an event takes place.

NOTE

The following are the conditions under which the BIOS will currently set the system fault LED(solid on, not blinking) : PCI SERR errors, Multi-bit errors, Single-bit errors and all POST errors.

5.5 Front Panel I/O Connector

The front panel board is connected to the TR440BX serverboard through a high-density connector for I/O information. Table 50 shows the signal definitions.

Table 50: Front panel I/O connector (J3)

Pin	Signal Name	Pin	Signal Name
1	GND	2	+5V Power
3	D1	4	D0
5	D2	6	GND
7	D3	8	D4
9	D5	10	GND
11	D6	12	D7
13	GND	14	Reserved
15	Reserved	16	Reserved
17	DSR2	18	Reserved
19	CS2	20	FP_TYPE_BIT1
21	CS1	22	RI2
23	LED_GREEN_BLINK	24	Reserved
25	LED_YELLOW_BLINK	26	Reserved
27	LED_HDD	28	RESET_SW#
29	+5V Standby Power	30	POWERON_SW#
31	+3.3V	32	THERM_TRIP#
33	SLEEP_SWITCH#	34	NMI
35	Reserved	36	Reserved
37	LAN1_ACTLED	38	LAN2_ACTLED
39	LAN1_LINKLED	40	LAN2_LINKLED
41	LAN1_SPEEDLED	42	LAN2_SPEEDLED
43	PROG_LED1	44	PROG_LED2
45	SIN2#	46	SOUT2#
47	RTS2	48	CTS2
49	DTR2	50	DCD2

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6 BIOS Description

6.1 Overview

The TR440BX serverboard uses an Intel/AMI BIOS, which is stored in Flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the Flash memory contains the Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

This serverboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as TR440BXA.86B.00xx.P01.

The term "BIOS," as used in the context of this document, refers to the following:

- System BIOS, that controls basic system functionality using stored configuration values.
- Configuration Utilities (CU) consisting of a Flash ROM-resident Setup utility that provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update Utility (IFLASH.EXE) that loads predefined areas of Flash ROM with Setup, BIOS, and other code/data.

Each of these is introduced here, with references to the appropriate section for details. A summary of memory maps for Flash, and CMOS configuration RAM and NVRAM register spaces (which provide the operating environment for BIOS code) is also presented.

6.1.1 System BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services. In addition, the system BIOS provides support for these TR440BX specific features:

- Security features
- Multiple-speed processor support
- Logging of critical events
- CMOS configuration ram defaults
- Defective DIMM detection and remapping
- PCI BIOS interface
- Option ROM shadowing
- ECC support
- SMI support
- L2 cache support
- Memory sizing
- Boot drive sequencing
- Resource allocation support

6.1.2 Configuration Utility

The CU provides the means to configure on-board hardware devices and add-in cards. The CU consists of the standard PC-AT Setup utility (a.k.a. Setup), embedded in Flash ROM, for configuration of on-board resources.

6.1.3 CMOS Configuration RAM Summary

The PIIX4E chip on the serverboard contains battery-backed CMOS memory for system hardware setup parameters.

6.1.4 Flash Memory Update Utility

The system BIOS is resident in partitioned Flash ROM. The device is in-circuit reprogrammable, except for the recovery boot block, which is electrically protected from erasure.

To reload Flash memory, use a Flash update utility. The file to be loaded contains a new copy of BIOS code. The utility must match the board ID with the one in the load file to protect against reprogramming the Flash with BIOS for another platform. For more information, see Section 7 for information on the Flash memory update utility.

6.1.5 System Flash ROM Layout

The Flash ROM contains system initialization routines and runtime support routines. The exact layout is subject to change, as determined by Intel. All areas are 64 KB in size (symmetric flash). The complete ROM is visible, starting at physical address 4 GB less 1 MB. The Flash Memory Update utility loads BIOS components to blocks of specified length and location. None of the blocks are visible at the aliased addresses below 1 MB due to shadowing. The BIOS alone needs to know the exact Flash map. Intel reserves the right to change the Flash map without notice. All blocks in this flash part are 64k (10000h) in length. The BIOS will adjust the size of each component to fit in a given block. The Flash part used in TR440BX is the Intel® E28F008S585.

6.2 System BIOS

This section describes features of the system BIOS that are unique to TR440BX. For a complete specification of standard PC-BIOS functions, see Section 13.2 for information about the AMBIOS 98 specification. The following groups of system BIOS features are described here:

- Security features
- Auto-configuration features
- Performance features
- System services
- Boot options
- OEM customization hooks
- SMBIOS support
- Soft power switch
- POST memory manager support
- ACPI support

6.2.1 Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the system. A supervisor password and a user password can be set for the BIOS Setup program and for booting the system, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all Setup options in the BIOS Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the system. The password prompt will be displayed before the system is booted. If only the supervisor password is set, the system boots without asking for a password. If both passwords are set, the user can enter either password to boot the system.

Table 51 shows the effects of setting the supervisor password and user password.

Table 51: Supervisor and user password functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options*	Can change all options*	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor password	Supervisor	None
User only		Can change all options	Enter password Clear user password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor password Enter password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

6.2.2 Auto-Configuration Features

The BIOS provides support for auto-configuration of:

- Plug and Play
- Memory sizing
- Boot device selection
- Processor microcode update API
- Processor clock ratio settings and CMOS clear

6.2.2.1 Plug and Play

The BIOS supports the following industry standards for full Plug and Play capabilities:

- Plug and Play (PnP) ISA specification
- System Management BIOS Reference Specification
- PCI Local Bus specification

See Section 13.2 for information about these specifications.

6.2.2.1.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. Devices required for early console redirection
2. ISA devices
3. Off-board PCI devices
4. On-board PCI devices

6.2.2.1.2 Early Device Auto-Configuration

The BIOS performs early initialization of the serial ports and on-board LAN controllers for console redirection. This initialization must occur before initialization of the video controller so that all POST information may be redirected to a remote user.

6.2.2.1.3 PnP ISA Auto-Configuration

The BIOS:

- Fully supports the PnP ISA protocol.
- Reads the PnP ISA configuration port.
- Assigns the system I/O, memory, DMA channels, and IRQs from the resource pool. The Super I/O* chip is an example of a PnP ISA device.

6.2.2.1.4 PCI Auto-Configuration

The BIOS supports the INT 1Ah, AH = B1h functions in conformance with the PCI specification, Rev. 2.1. It also supports the 16 and 32-bit protected mode interfaces as required by the PCI BIOS specification. System POST performs auto-detection and auto-configuration of ISA, ISA Plug-N-Play, and PCI devices. This process maps each device into memory and/or I/O space and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. The BIOS scans the PCI devices on each PCI bus in low to high sequence. The PCI buses are also scanned in the same order. The BIOS programs the PCI-ISA interrupt routing logic in the PIIX4E to steer PCI interrupts to compatible ISA IRQs.

Drivers and OS programs can determine the installed devices and their assigned resources using the BIOS interface functions. The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to architectural limitation.

6.2.2.1.5 On-board Device Auto-Configuration

The BIOS detects all on-board devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the on board devices to DOS compatibility hole (C0000h to DFFFFh) and transfers control to the entry point.

6.2.2.2 Memory Sizing

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

TR440BX supports various sizes and configurations of ECC SDRAM DIMMs. Memory sizing and configuration are only guaranteed for qualified DIMMs. The BIOS gathers all type, size, speed and memory attributes from the on-board EEPROM or SPD on the memory DIMM. It is not required that the memory be stuffed from the lowest DIMM socket to the highest for the memory to work in all configurations over the full environmental range of the server.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS reads the DIMM speed information and programs the PAC accordingly. The BIOS always initializes ECC memory. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 1024 MB. The BIOS is capable of reporting up to 64 MB using INT 15h, AH = 88h, or 4096 MB using INT 15h, function E801h. INT 15h, function E820h supports reporting of the system memory regions. See Section 6.2.5 for other non-standard INT 15h functions supported by the system BIOS.

6.2.2.3 Boot Device Selection

The BIOS adheres to the *BIOS Boot Specification* (BBS). See Section 13.2 for information about this specification. A boot device other than the one specified by the BBS may be selected during recovery from boot failures.

6.2.2.4 Processor Microcode Update API

The Intel® Celeron™ and Pentium® III processors have the capability to correct specific errata through the loading of an Intel supplied data block. The *Pentium® Pro Processor BIOS Update Specification* defines a way of incorporating future releases of such a data block (also called the "update") into a system BIOS. The BIOS is responsible for storing the update in a non-volatile memory block and loading it into the Celeron® or Pentium® III processor during POST sequence. The Pentium® Pro processor BIOS update specification requires the system BIOS to implement function calls to read the update and overwrite the existing update with a new release. These functions can be accessed from real mode by executing INT 15 with AX=0xD042. The corresponding 16-bit protected mode interface is not implemented. The BIOS performs all the recommended security checks before validating an update. See Section 13.2 for information about the *Pentium® Pro Processor BIOS Writer's Guide*.

6.2.2.5 Processor Clock Ratio Settings and CMOS Clear

TR440BX will support all indicated speeds of the Intel® Celeron™ and Pentium® III processors listed in Table 12. Processor speeds and, therefore, clock ratios are hard-coded within the processor and no jumpers are required.

6.2.3 Performance Features

For enhanced performance, the BIOS sets up the L2 cache controller for the Celeron™ or Pentium® III processor and performs option ROM shadowing.

6.2.3.1 L2 cache Initialization

There are differences between the Celeron™ and Pentium® III processor cache implementation and previous Intel processor architectures. To boost system performance, the processor contains an L2 cache and cache controller, which previously had been handled by external devices. The BIOS programs the processor's L2 cache controller in a manner that is consistent with the PCIset.

L2 cache is tested as a part of the processor BIST. The BIOS detects the cache size and cache type (ECC or non-ECC), and programs the cache controller accordingly before performing any cache operations. Table 52 describes the default values loaded in the MTR registers.

Table 52: Memory type range register table

Offset	Name	Description	Default
0FEh	MTRRCAP	Capability MSR, RO: VCNT, FIX, USWC	0508h
200h	MTRRphysBase0	Physical Address Base 0	00006h
201h	MTRRphysMask0	Physical Address Mask 0	00FFE000800h
202h	MTRRphysBase1	Physical Address Base 1	0000h
203h	MTRRphysMask1	Physical Address Mask 1	0000h
204h	MTRRphysBase2	Physical Address Base 2	0000h
205h	MTRRphysMask2	Physical Address Mask 2	0000h
206h	MTRRphysBase3	Physical Address Base 3	0000h
207h	MTRRphysMask3	Physical Address Mask 3	0000h
208h	MTRRphysBase4	Physical Address Base 4	0000h
209h	MTRRphysMask4	Physical Address Mask 4	0000h
20Ah	MTRRphysBase5	Physical Address Base 5	0000h
20Bh	MTRRphysMask5	Physical Address Mask 5	0000h
20Ch	MTRRphysBase6	Physical Address Base 6	0000h
20Dh	MTRRphysMask6	Physical Address Mask 6	0000h
20Eh	MTRRphysBase7	Physical Address Base 7	0000h
20Fh	MTRRphysMask7	Physical Address Mask 7	0000h
250h	MTRRfix64k_00000	Fixed range for 00h - 7Fh segment in 64KB block	0606060606060606h
258h	MTRRfix16k_80000	Fixed range for 80h - 9Fh segment in 16KB block	0606060606060606h
259h	MTRRfix16k_A0000	Fixed range for A0h - BFh segment in 16KB block	0000h
268h	MTRRfix4k_C0000	Fixed range for C0h segment in 4KB block	0000h
269h	MTRRfix4k_C8000	Fixed range for C8h segment in 4KB block	0000h
26Ah	MTRRfix4k_D0000	Fixed range for D0h segment in 4KB block	0000h
26Bh	MTRRfix4k_D8000	Fixed range for D8h segment in 4KB block	0000h
26Ch	MTRRfix4k_E0000	Fixed range for E0h segment in 4KB block	0000h
26Dh	MTRRfix4k_E8000	Fixed range for E8h segment in 4KB block	0000h
26Eh	MTRRfix4k_F0000	Fixed range for F0h segment in 4KB block	0505050505050505h
26Fh	MTRRfix4k_F8000	Fixed range for F8h segment in 4KB block	0505050505050505h
2FFh	MTRRdefType	Default memory type and global enable flags	00C00h

6.2.3.1.1 Cache State on Boot

The BIOS looks at a bit in CMOS to determine if the system cache should be enabled or disabled. If the cache is enabled, the cache controller in the processor is initialized in a consistent manner with the PCISet.

6.2.3.2 Option ROM Shadowing

All on-board adapter ROMs (stored in compressed form in the system Flash ROM), and PCI adapter ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to DFFFFh. PCI BIOS ROMs are always shadowed. Typically, the video BIOS is shadowed at C0000h if a video controller is present.

6.2.3.3 Memory Speed Optimization

The BIOS detects the system memory speed and bus speed and optimizes the memory controller for the best performance.

The system bus speed can be determined by using the processor internal speed and the bus ratio. The memory DIMM speed can be determined using its ID. Using this information the BIOS can set up the memory controller register for the best performance.

6.2.3.4 PCIset Performance Optimization

The BIOS detects the system configuration (such as board ID, PCIset stepping, and processor stepping) and optimizes the PCIset for the best performance.

6.2.4 Reliability Features

The BIOS supports several features to create a robust computing environment including:

- ECC memory and defective DIMM handling
- Logging of critical events
- CMOS default override

Also see Section 8 for more information on error handling and critical event logging.

6.2.4.1 Defective DIMM Detection and Remapping

The ECC memory subsystem on TR440BX is able to detect SBEs and certain multi-bit errors (MBE) during reads from and writes to system DRAM. SBEs can be detected and corrected. Certain patterns of MBEs can be detected but cannot be corrected, whereas other types of MBEs cannot be detected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled. Any error is avoided by reducing the usable memory in that bank so the byte containing the hard error is no longer accessible. This is done automatically by the BIOS during POST and does not require any user intervention. The BIOS logs the errors in the nonvolatile system event log. The BIOS detects the speed of individual DIMMs. The BIOS disables a DIMM that is slower than what the hardware requires and displays a warning message.

6.2.4.1.1 Memory Configuration Algorithm

The algorithm for determining memory configuration is:

> If there is no DIMM population, or the DIMMs are defective, or have the wrong speed, the BIOS sounds a beep code error and POST is terminated (see Section 8.5 for beep codes and error messages). The BIOS requires at least 4 MB of good memory for POST to start up. The BIOS individually probes each bank for the size of installed DIMMs. The BIOS detects the speed and type of the DIMM

SDRAM and programs the PCIset accordingly. If the bank does not match one of the allowable configurations, the BIOS reports the error with an error message. EDO memory is not physically supported due to the memory socket used on the serverboard. The BIOS will automatically shut off all ECC capability for the system if non-ECC memory is detected. All configuration data for the memory DIMMs is gathered by the BIOS from the SPD or EEPROM on the DIMM. This is done via the SMBUS interface on the PIIX4E.

In the event that the BIOS disables or resizes a bank, an error message is displayed with the number of the failed memory. Another message informs the user that the amount of usable memory in that bank is being reduced to eliminate the failing location. Eliminating hard errors in this way during POST is done as a precaution to prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed. This is recorded in the SEL (System Event Log) at both POST time as well as runtime with an SMI.

If the error is an SBE, the 440BX automatically corrects the data before it is returned to memory. The 440BX memory controller scrubs the memory location where the error occurred to correct the SBE, and the BIOS will record the SBE via an SMI to the SEL. If the error is an MBE this condition is considered fatal, and after the error is logged an NMI is generated telling the OS to handle this fatal error.

6.2.4.1.2 ECC Memory Initialization

The system BIOS handles ECC memory initialization. All memory locations, including System Management RAM and shadow memory region, are unconditionally initialized during POST (set to 0). Error detection is disabled while ECC memory is initialized to prevent false alarms caused by un-initialized memory bytes. If hard errors are detected during the memory test, the memory partition containing the errors is resized to eliminate the failing locations.

6.2.4.1.3 ECC and SMI Support

During normal operation, any SBEs are detected and are handled by the SMI support code. The SMI code logs the SBE to the system event log. Scrubbing is always automatically enabled when ECC memory is detected. The row containing the failing location is scrubbed by reading the corrected data and writing back the correct data automatically by the memory controller. If a read from shadow memory results in a SBE, the BIOS must enable writes to that area, scrub the location, and disable writes. Scrubbing helps to prevent a single-bit correctable error from turning into multiple-bit errors in the future. Scrubbing an entire row is a time consuming operation and might affect correct functioning of certain operating systems. If MBEs are detected, the BIOS SMI handler will log an event into the SEL and then generate an NMI to the OS.

For more information on SMI handlers, see Section 8.3.3.

6.2.4.2 Logging System Events

The BIOS can log critical and informational events to nonvolatile memory. This area is managed by the BIOS and can be accessed by an OS NVRAM driver. A critical event is one that might result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory

subsystem are considered critical errors, as are most errors that traditionally generate a Non-Maskable Interrupt (NMI). On TR440BX, these errors are first routed to System Management Interrupt (SMI). These errors include I/O channel check, software generated NMI, and PCI SERR and PERR events. For details on error handling, see Section 8.4.

During POST, the BIOS initializes System Management RAM (SMRAM) with error handling and logging code. The processor has a private area of SMRAM dedicated to it for SMI processing. The DRAM controller and PIIX4E are programmed to generate an SMI for PCI SERR and PERR, software generated NMI, I/O channel check, and ISA watchdog time-out and NMIs generated by the PAC. The PAC generates an SERR if parity/ECC errors are observed in the memory subsystem. The PAC generates an interrupt if a single-bit correctable error is observed in the memory subsystem. The PIIX4E can be programmed to generate an SMI on this interrupt. When these errors are detected, the SMI routines log the error or event in a manner that is transparent to the OS and then causes an NMI to be generated for certain events, so that the OS can respond appropriately. The BIOS also logs an event on another type of memory error called Single Bit Error (SBE). For this error, the BIOS will not generate an NMI to the OS.

For more information about handling and logging system errors, see Section 8.4.

6.2.5 System Services

The BIOS provides an interface, using the software interrupt 15h, to report system configuration information to application programs or the OS. The following functions are provided by the BIOS in addition to the IBM AT standard INT 15h functions:

Table 53: System information (INT15h) functions

Function (AX)	Description
DA12h	New cache services
DA8Ch	Get version information
DA92h	Processor information

The following sections describe each function, showing the values in processor registers on call and return.

6.2.5.1 New Cache Services

Call With:

```
AH = DAh
AL = 12h
CL = 0          Disable Cache
   = 1          Enable Cache
   = 2          Read Cache Status
   = 3          Set Writeback Mode
   = 4          Set Write-through Mode
```

Returns:

```
AH = bit 0 = 0      Cache Disabled
           = 1      Cache Enabled
     bit 1 = 0      Write-through Mode
           = 1      Writeback Mode
CX = bit 15 =       Size Information valid flag
     bits 14::0 =   Size of L2 cache in 32KB blocks
CF = 1, AH = 86h    Function not supported
```

NOTE

The TR440BX does not support switching from writeback to write-through modes during runtime. This function is not supported if the processor is not in real mode.

6.2.5.2 Get Version Info

Call With:

```
AH = DAh
AL = 8Ch
CL = 0h         Get BIOS Version
ES =            Segment for Data Buffer (32 bytes)
DI =            Offset for Data Buffer
```

Returns:

```
CL = 3          To indicate AMIBIOS ID version 3 format32 byte ID
                includes:
                3-7 byte board ID, 'TR440BX'
                1 byte board revision, starting from '0'
                3 byte OEM ID, '86B' for standard BIOS
                4 byte build number
                1-3 byte describing build type (D for development, A for
                    Alpha, B for Beta, Pxx for production version xx)
                6 byte build date in mmddyy format
                4 byte build time in hhmm format
                5 bytes reserved for future use

In case of an error:    Invalid parameters
CF = 1                  Function Not Supported
AH = 86h
```

NOTE

The call "Get PCIset Version" is now obsolete.

6.2.5.3 Processor Info

Call With:

```
AH = DAh
AL = 92h
CL = 0
```

Returns:

```
AL =                    Stepping ID
AH =                    Model
BL =                    Family
CX =                    Processor bus speed in BCD (MHz)
DX =                    Processor core speed in BCD (MHz)

In case of error:
CF = 1

If function not
supported:
AH = 86h
CF = 1
```

NOTE

This call is enhanced to report the processor core speed and the maximum number of processors in the system. The way processors are numbered is also changed.

6.2.6 Boot Options

The TR440BX BIOS conforms to the BIOS Boot Specification (BBS). There are several additional BIOS features not described in the BBS, which pertain to booting. These are described in the following sections.

6.2.6.1 Quiet Boot

The BIOS includes a default Intel logo that can optionally be displayed during BIOS POST in lieu of the POST diagnostic screen. If the Quiet Boot feature is disabled via BIOS setup, during POST the BIOS displays the usual POST screen including the memory count and processor information. If Quiet Boot is enabled and a valid logo is detected, the BIOS displays the logo during POST and suppresses the usual POST screen. The user may press the <ESC> key to switch to the POST diagnostic screen from the logo. The OEM splash screen implementation follows the guidelines specified in PC99 System Design Guide. See Section 13.2 for information about this specification.

While the splash logo is displayed, the video is in graphics mode. OEMs can customize the logo (see Section 6.2.7.3).

6.2.6.2 PXE Boot

The TR440BX BIOS provides network boot support as described in the *Preboot Execution Environment (PXE) Specification*, ver 1.0 and the *Preboot Execution Environment BIOS Support Specification*, ver 1.1. This feature works within the standard framework of the BBS support. See Section 13.2 for information about this specification.

6.2.6.3 Ultra DMA IDE Support

The TR440BX BIOS provides Ultra DMA IDE support. This feature may be disabled via BIOS setup.

6.2.7 OEM Customization

OEMs can customize the BIOS for product differentiation. The extent of customization is limited to what is stated in this section. OEMs can change the BIOS look and feel and manage OEM-specific hardware, if any, by executing their own code during the POST sequence. OEMs can modify the contents of the message strings and supported languages by translating Intel supplied strings into the desired language. The code in a user binary may not hook critical interrupts, reprogram the PCIset, or take any action that affects the correct functioning of the system BIOS.

6.2.7.1 User-supplied BIOS Code Support

A 64KB region of Flash ROM is available to store the User Binary. Using the IFLASH utility, this region can be updated with OEM supplied code and data – a User Binary. At several points throughout POST (see Table 54) control is passed to this User Binary.

The User Binary must adhere to the following requirements:

1. In order to be recognized by the BIOS and protected from runtime memory managers, the User Binary must have an Option ROM header (55AA, size).
2. The system BIOS performs a scan of the User Binary Area at predefined points during POST. Mask bits must be set within the User Binary that inform the BIOS if an entry point exists for a given time during POST.
3. System state must be preserved by the User Binary.
4. User Binary code must be relocatable. It will be located within the first Megabyte. The User Binary code should not make any assumptions about the value of the code segment.
5. User Binary code will always be executed from RAM and never from flash.

The BIOS copies the User Binary into system memory before the first scan point. If the User Binary reports that it does not contain runtime code, it is located in conventional memory (0-640k) saving limited option ROM space. If User Binary code is required at runtime, it is copied to option ROM space. At each scan point during POST, the system BIOS will determine if this scan point has a corresponding User Binary entry point to transfer control to. To determine this, the bitmap at byte 4 of the header is tested against the current mask bit (which has been determined/defined by the scan point). If the bitmap has the appropriate bit set, the mask is placed in AL and execution is passed to the address computed by (ADR(Byte 5)+5*scan sequence #).

During execution, the User Binary may access 11 bytes of Extended BIOS Data Area RAM (EBDA). The segment of the EBDA can be found at address 40:0e. Offset 18 to offset 21h is available for the User Binary. The BIOS also reserves four CMOS bits for the User Binary. These bits are in a non-checksummed region of CMOS with default values of zero. These bits will be contiguous, but are not in a fixed location. Upon entry into the User Binary, the DX register will contain a ‘token’ that points to the reserved bits. This token is of the following format:

MSB LSB

15	…	12	11	…	0
# of bits available - 1			Bit offset from start of CMOS of first bit		

The most significant 4 bits will be equal to the number of CMOS bits available minus 1. This field will be equal to 3 since there are four CMOS bits available. The 12 least significant bits will define the position of the CMOS bit in the RTC (Real Time Clock). This will be a bit address rather than a byte address. The CMOS byte location is 1/8th of the 12-bit number, and the remainder will be the starting bit position within that byte. For example, if the 12-bit number is 0109h, user binary can use bit 1 of CMOS byte 0108h/8, or 021h.

The following code fragment shows the header and format for a User Binary:

```
.286
                db  55h,0AAh,10h   ; USER binary signature is 55h,AAh
                                   ; 10h = size of user binary area
                                   ; 8k = 10h*512 bytes
MyCode          PROC    FAR        ; MUST be a FAR procedure

;***  Use for normal CU controllable user binaries
;
;               RETF               ; Signal to BIOS that what follows
                                   ; is a standard user binary
                                   ; that will be used if the Scan User
                                   ; Flash CU selection is enabled.
;***
;***            Use for Mandatory user binaries
;
;               db  0CBh           ; Signal to BIOS that what follows
                                   ; is a user binary that
;***
                db  04h            ; Bit map to define call points, a
                                   ; one in any bit specifies that the
                                   ; BIOS will be called at that scan
                                   ; point in POST (scan points to be
                                   ; defined
;*** jump table for each scan point

                JMP scanpoint_01h  ; follows a list of 8 transfer
                JMP scanpoint_02h  ; addresses, one for each bit in the
                JMP scanpoint_04h  ; bitmap. In all likelihood, only
                JMP scanpoint_08h  ; one of these will be used, earlier
                JMP scanpoint_10h  ; entries must be present, later can
                JMP scanpoint_20h  ; be omitted if desired.
                JMP scanpoint_40h
                JMP scanpoint_80h

;* it is extremely important that this table's assembled code appears
;* as a jump table in real mode (jmps must be e9 xx 00 00) for each entry.
;* some assemblers will change the jmp to eb xx yy 00 00 or do a long
;* jump eb xx yy 00 00 00 00 which will create incorrect offsets. That is
;* why the .286 directive was used with masm 6.11.  .586p is used to insert
;* instructions that do not appear in the 286 instruction set and to maintain
;* the offsets in the table.

; In this example since the mask is defined as 04h only scanpoint_04h
; will be executed during post. This happens to occur just before video
; initialization. If the mask were 0Ch. Both scanpoint_04h and
```

```
; scanpoint_08h would be executed during post.
```

6.2.7.1.1 Scan Point Definitions

Table 54 defines the bitmap for each scan point, indicating when the scan point occurs and which resources are available (RAM, Stack, Binary Data Area, Video, Keyboard).

Table 54: User binary area scan point definitions

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
Near pointer to the User Binary extension structure: Mask bit is 0 if this structure is not present. Instead of a jump instruction the scan address (offset 5) contains a 0CB followed by a near pointer.	01h	Not applicable	Not applicable
If SMM is enabled in CU, the system BIOS copies the User Binary code into SMRAM. The part of the User Binary that is executed on SMI will be executed in SMRAM. The SMI handler will not make far calls because of security concerns. The User Binary can be used to handle OEM-specific SMI events that a standard SMI handler does not know about. This is done in order to minimize the SMI latency. This scan only occurs as a result of an SMI (during SMM). This routine is executed after all other SMI detection routines if the standard detection routines cannot handle the SMI.	02h	A stack is assured. In addition, the part of SMRAM that User Binary is copied to can be used for storing data. A User Binary implementation can reserve some bytes for data storage. These locations can only be written to while in SMM. Remember, this is SMRAM and only accessible when in SMM. It will persist between SMM invocations (but not across resets or power-downs). The processor is in real mode at this point.	Video memory and INT 10h services are not accessible since SMRAM is mapped on top of where video RAM usually is. Keyboard services are not available through BIOS, although port accesses to the keyboard are possible. All the restrictions that are placed on SMM code apply.
This scan occurs immediately after video initialization.	04h	Yes	Yes
This scan occurs immediately before video initialization	08h	Yes	No
This scan occurs on POST error. On entry, BX register contains the number of the POST error	10h	Yes	Yes
This final scan occurs immediately before the INT 19 for normal boot and allows you to completely circumvent the normal INT 19 boot if desired.	20h	Yes	Yes
This scan occurs immediately before the normal external ROM scan. This is just before boot, but prior to the scan for external ROMs and the scan for conventional BIOS in User Binary.	40h	Yes	Yes
This scan occurs immediately after the “normal” User Binary area scan.	80h	Yes	Yes

Table 55: Format of the user binary information structure

Offset	Bit Definition
0	Bit 0 = 1 if mandatory User Binary, = 0 if not mandatory Bit 1 = 1 if runtime presence required (other than SMM user binary portion, SMM user binary will always be present in runtime irrespective of setting of this bit), = 0, if not required in runtime, and can be discarded at boot time. Bit 7:2 - reserved for future expansion
1 - 0fh	Reserved for future expansion

If this structure is not present, that is, the mask bit 01 is not set, the system BIOS assumes that the user binary is not mandatory, and it is required in runtime.

6.2.7.2 Multiple Language Support

The BIOS supports five languages at a time. IFLASH is used to load language support that replaces the text strings for POST and general error messages with text strings translated into a particular language.

Intel provides specifications for all BIOS text strings, so that any OEM can have them translated and prepared for updating with IFLASH. By default, the BIOS provides language support for English, Spanish, French, German, and Italian. The language can be selected using the CU.

6.2.7.3 OEM Logo Screen

A 16 KB region of Flash ROM is available to store the OEM logo in compressed format. The BIOS will contain the standard Intel logo. Using the IFLASH utility, this region can be updated with an OEM-supplied logo image. This utility will compress and convert a 16-color bitmap file into a logo file suitable for IFLASH. See section 6.2.6.1 for details on how the logo works.

6.2.8 SMBIOS Support

System management BIOS (SMBIOS) is a method of managing computers in an enterprise. The main component of SMBIOS is the Management Information Format Database, or MIF. This database contains all the information about the computing system and its components. Using SMBIOS, a system administrator can obtain the types, capabilities, operational status, installation date, and other information about the system components.

The *System Management BIOS Reference Specification* and its companion *DMTF Systems Standard Groups Definition* define "manageable attributes that are expected to be supported by SMBIOS-enabled computer systems." Many of these attributes have no standard interface to the management software, but are known by the system BIOS. The *System Management BIOS Reference Specification* provides this interface via data structures through which the system attributes are reported. There are two access methods defined for the SMBIOS structures; one or both methods can be used in an SMBIOS-compliant BIOS. The first method, defined in v2.0 of this specification, provides the SMBIOS structures through a Plug-and-Play function interface. A table-based method, defined in v2.1 of this specification, provides the SMBIOS structures as a packed list of data referenced by a table entry point. Using SMBIOS, a system administrator can obtain

the types, capabilities, operational status, installation date, and other information about the system components. Plug and Play functions 50h-5Fh are assigned for SMBIOS interface. Each of the SMBIOS Plug and Play functions are available both in real-mode and 16-bit protected mode. General Purpose Nonvolatile (GPNV) interface as defined in the SMBIOS specification, Revision 2.3 will be provided. The TR440BX BIOS supports GPNV areas as required by manufacturing.

The table convention, provided as an addition or alternative to the calling interface, allows the SMBIOS structures to also be accessed under 32-bit protected-mode operating systems such as Microsoft Windows® NT. This convention provides a searchable entry-point structure that contains a pointer to the packed SMBIOS structures residing somewhere in 32-bit physical address space. Please refer to the *System Management BIOS Reference Specification* for details.

The SMBIOS structure entry types currently supported in TR440BX are:

- BIOS information (Type 0)
- System information (Type 1)
- Serverboard information (Type 2)
- System enclosure/chassis (Type 3)
- Processor information (Type 4)
- Memory controller information (Type 5)
- Memory module information (Type 6)
- Cache information (Type 7)
- Port connector information (Type 8)
- System slots (Type 9)
- On-board devices information (Type A)
- System configuration options (Type C)
- BIOS language information (Type D)
- System event log (Type F)

See Section 13.2 for more information about these specifications.

6.2.9 Soft Power Switch

The power button in the TR440BX design is now a request to the power state machine in the PIIX4E. It does not directly control power on the power supply.

Off to On: PIIX4E monitors the power button and turns the system on. The BIOS is not running so it does not participate. PIIX4E receives good power and resets to get into the ON state. PIIX4E may be set up for several different events to turn on the system: Wake on LAN and Wake on Ring.

On to Off: PIIX4E generates an SMI. The BIOS will service this SMI and set the state machine in the PIIX4E to the off state. As a safety mechanism, the PIIX4E will automatically power the system off if the BIOS fails to service the SMI after 4 seconds. It will also power the system off if the power button is pressed and held for 4 seconds. During power-up of the system the SMI handler to service the power button is not loaded until SMI is initialized. The SMI handler only sets the state machine in PIIX4E to the off

state if the OS is not yet running. Once the OS is running, the SMI handler leaves the machine running and allows the OS to handle the power state.

6.2.10 POST Memory Manager Support

The BIOS supports revision 1.0 of the POST Memory Manager (PMM) specification. This specification allows external clients, such as option ROMs, to request memory buffer during initialization and release it later. Without the PMM, the option ROMs may overwrite buffers used by the system BIOS or another client. Check with your plug-in card vendor to make sure that their PCI or ISA option ROM is PMM compliant. Being PMM compliant insures that the plug in cards will not cause system hangs or memory conflicts during post initialization of Option ROMs.

6.2.11 ACPI Support

The TR440BX BIOS supports the *Advanced Configuration and Power Interface Specification*, Revision 1.0. The primary role of the ACPI BIOS is to supply the ACPI Tables. POST initializes the ACPI tables and relocates them to extended memory. INT 15h, function E820 reports memory, which is used by the ACPI BIOS as reserved. An ACPI aware OS causes an SMI if the system is to be switched into ACPI mode. The system returns to legacy mode on hard reset or power-on reset.

There are three runtime components to ACPI:

- ACPI Tables - These tables describe the interfaces to the hardware. ACPI Tables can make use of a p-code type of language, the interpretation of which is performed by the OS. That is, the OS contains and uses an AML interpreter that executes procedures encoded in AML and stored in the ACPI tables; ACPI Machine Language (AML) is a compact, tokenized, abstract kind of machine language. The tables contain information about power management capabilities of the system, APIC information, and bus structure. The tables also describe control methods that operating system uses to change PCI interrupt routing, enable/disable devices in Super I/O, and find out the cause of the wake event.
- ACPI Registers - The constrained part of the hardware interface, described (at least in location) by the ACPI Tables.
- ACPI BIOS - The code that boots the machine and implements interfaces for sleep, wake, and some restart operations. The ACPI Description Tables are also provided by the ACPI BIOS.

The TR440BX platform supports states S0, S1, S4 and S5. Different sleep states are defined in the ACPI specification. While entering S4 state, the operating system saves the context to the disk and most of the system is powered off. The system can wake up from such a state on front panel input, or a magic packet received by a Wake on LAN compliant LAN card, modem ring or RTC alarm. The BIOS performs complete POST upon wake up from S4, and initializes the platform. The BIOS is not responsible for enabling Wake on LAN functionality in add-in cards. The WOL enable bit is typically located in the EEPROM on the network card, and the user needs to use the configuration utilities that are shipped with the network card to set up the card in the correct mode. The RTC alarm is setup in the standard CMOS locations from 0 to 0Ch of the RTC ram. Wakeup can be setup for any time during 24 hours.

S1: The BIOS will set up the ACPI tables for CPU sleep halt capability only. No context will be lost in this state and the CPU caches will maintain coherency.

S4: Hibernate or Save to disk. The BIOS will set up the ACPI tables and AML code to store memory and the machine state to disk. All context is saved to the disk before the system reverts to the soft off state (S5). Upon a power button press or wakeup event the system will restore from disk and resume. This assumes that no hardware changes have been made to the system while it was off.

S5: Soft off. The system when executing a shutdown will go to a state where the PIIX4E is waiting for events to wake it up. Only the RTC section of the PIIX4E is running in this state. The system is only truly off when the AC power is unplugged.

6.2.12 Console Redirection

The BIOS supports redirection of both video and keyboard through a remote link (serial or LAN). When console redirection is enabled, local (host system) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console through the remote link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the host server can operate without a keyboard or video controller attached and run entirely via the remote console, thus allowing the host system to be completely headless. Setup and any other text-based utilities can be accessed via console redirection.

6.2.12.1 Limitations

Console redirection is a Real Mode BIOS extension, and does not operate outside of Real Mode. Console redirection does not work once an operating system or a driver such as EMM386 takes the processor into Protected Mode. If an application takes the processor in and out of Protected Mode, it should inhibit redirection before entering Protected Mode and restart it once back into Real Mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

6.2.12.2 Keystroke Mappings

During console redirection, the remote terminal (which may be a dumb terminal or a system with a modem running a communication program, such as ProComm) sends keystrokes to the local server. The local server passes video back over this same link. For keys that have an ASCII mapping, such as A and Ctrl-A, the remote simply sends the ASCII character. Keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters, as defined in the tables below. The strings are based on the ANSI terminal standards. Since the ANSI terminal standard does not define all the keys on the standard 101 key US keyboard, mappings for these keys were created, such as F5 – F12, Page Up, and Page Down.

Alt key combinations are created by sending the combination ^[} followed by the character to be alt modified. Once this Alt key combination is sent (^[}), the next keystroke sent will be translated into its Alt-key mapping (that is, if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by ‘a’ would send an Alt-a to the server.

The remote terminal can force a refresh of its video by sending ^[{.

Presently, the unusual combinations outside of the ANSI mapping and not in the table below are not supported (for example, Ctrl-F1).

Table 56: Non-ASCII key mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[			
F1	^[OP			
F2	^[OQ			
F3	^[OR			
F4	^[OS			
F5	^[OT			
F6	^[OU			
F7	^[OV			
F8	^[OW			
F9	^[OX			
F10	^[OY			
F11	^[OZ			
F12	^[O1			
Print Screen				
Scroll Lock				
Pause				
Insert	^[[L			
Delete	(7Fh)			
Home	^[[H			
End	^[[K			
Page Up	^[[M			
Page Down	^[[2J			
Up Arrow	^[[A			
Down Arrow	^[[B			
Right Arrow	^[[C			
Left Arrow	^[[D			
Tab	(09h)			

Grey cell = not supported, (xxh) = ASCII character xx

Table 57: ASCII key mappings

Key	Normal	Shift	Ctrl	Alt
Backspace	(08h)	(08h)	(7Fh)	^[](08h)
(accent) `	`	(tilda) ~		^[]`
1	1	!		^[]1
2	2	@		^[]2
3	3	#		^[]3
4	4	$		^[]4
5	5	%		^[]5
6	6	^		^[]6
7	7	&		^[]7
8	8	*		^[]8
9	9	(		^[]9
0	0	)		^[]0
(dash) -	-	(under) _	(1Fh)	^[]-
=	=	+		^[]=
a to z	a to z	A to Z	(01h) to (1Ah)	^[]a to ^[]z
[	[	{	(1Bh)	^[][
]	]	}	(1Dh)	^[]]
\	\	|	(1Ch)	^[]\
(semi-colon) ;	;	(colon) :		^[];
(apostrophe) ‘	`	(quote) “		^[]’
(comma) ,	,	<		^[],
(period) .	.	>		^[].
/	/	?		^[]/
(space)	(20h)	(20h)	(20h)	^[](20h)

Grey cell = not supported, (xxh) = ASCII character xx

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7 Flash Memory Update & Recovery Utility

7.1 Flash Memory Update Utility

The Flash Memory Update Utility (IFLASH.EXE) loads a fresh copy of the BIOS into Flash ROM. Updating a Flash area takes a file or series of files from a hard or floppy disk, and loads it in the specified area of Flash ROM.

BIOS upgrades and the Intel Flash Memory Update Utility are available from http://www.intel.com/isp.

NOTE

The utility IFLASH.EXE must be run without the presence of a Protected Mode control program, such as Windows or EMM386. Do not run in a DOS window under Windows NT, Win98 or Win95. IFLASH.EXE uses the processor's flat addressing mode to update the Flash part.

7.2 Loading the System BIOS

A new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the Flash part. As of this writing, the system BIOS area is 11 files. They are named:

- xxxxxxxx.BIO
- xxxxxxxx.BIA
- xxxxxxxx.BI1
- xxxxxxxx.BI2
- etc until xxxxxx.BI9

The first 8 letters of each filename on the release diskette can be any value, but cannot be renamed. Each file contains a link to the next file in the sequence. IFLASH.EXE does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged.

7.3 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in Flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. The procedure can only be monitored by listening to the speaker and looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS Flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.

- A series of continuous beeps indicates a failed BIOS recovery.

NOTE

BIOS recovery cannot be accomplished using non-SPD DIMMS. SPD data structure is required for the recovery process.

BIOS recovery diskette must be a standard 1.44 MB diskette, not a LS-120 type diskette.

8 Error Handling, Messages & Beep Codes

8.1 Introduction

This section defines how errors are handled by the system BIOS on the TR440BX platform. It describes the role of the BIOS in error handling and the interaction between the BIOS and platform hardware as far as error handling is concerned. In addition, error-logging techniques are described, and beep codes for errors are defined.

8.2 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on TR440BX can be categorized as follows:

- ISA bus
- PCI bus
- Memory single and multi-bit errors
- Sensors
- Processor internal error, thermal trip error, temperatures and voltages, GTL voltage levels

The BIOS cannot detect errors on the processor bus because PAC does not monitor these.

ISA and PCI bus errors can be further classified as ‘standard bus’ errors, which have a standard register interface across all platforms. All other errors, such as processor and ECC errors, are referred to as ‘product-specific’ errors, which require special consideration depending upon the system configuration. Product-specific errors can be emulated as standard bus errors, if specific routing of certain hardware signals, as documented in this section, will follow. This emulation is important to both OS and BIOS NMI handlers, which have no knowledge of product-specific errors, but need to recover and shut down the system gracefully.

8.3 Error Handlers

The BIOS has an NMI handler that gets invoked when an NMI occurs in POST. Generally, the OS traps the NMI and does not pass it onto the BIOS NMI handler. Therefore, the BIOS NMI handler is rarely invoked in a real operating environment. The SMI handler cannot be bypassed by the OS, and is used to handle and log system-level events that are not visible to the OS.

8.3.1 BIOS NMI Handler

To maintain DOS compatibility, the BIOS NMI handler only processes enabled standard bus errors, such as ISA Parity check or IOCHK# errors. It displays an error message, issues a beep signal, and halts. It disables NMI using bit 7 of I/O port 70h (RTC Index Port) on the occurrence of an unknown or spurious NMI. This can cause unusual side effects because it allows a spurious NMI to block a subsequent valid NMI.

8.3.2 OS NMI handler

The OS NMI handler processes standard bus errors at the OS level. Most OS NMI handler implementations are not product specific and behave in a manner similar to a BIOS NMI handler. It is the responsibility of the BIOS SMI handler to present platform-specific errors, such as multi-bit ECC error, as one of the standard bus errors, like parity error, to the OS NMI handler.

8.3.3 SMI Handler

The SMI handler preprocesses all system errors, even those that are normally considered to generate an NMI. The SMI handler is responsible for properly detecting the error type, logging it to the appropriate error log, and passing the error on to the OS if required.

8.4 Handling and Logging System Errors

This section describes the register bits associated with the various categories of system errors, and actions taken by error handlers. It covers the events logged by the BIOS and the format of data bytes associated. The BIOS is responsible for monitoring and logging certain system events. Some of the errors, such as processor failure, are logged by POST and not by the SMI handler.

8.4.1 Logging Format Conventions

The BIOS complies with the *System Management BIOS Reference Specification.* See this specification for the error log entry format. The current subset of supported system event log types is listed below. This list may change at any time and is only limited by the SMBIOS specification.

Table 58: Logging format conventions

Description	SEL Type	Variable Data Format
Single-bit ECC memory error	01h	00h
Multi-bit ECC memory error	02h	00h
Parity memory error	03h	02h
I/O channel check	05h	02h
POST error	08h	04h
PCI system error	0Ah	00h
System limit exceeded	10h	05h

8.4.2 ISA Bus Error

ISA bus errors generate an NMI, triggered by a memory error or IOCHK# assertion on the ISA bus. TR440BX always uses ECC memory, so it emulates the ISA memory parity error as an uncorrectable ECC memory error. For other system fatal errors generated by the PCI or processor bus, the SMI handler can emulate a memory parity error to pass control to the NMI handler. An I/O register at 61h (System Control port B) is defined that controls and indicates the errors. The NMI can be disabled using the RTC Index port bit 7 (I/O port 70h). The following tables show the action taken by each error handler, and control bits associated with the error.

Table 59: Error handler action on ISA bus error

Handler	Action
BIOS NMI	Display an error message, and halt the system.
OS NMI	Log the error and gracefully shut down the system.
BIOS SMI	Log the event(s).

Table 60: ISA bus error control bits

Location	Function	Bit(s)	Description	Value
I/O 61h	System Control	7	Memory parity check error flag (RO)	1 = error, 0 = OK
	Port B	6	Channel check (IOCHK#) error flag (RO)	
		5::4	Reserved	
		3	Channel check enable (RW)	1 = enable, 0 = disable
		2	Parity check enable (RW) (system board error enable)	
		1::0	Reserved	

8.4.3 PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported directly by SERR#. SERR# can be routed to NMI. In the TR440BX platform, PAC is the device that reports errors on PCI #1 using SERR#. All the PCI-to-PCI bridges are configured so they generate SERR# on the primary interface whenever there is SERR# on the secondary side. The same is true for PERR#. The following tables show the action taken by each error handler, and control bits associated with this error.

Table 61: Error handler action on PCI bus error

Handler	Action
BIOS NMI	Halt the system and disable NMI
OS NMI	Log the error and shutdown the system
BIOS SMI	Log PCI errors

Table 62: PCI bus error control bits

Location	Function	Bit(s)	Description	Value
PAC 04h	Command	6	PERR# enable	1 = enable, 0 = disable
PAC 05h	Command	1	SERR# enable	1 = enable, 0 = disable
PAC 90h	Error	4	Enable SERR# on receiving Target abort	1 = enable, 0 = disable
	Command	3	Enable SERR# on PCI parity Error	
	Register	1	Enable SERR# on Multi-Bit ECC/Parity error	
		0	Enable SERR# on Single-Bit ECC/Parity error	
PAC 91h	Error	4	Multi-Bit ECC/Parity error	1 = error, 0 = OK
	Status Reg.	0	Single-Bit ECC/Parity error	

8.4.4 Processor Bus Error

The PAC does not report processor bus AERR# and BERR# error signals to the system. (AERR# indicates an address parity error and BERR# indicates an unrecoverable processor bus error.) Therefore, the system SMM handler does not log and report these types of errors to the OS.

8.4.5 Memory Bus Error

The PAC generates SERR# on single and double-bit errors. The following register bits control and log the errors. The following tables show the action taken by each error handler, and control bits associated with this error.

Table 63: Error handler action on memory bus error

Handler	Action
BIOS NMI	Emulation or Disable NMI
OS NMI	Log the error and shutdown the system
BIOS SMI	Log the error Note: The SMI handler might emulate processor bus fatal errors (only), and pass control to the BIOS NMI handler.

Table 64: Memory bus error control bits

Location	Function	Bit(s)	Description	Value
PAC 90h	Command	1	Enable multi-bit memory Error Reporting	1 = enabled, 0 = disabled
		0	Enable single-bit memory Error Reporting	
PAC 91h	Memory Error	7-5	DRAM row where the last multi-bit error occurred Valid only if bit 4 is set	0 to 7
		4	Multi-bit ECC error flag	1 = error, 0 = OK
		3-1	DRAM row where the last SBE occurred Valid only if bit 0 is set	0 to 7
	Status	0	Single-Bit ECC error flag,	1 = error, 0 = OK

8.4.6 System Limit Error

The TR440BX Heceta 2 ASIC monitors system operational limits. It manages the A/D converter, defines voltage and temperature limits, and defines chassis intrusion. Any

sensor values outside of specified limits are fully handled by the BIOS and OS software. The BIOS response to any critical Heceta 2 error is to log the error, display an error condition, and shutdown the system.

8.4.7 Processor Failure

The BIOS detects BIST failure and watchdog timer reset events.

8.5 Error Messages and Error Codes

The following tables show the beep codes and error messages for AMIBIOS.

Table 65: Beep codes

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry is faulty.
2	Parity Error	Parity error in the base memory (the first 64 KB block) of memory.
3	Base 64 KB Memory Failure	Memory failure in first 64 KB.
4	Timer Not Operational	A memory failure in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU generated an error.
6	8042 - Gate A20 Failure	Cannot switch to protected mode.
7	Processor Exception Interrupt Error	The CPU on the CPU Card generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in AMIBIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM has failed.
11	Cache Memory Bad – Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. Do not press <Ctrl> <Alt> <Shift> <+> to enable cache memory.

Table 66: Error messages description

Error Message	Description
8042 Gate-A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry.
C: Drive Error	No response from drive C:. Run the AMIDiag Hard Disk Utility. Check the C: hard disk type in Standard Setup.
C: Drive Failure	No response from hard disk drive C:. Replace the drive.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Run AMIDiag.
CH-2 Timer Error	An AT system has two timers. There is an error in timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	CMOS RAM checksum is different than the previous value. Run WINBIOS Setup.
CMOS System Options Not Set	The values stored in CMOS RAM have been destroyed. Run WINBIOS Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected. Run WINBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory found by AMIBIOS is different than the amount in CMOS RAM. Run WINBIOS Setup.
CMOS Time and Date Not Set	Run Standard Setup to set the date and time.
D: Drive Error	No response from drive D:. Run the AMIDiag Hard Disk Utility. Check the hard disk type in Standard Setup.
D: Drive failure	No response from hard disk drive D:. Replace the drive.
Diskette Boot Failure	The boot diskette in drive A: cannot be used to boot the system. Use another boot diskette and follow the screen instructions.
Display Switch Not Proper	Some systems require a video switch be set to either color or monochrome. Turn the system off, set the switch properly, then power on.
DMA Error	Error in the DMA controller.
DMA 1 Error	Error in the first DMA channel.
DMA 2 Error	Error in the second DMA channel.
FDD Controller Failure	AMIBIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	AMIBIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR1 Error	Interrupt channel 1 failed POST.
INTR2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	AMIBIOS can read the diskette in floppy drive A:, but it cannot boot the system with it. Use another boot diskette and follow the screen instructions.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue to boot.
Keyboard Error	The keyboard has a timing problem. Make sure a Keyboard Controller AMIBIOS is installed. Set Keyboard in Advanced Setup to Not Installed to skip the keyboard POST routines.
KB/Interface Error	There is an error in the keyboard connector.

Error Message	Description
No ROM BASIC	Cannot find a proper bootable sector on drive A:, C:, or CD-ROM drive. AMIBIOS cannot find ROM Basic.
Off Board Parity Error	Parity error in memory installed on an adapter card in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On Board Parity Error	Parity error in serverboard memory. The format is: ON BOARD PARITY ERROR ADDR = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
Parity Error ????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.

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9 BIOS Setup Program

9.1 Introduction

The Setup program is used for viewing and changing the BIOS settings of this system. The user accesses Setup by pressing <F2> key after the POST memory test begins and before the operating system boot begins. The menu bar and brief description of each is shown in Table 67.

Table 67: BIOS Setup menu bar

Main	Advanced	Security	Boot	System Management	Exit
Allocates resources for hardware components	Configures advanced features available through the chipset	Set passwords and security features	Selects boot options and power supply control	Configures server management features such as console redirection	Saves or discards changes to Setup program options

If "Quiet Boot" is enabled, an OEM logo will display instead of the "Press <F2> to enter Setup" message. The user can still enter Setup by pressing <F2> during the time an OEM logo is displayed.

NOTE

Note that a few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

Table 68 shows the function keys available for menu screens.

Table 68: BIOS Setup function keys

Setup Key	Description
<**Enter**>	Select Submenu: The <Enter> key activates sub-menus when the selected feature is a sub-menu, displays a pick list if a selected feature has a value field, or selects a sub-field for multi-valued features like time and date. If a pick list is displayed, the <Enter> key undoes the pick list, and allows another selection in the parent menu.
<**ESC**>	Exit: The <ESC> key provides a mechanism for backing out of any field. This key undoes the pressing of the <Enter> key. When the <ESC> key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the <ESC> key is pressed in any sub-menu, the parent menu is re-entered. When the <ESC> key is pressed in any major menu, the exit confirmation window displays and the user is asked whether changes can be discarded.
<**Tab**>	Select Field: The <Tab> key selects a field within a configurable field. For example, when configuring the system time, use the <Tab> key to move between the hour, minute, and second fields.
<↑> or <↓>	Select Item: The up or down arrow selects the previous or next value in a pick list, or the previous or next feature in a menu item's option list. The selected item must then be activated by pressing the <Enter> key.

Setup Key	Description
<→> or <←>	Select Menu: The left and right arrow keys move between the major menu pages. The keys have no effect if a sub-menu or pick list is displayed.
<**F9**>	Setup Defaults: Load the default configuration values for all fields. A menu will appear asking user to confirm. Press <Yes> to load defaults. Press <No> to cancel loading defaults.
<**F10**>	Save and Exit: Save the current values and exit Setup. A menu will appear asking user to confirm. Press <Yes> to save and exit. Press <No> to remain in Setup.

9.2 Main Menu

The menu bar is shown below.

Main	Advanced	Security	Boot	System Management	Exit

Table 69 shows the Main menu. This menu reports processor and memory information and is for configuring the system date and time.

Table 69: Main menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed (MHz).
Processor Serial Number	Disabled **Enabled (default)**	Enables or disables PSN. PSN is only available for a Pentium III processor.
Cache RAM	No options	Displays cache size (KB).
Total Memory	No options	Displays total memory (MB).
Bank 0 Bank 1 Bank 2 Bank 3	No options	Displays memory type for each bank or “Not Installed.”
Language	**English (US) (default)** French Deutsch Japanese Italian Spanish	Selects which language the BIOS displays.
Memory Configuration	Non-ECC **ECC (default)**	Allows the user to turn error reporting on or off if the system and all memory installed support ECC (Error Correction Code).
System Time	HH:MM:SS	Sets the system time.
System Date	MM/DD/YYYY	Sets the system date.

9.3 Advanced Menu

The menu bar is shown below.

Main	**Advanced**	Security	Boot	System Management	Exit

Table 70 shows the Advanced menu. This menu configures advanced features that are available through the chipset.

Table 70: Advanced menu

Feature	Options	Description
Boot Configuration	See Table 71	Configures Plug and Play, Numlock key, and reset Configuration Data on next boot.
Peripheral Configuration	See Table 72	Configures peripheral ports and devices.
IDE Configuration	See Table 73	Configures IDE devices.
Diskette Configuration	See Table 75	Configure diskette drive settings.
Event Log Configuration	See Table 76	Configures system event log options.

Table 71: Boot configuration submenu

Feature	Options	Description
Plug & Play O/S	Yes **No (default)**	Specifies if a Plug and Play operating system is being used. “No” lets the BIOS configure all the devices in the system. “Yes” lets the operating system configure Plug & Play (PnP) devices not required for boot if yours system has a Plug and Play operating system.
Reset Config Data	Yes **No (default)**	Clears the BIOS PCI/PnP configuration data stored in Flash on next boot.
Numlock	Off **On (default)**	Selects the power on state of the Numlock key.

Table 72: Peripheral configuration submenu

Feature	Options	Description
Serial Port A	**Enabled (default)** Disabled Auto	Disables or enables serial port A. Enabled (default) Base I/O address [3F8] Interrupt [IRQ 4]
Serial Port B	**Enabled (default)** Disabled Auto	Disables or enables serial port B. Enabled (default) Base I/O address [2F8] Interrupt [IRQ 3]
Legacy USB Support	**Disabled (default)** Enabled Auto	Disables or enables support for legacy USB.

Table 73: IDE configuration menu

Feature	Options	Description
IDE Controller	**Boot (default)** Disabled Primary Secondary	"Disabled" disables the integrated IDE Controller. "Primary" enables only the primary IDE Controller. "Secondary" enables the secondary IDE Controller. "Both" enables both IDE Controllers.
Hard Disk Pre-Delay	**Disabled (default)** 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Selects the hard disk drive pre-delay. Causes the BIOS to insert a delay before attempting to detect IDE drives in the system. Configures primary and secondary IDE devices as the name of the drive found or Not Installed.
Primary IDE Master	If device detected, see Table 74 for IDE configuration options.	Reports name of device installed, otherwise displays "Not Installed."
Primary IDE Slave	If device detected, see Table 74 for IDE configuration options.	Reports name of device installed, otherwise displays "Not Installed."
Secondary IDE Master	If device detected, see Table 74 for IDE configuration options.	Reports name of device installed, otherwise displays "Not Installed."
Secondary IDE Slave	If device detected, see Table 74 for IDE configuration options.	Reports name of device installed, otherwise displays "Not Installed."

Table 74: IDE configuration submenu

Feature	Options	Description
Type	None User **Auto (default)** CD-ROM ATAPI Removable Other ATAPI IDE Removable	Specifies the IDE configuration mode for IDE devices. "User" allows the cylinders, heads, and sectors fields to be changed. "Auto" automatically fills in the values of the cylinders, heads, and sectors fields.
LBA Mode Control	Disabled **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	Disabled 2 sectors 4 sectors 8 sectors **16 sectors (default)**	Specifies the number of sectors per block for transfers in a single interrupt from the hard drive to memory. Check the hard drive's specification for optimum setting.
PIO Mode	**Auto (default)** 0 1 2 3 4	Configures the PIO mode.
Ultra DMA	**Disabled (default)** Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	Configures the Ultra DMA mode.

Table 75: Diskette configuration submenu

Feature	Options	Description
Diskette Controller	Disabled **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	Not Installed 360KB 5.25” 1.2MB 5.25” 720KB 3.5” **1.44/1.25MB 3.5” (default)** 2.88MB 3.5”	Disables or enables floppy A and specifies size.
Diskette Write Protect	**Disabled (default)** Enabled	Disables or enables write protect for the diskette drive.

Table 76: Event log configuration submenu

Feature	Options	Description
Event Log	No options	Displays whether or not there is space available in the event log.
Event Log Validity	No options	Displays whether or not the contents of the event log are valid.
Clear All Event Logs	Yes **No (default)**	Clears the event log after rebooting.
Event Logging	Disabled **Enabled (default)**	Disables or enables logging of events.
ECC Event Logging	Disabled **Enabled (default)**	Disables or enables logging of ECC events.

9.4 Security Menu

The menu bar is shown below.

Main	Advanced	**Security**	Boot	System Management	Exit

Table 77 shows the Security menu. This menu sets passwords and security features.

Table 77: Security menu

Feature	Options	Description
User Password Is	No options	Displays whether or not there is a supervisor password installed. Default is no user password installed.
Supervisor Password Is	No options	Displays whether or not there is a user password installed. Default is no supervisor password installed.
Set Supervisor Password	Press <Enter> to input a supervisor password.	Password can be up to seven alphanumeric characters. Default is no supervisor password.
Set User Password	Press <Enter> to input a user password.	Password can be up to seven alphanumeric characters. Default is no user password.
Clear User Password	No options	Clears the user password.
User Access Level	Limited No Access View Only **Full (default)**	"Limited" allows only limited fields to be changed such as Date and Time. "No Access" prevents user access to the Setup Utility. "View Only" allows access to the Setup Utility but the fields can not be changed. "Full" allows any field to be changed.

9.5 Boot Menu

The menu bar is shown below.

Main	Advanced	Security	**Boot**	System Management	Exit

Table 78 shows the Boot menu. This menu sets boot features and the boot sequence.

Table 78: Boot menu

Feature	Options	Description
Quiet Boot	**Enabled (default)** Disabled	"Disabled" displays normal POST messages. "Enabled" displays OEM logo instead of POST messages.
Quick Boot	**Enabled (default)** Disabled	Allows the BIOS to skip certain tests while booting. This decreases the time needed to boot the system.
Scan User Flash Area	**Disabled (default)** Enabled	Allows the BIOS to scan the Flash ROM for user binaries.
After Power Failure*	Stays Off **Last State (default)** Power On	Determines the mode of operation if a power loss occurs. "Stays Off" keeps system off once power is restored. "Power On" boots the system after power is restored. "Last State" restores the system to the same state it was in before the power failed.
On Modem Ring	**Stay Off (default)** Power On	Determines the action of the system when the system power is off and the modem is ringing.
On LAN	Stay Off **Power On (default)**	Determines the action of the system when a LAN wake up event occurs.
On PME	**Stay Off (default)** Power On	Determines the action of the system when a PCI Power Management Enabled wake up event occurs.
IDE Drive Configuration	Primary Master IDE **1st IDE (default)** 2nd IDE 3rd IDE 4th IDE Primary Slave IDE **2nd IDE (default)** Secondary Master IDE **3rd IDE (default)** Secondary Slave IDE **4th IDE (default)**	Configures the peripheral devices. Configurable options for other IDE devices are similar to Primary Master IDE.
1st to 8th Boot Devices	**Floppy (default)** **IDE-HDD** **ATAPI CD-ROM** **ARMD-FDD** **ARMD-HDD** **Intel UNDI, PXE-2.0** **Intel UNDI, PXE-2.0** **Disabled**	Configures the boot sequence from the available devices. IDE-HDD = Hard disk drive. Intel UNDI, PXE-2.0 = Network boot using PXE. ARMD-FDD = ATAPI removable device-floppy disk drive. SCSI = If a SCSI device is installed, it will appear as one of the possible boot devices with the name of device.

* Note for the BIOS to correctly set this feature, the system must be powered down via the power switch

9.6 System Management Menu

The menu bar is shown below.

Main	Advanced	Security	Boot	**System Management**	Exit

Table 79 shows the System Management menu. This menu sets server management features.

Table 79: System management menu

Feature	Options	Description
Serial Console Redirection	**Disabled (default)** Enabled	Disables or enables serial console redirection.
Baud Rate	9600 **19.2K (default)** 38.4K 115.2K	Sets the baud rate.
Flow Control	No Flow Control **CTS/RTS (default)** XON/XOFF CTS/RTS+CD	If enabled, it will use the flow control selected. CTS/RTS = Hardware. XON/XOFF = Software. CTS/RTS + CD = Hardware + Carrier Detect for modem use.

9.7 Exit Menu

The menu bar is shown below.

Main	Advanced	Security	Boot	System Management	**Exit**

Table 80 shows the Exit menu. This menu exits the Setup program – saving, discarding, and loading default settings.

Table 80: Exit menu

Feature	Options	Description
Exit Saving Changes	No options	Exits system Setup and saves your changes in CMOS.
Exit Discarding Changes	No options	Exits system setup without saving your changes in CMOS.
Load Setup Defaults	No options	Loads setup defaults.
Load Custom Defaults	No options	Loads custom defaults.
Save Custom Defaults	No options	Save custom defaults.
Discard Changes	No options	Discards changes.

10 Certification

10.1 Safety Standards / Certifiers

Table 81: Safety standards/certifier summary

USA/Canada	UL 1950, 3rd Edition/CSA 22.2, No. 950M93, 3rd Edition
Europe	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International	CB Certificate and Report to IEC 60950, 3rd Edition including EMKO-TSE (74-SEC) 207/94 and other national deviations

10.2 Electromagnetic Compatibility (EMC) Regulations

Table 82: Electromagnetic compatibility (EMC) summary

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024, Immunity Standard for Information Technology Equipment EN61000-3-2 Harmonic Currents EN61000-3-3 Voltage Flicker
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit). IEC 1000-3-2; Harmonic Currents
Taiwan	BSMI, Class A (CISPR 22)
Russia	Gost Approval
International	CISPR 22, Class A Limit

10.3 Mandatory / Standard: Certifications, Registration, Declarations

- UL, cUL Listing
- German GS Mark
- Nordic Certification
- FCC Declaration of Conformity
- CE Mark Declaration of Conformity
- VCCI Certification
- Industry Canada Certification
- Australia Communications Authority Declaration of Conformity

10.4 Environmental Limits

10.4.1 System Office Environment

Table 83: System office environment summary

Operating Temperature	+10°C to +35°C De-rated 0.5°C/1000ft. Altitude to 5,000 ft. max. Maximum rate of change of 10°C per hour.
Non-Operating Temperature	-40°C to +70°C
Non-operating Humidity	95%, non-condensing @ 30°C
Acoustic noise	< 48 dBA @ 28°C±2°C
Operating Shock	No errors with a half sine wave shock of 2G (with 11-millisecond duration).
Package Shock	Operational after a 24-inch free fall, although cosmetic damage may be present
ESD	15kV per Intel Environmental test specification

10.4.2 System Environment Testing

The system was tested per *Intel Product Qualification Specification, Intel Doc. #25-653000*. These tests include:

- Temperature Operating and Non-Operating
- Humidity Non-Operating
- Shock Packaged and Un-packaged
- Vibration Packaged and Un-packaged
- AC Voltage, Freq. & Source Interrupt
- AC Surge
- Acoustics
- ESD

11 Reliability and Serviceability

11.1 Reliability

Based on a typical configuration, as listed in Table 84, the system's Mean-Time-Between-Failure (MTBF) as shipped from the factory was calculated to be approximately 21,182 hours.

Table 84: MTBF summary

Component	Qty	MTBF (hrs)
Fan	5	125,000*
125W power supply	1	200,000
TR440BX serverboard	1	670,000
Pentium® III processor	1	4,000,000
Front panel	1	7,000,000
Slim-line CD-ROM drive (1% duty cycle)	1	14,100,000
Slim-line floppy drive (1% duty cycle)	1	18,200,000
Memory (256MB)	4	24,100,000*
PCI I/O riser card	1	55,800,000
		21,182 hrs

11.2 Serviceability

The desired Mean-Time-To-Repair (MTTR) of the system is approximately less than 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Table 85: MTTR summary

Action	Approx. Time (min)
Remove top cover	0.20
Remove and replace disk drives	5
Remove IDE disk drives and install SCSI hard drives	12
Remove and replace 3.5" diskette drive	3
Remove 3.5" floppy and install slim-line CD-ROM/diskette combo	5
Remove and replace slim-line CD-ROM/diskette combo	9
Remove and replace power supply	3
Remove and replace fans	8
Remove and replace riser card	1
Remove and replace front panel board	2
Remove and replace serverboard (with CPU, memory, riser card installed)	6
Remove and replace DIMMs	1
Remove and replace processor	1

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12 Compatibility Testing

Validation of the Intel® ISP1100 Internet Server with third-party operating systems and hardware is an on-going process. Please visit http://www.intel.com/isp to find an up-to-date compatibility test report.

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13 Specifications and Customer Support

13.1 Online Support

Find the latest information on the Intel® ISP1100 Internet Server online at Intel's site at http://www.intel.com/isp.

13.2 Specifications

Table 86 lists the specifications mentioned in this document.

Table 86: Specification references

Specification	Description	Revision Level
ACPI	Advanced Configuration and Power Interface Specification	Revision 1.0b, February 8, 1999. Intel Corporation, Microsoft Corporation, and Toshiba Corporation. http://www.teleport.com/~acpi
AMI BIOS	American Megatrends BIOS Specification	AMIBIOS 98. http://www.amibios.com
ATA-3	Information Technology – AT Attachment-3 Interface	X3T10/2008D Revision 6, October 25, 1995. ftp://fission.dt.wdc.com/pub/standards
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5. (SFF) Fax Access: (408) 741-1600
ATX	ATX Form Factor Specification	Revision 2.03, December 1998. Intel Corporation http://www.teleport.com/~ffsupprt/spec/atxspecs.htm
BIOS Boot Specification	BIOS Boot Specification (BBS)	Version 1.01, January 11, 1996. Compaq Computer Corporation, Intel Corporation, and Phoenix Technologies Ltd. ftp://download.intel.com/ial/wfm/bbs101.pdf
DMTF Systems Standard Groups Definition	DMTF Systems Standard Groups Definition	http://www.dmtf.org/spec/dmis.html.
El Torito	Bootable CD-ROM Format Specification	Version 1.0, January 25, 1995. Phoenix Technologies Ltd. and IBM Corporation http://www.phoenix.com/products/specs.html
Heceta 2	Heceta 2 ASCI – Low Cost Hardware Monitor	Revision 1.03, December 30, 1997. Intel Corporation http://developer.intel.com/ial/wfm/wfm20/design/bibliog.htm
Intel 440BX AGPSet	Intel 440BX AGPSet: 82443BX Host Bridge/Controller	Intel Corporation http://developer.intel.com/design/chipsets/440bx/
Intel 82371 PIIX4E	Intel 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4E)	Intel Corporation http://developer.intel.com/design/chipsets/datashts/

Specification	Description	Revision Level
Intel 82559 Ethernet Controller	Intel Fast Ethernet Multifunction PCI/Cardbus Controller	Revision 2.0, May 1999. Intel Corporation ftp://download.intel.com/design/network/datashts/73825902.pdf
Intel E28F008S585 Flash	Intel E28F008S585 Flash	Intel Corporation http://developer.intel.com/design/flash/
Intel® Celeron™ Processor	Intel® Celeron™ Processor	Intel Corporation http://developer.intel.com/design/processor/
Intel® Pentium® III Processor	Intel® Pentium® III Processor	Intel Corporation http://developer.intel.com/design/processor/
IrDA	Serial Infrared Physical Layer Link Specifications	Infrared Data Association http://www.irda.org/standards/specifications.asp
Low-Profile PCI	Low-Profile PCI Specification	PCI Special Interest Group http://www.pcisig.com
microATX	microATX Serverboard Interface Specification	Version 1.0, December 1997. Intel Corporation http://www.teleport.com/~ffsupprt/spec/microatxspecs.htm
PC99 Design Guide	PC99 Design Guide	Version 1.0, July 14, 1999. Microsoft Corporation, Intel Corporation, Compaq Computer Corporation, Dell Corporation, Gateway, Inc., and Hewlett-Packard Company http://www.microsoft.com/hwdev/pc99.htm.
PCI	PCI Local Bus Specification	Revision 2.2, December 18, 1998. PCI Special Interest Group Revision 1.1, December 18, 1998. PCI Special Interest Group http://www.pcisig.com
Intel® Pentium® Pro BIOS Writer's Guide	Intel® Pentium® Pro BIOS Writer's Guide	Intel Corporation Call 1-800-548-4725
Plug and Play	Plug and Play BIOS Specification	Version 1.0a, May 5, 1994. Compaq Computer Corporation, Phoenix Technologies Ltd., and Intel Corporation http://www.microsoft.com/hwdev/respec/pnpspecs.htm
POST Memory Manager	POST Memory Manager (PMM)	Version 1.01, November 21, 1997. Phoenix Technologies Ltd. and Intel Corporation http://www.ptltd.com/products/specs-pmm101.pdf.
PXE	Preboot Execution Environment (PXE) Specification	Version 2.1, September 20, 1999. Intel Corporation and SystemSoft Corporation http://developer.intel.com/ial/wfm/wfmspecs.htm
PXE BIOS Support	Preboot Execution Environment (PXE) BIOS Support	Revision 1.1, June 9, 1997. Intel Corporation ftp://download.intel.com/ial/wfm/lsa-wp.pdf
SDRAM DIMMs (64 and 72-bit)	PC SDRAM Unbuffered DIMM	Revision 1.0, February 1998. Revision 1.63, October 1998.

Specification	Description	Revision Level
	Specification PC SDRAM DIMM Specification PC100 Registered DIMM Specification PC Serial Presence Detect (SPD) Specification	Revision 1.2, October 1998. Revision 1.2a, December 1997. Intel Corporation http://developer.intel.com/design/chipsets/memory/
SMBIOS	System Management BIOS Reference Specification	Version 2.3.1, March 16, 1999. American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, IBM Corporation, Phoenix Technologies Ltd., and SystemSoft Corporation http://developer.intel.com/ial/wfm/design/smbios/
SMSC FDC37B80X	FDC37B80x PC98/99 Compliant Enhanced Super I/O Controller with Keyboard/Mouse Wake-Up	Standard Microsystems Corporation http://www.smsc.com/main/datasheet.html
UHCI	Universal Host Controller Interface (UHCI) Design Guide	Revision 1.1, March 1996. Intel Corporation http://www.usb.org/developers/docs.html
USB	Universal Serial Bus Specification	Revision 1.1, September 23, 1998. Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC Corporation http://www.usb.org/developers/docs.html