ALC203
ALC203-LF

TWO-CHANNEL AC'97 2.3 AUDIO CODEC

DATASHEET

Rev. 1.6
28 April 2006

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw

USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.00	2003/06/10	First release.
1.10	2003/05/30	1.Pin-45 is re-defined as a Jack-Detect (JD0).
1.20	2003/08/06	1.Digital data path in Section 3-2.
1.30	2003/10/24	Add ordering information.
1.40	2005/03/14	Add lead (Pb)-free and version package identification information on page 4 and on page 48.
1.50	2005/12/05	Update section 6.1.12 MX1A Record Select, page 12. Update section 12. Ordering Information, page 48.
1.60	2006/04/28	Add a note to, and change Susceptibility Voltage data in section 7.1.1 Absolute Maximum Ratings, page 27.

Table of Contents

1. General Description

The ALC203 AC'97 codec is a 20-bit DAC and 18-bit ADC full duplex AC'97 2.3 compatible stereo audio codec designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC203 incorporates proprietary converter technology to achieve a high SNR, greater than 100 dB, sensing logic for device reporting, and Universal Audio Jack® to improve user experience.

The ALC203 supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC203 CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The circuitry of the ALC203 codec operates from a +3.3V digital power and +5V analog power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. An integrated 14.318M→24.576MHz PLL generate required clock to eliminate the need for external crystal. Built in PCBEEP generator to save buzzer on board.

The ALC203 integrates a 50mW/20Ω headset audio amplifier into the codec, saving BOM costs. The ALC203 also supports the SPDIF out function, compliant with AC'97 2.3, which offers easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. The ALC203 codec supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipsets.

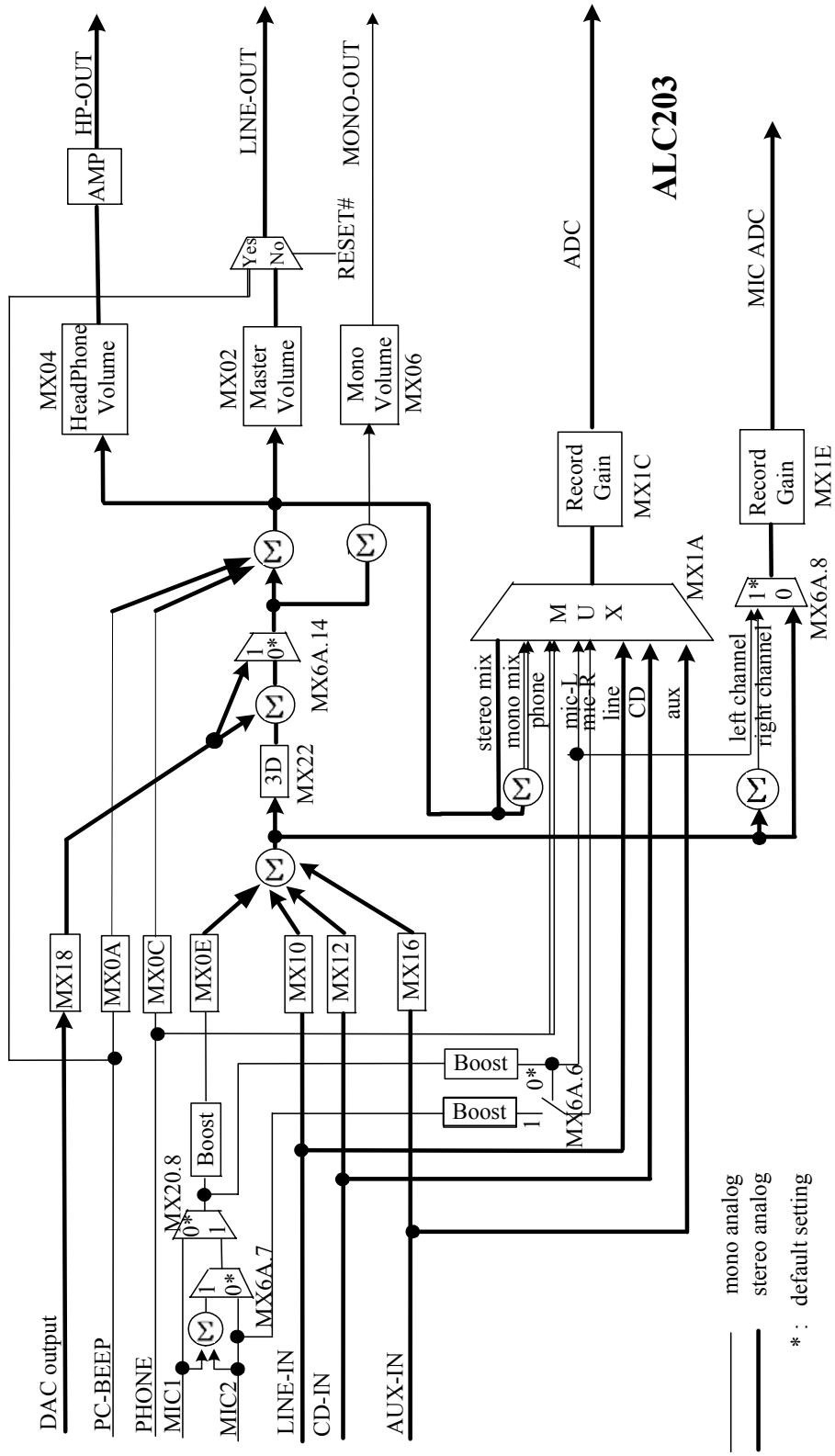
Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/ Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-types of environment sound emulation, 10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users.

2. Features

- Single chip with high S/N ratio (>100 dB)
- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 20-bit DAC and 18-bit ADC resolution
- 18-bit Stereo full-duplex CODEC with independent and variable sampling rate
- ***Compliant with AC'97 2.3 specifications***
  -LINE/HP-OUT, MIC-IN and LINE-IN sensing
  -14.318MHz-→24.576MHz PLL saves crystal
  -12.288MHz BITCLK input can be consumed
  -Integrated PCBEEP generator to save buzzer
  -Interrupt capability
  -Page registers and Analog Plug&Play
- Support of S/PDIF out is fully compliant with AC'97 rev2.3 specifications
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP, PHONE-IN
- Supports double sampling rate (96KHz) of DVD audio playback
- Two software selectable MIC inputs
- +6/12/20/30dB boost preamplifier for MIC input
- Stereo output with 6-bit volume control
- Mono output with 5-bit volume control
- Headphone output with 50mW/20Ω amplifier
- 3D Stereo Enhancement
- Multiple CODEC extension capability
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features
- **Stereo MIC record for AEC/BF application**
- **DC Voltage volume control**
- Auxiliary power to support **Power Off CD**
- Adjustable VREFOUT control
- **2 GPIO pins with smart GPIO volume control**
- **2 Universal Audio Jack (UAJ)® for front panel**
- Support 32K/44.1K/48K/96KHz of S/PDIF output
- Support 32K/44.1K/48KHz of S/PDIF input
- Standard 48-Pin LQFP Package
- **EAX™ 1.0 & 2.0 compatible**
- **Direct Sound 3D™ compatible**
- **A3D™ compatible**
- **I3DL2 compatible**
- **HRTF 3D Positional Audio**
- **Sensaura™ 3D Enhancement** (optional)
- **10 Bands of Software Equalizer**
- **Voice Cancellation and Key Shifting in KaraOK mode**
- **AVRack® Media Player**
- **Configuration Panel to improve User Experience**

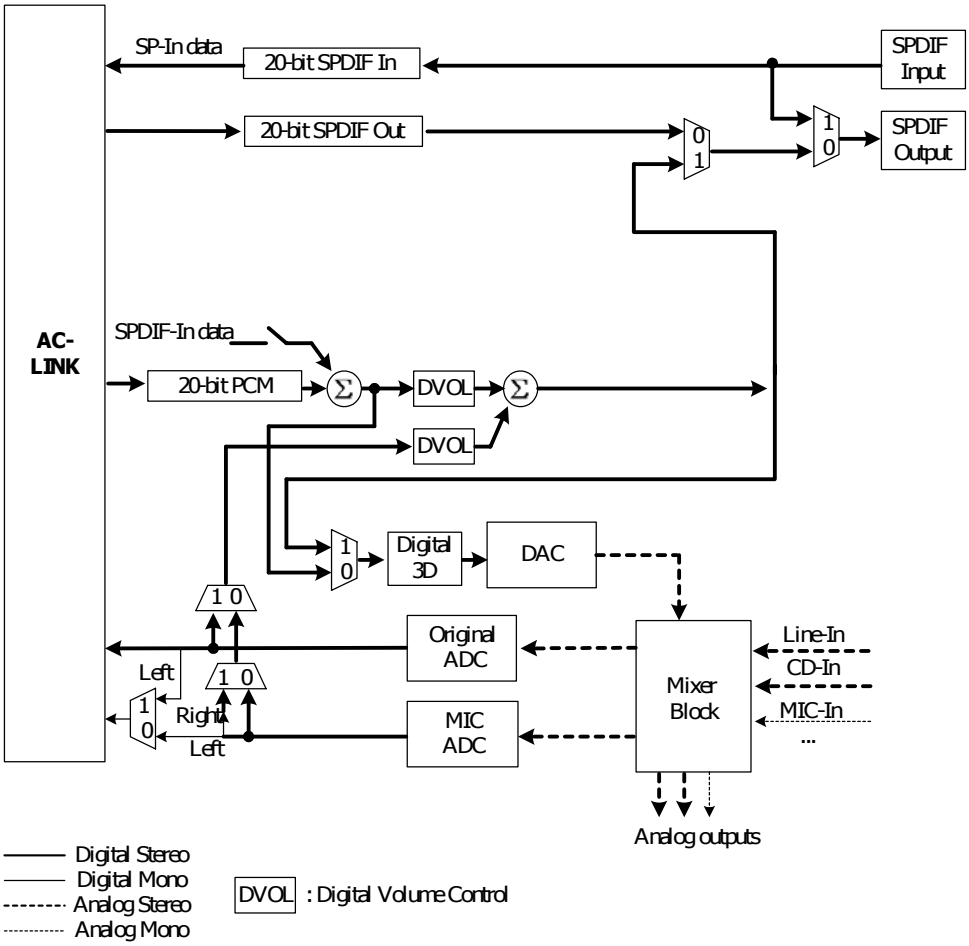
3. Block Diagram

3.1 Analog Mixer Block



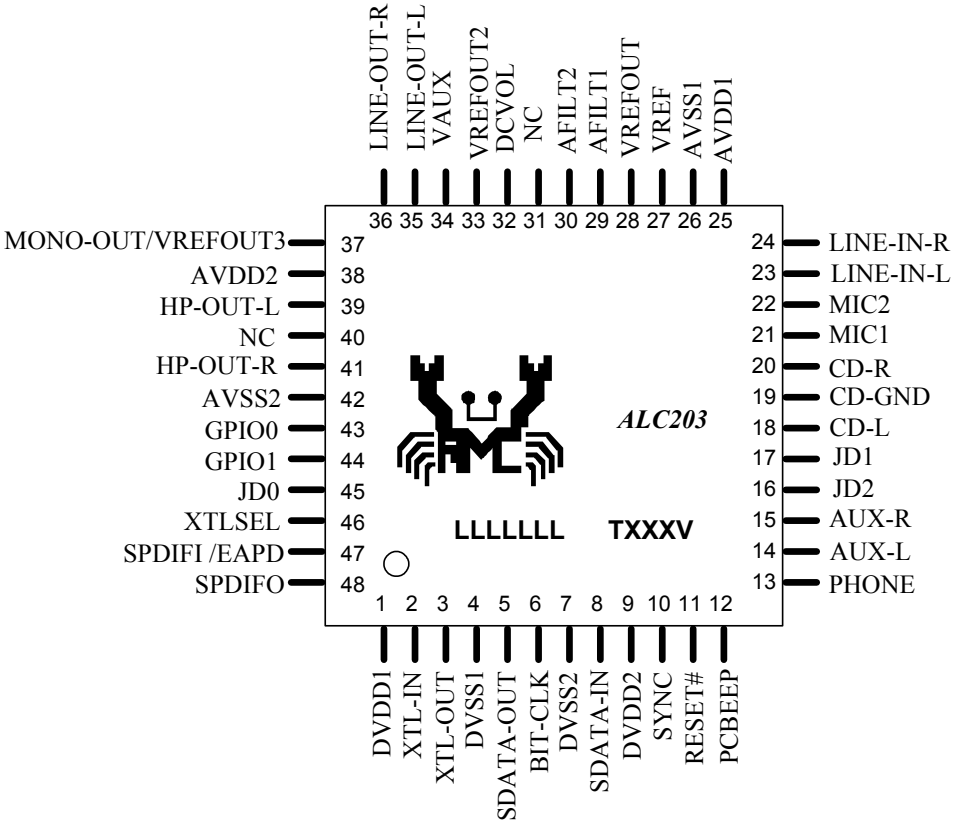
Analog Mixer Diagram

3.2 Digital Data Path



Digital data path diagram

4. Pin Assignments



Pin Assignments

4.1 Lead (Pb)-Free Package and Version Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in the figure above. The version number is shown in the location marked 'V'.

5. Pin Description

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the Pin Assignment diagram for a graphical representation.

5.1 Digital I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
RESET#	I	11	AC'97 H/W reset	Schmitt trigger input
XTL-IN	I	2	Crystal input pad	Crystal: 24.576M/14.318M crystal input External: 24.576M/14.318M external clock input
XTL-OUT	O	3	Crystal output pad	Crystal: 24.576M/14.318M crystal output External: 24.576M/14.318M clock output
SYNC	I	10	Sample Sync (48KHz)	Schmitt trigger input
BIT-CLK	IO	6	Bit clock input/output (12.288Mhz)	CMOS input/output
SDATA-OUT	I	5	Serial TDM AC97 output	CMOS input
SDATA-IN	O	8	Serial TDM AC97 input	CMOS output
GPIO0	I/O	43	General purpose pin-0. (Smart volume up)	Internally pulled high by a 50K resistor.
GPIO1	I/O	44	General purpose pin-1. (Smart volume down)	Internally pulled high by a 50K resistor.
XELSEL	I	46	Pulled low to use external 14.318MHz clock source	CMOS input Vt=0.35Vdd, internally pulled high by a 50K resistor.
SPDIFI/EAPD	O	47	S/PDIF input / External Amplifier power down control	CMOS input / output
SPDIFO	O	48	S/PDIF output	Digital output has 12 mA@75Ω driving capability.
				Total: 13 Pins

5.2 Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1.6Vrms)
PHONE	I	13	Speakerphone input	Analog input (1.6Vrms)
AUX-L	IO	14	AUX Left channel	Analog input/output
AUX-R	IO	15	AUX Right channel	Analog input/output
JD2	I	16	Jack Detect 2 for UAJ2	Internally pulled high to AVDD by a 50K resistor
JD1	I	17	Jack Detect 1 for UAJ2	Internally pulled high to AVDD by a 50K resistor
JD0	I	45	Jack Detect 0 for MIC	Internally pulled high to AVDD by a 50K resistor
CD-L	I	18	CD audio Left channel	Analog input (1.6Vrms)
CD-GND	I	19	CD audio analog GND	Analog input
CD-R	I	20	CD audio Right channel	Analog input (1.6Vrms)
MIC1	I	21	First MIC input	Analog input (1.6Vrms)
MIC2	I	22	Second MIC input	Analog input (1.6Vrms)
LINE-IN-L	I	23	Line input Left channel	Analog input (1.6Vrms)
LINE-IN-R	I	24	Line input Right channel	Analog input (1.6Vrms)
LINE-OUT-L	O	35	Line-Out Left channel	Analog output w/o amplifier
LINE-OUT-R	O	36	Line-Out Right channel	Analog output w/o amplifier
HP-OUT-L	IO	39	Headphone Out Left channel	ALC203: Analog output with amplifier / Analog input
HP-OUT-R	IO	41	Headphone Out Left channel	ALC203: Analog output with amplifier / Analog input
MONO-OUT/ VREFOUT3	O	37	Speaker Phone output / Third Ref. voltage out	Analog output / Third reference voltage output (2.5V/4.0V)
				Total: 18 Pins

5.3 Filter/Reference/NC

Name	Type	Pin No	Description	Characteristic Definition
VREF	-	27	Reference voltage	1uf capacitor to analog ground
VREFOUT	O	28	Ref. voltage out	Analog DC voltage output (2.5V / 4.0V)
AFILT1	-	29	ADC anti-aliasing filter	1000pf capacitor to analog ground.
AFILT2	-	30	ADC anti-aliasing filter	1000pf capacitor to analog ground.
NC	-	31	Not Connection	
DC VOL	I	32	DC Voltage Volume Control	Analog Input (AGND~AVDD)
VREFOUT2	O	33	Secondary Ref. voltage out	Analog DC voltage output (2.5V / 4.0V)
VAUX	I	34	Auxiliary Power to keep CD and amplifier turned on.	+5V analog stand-by power
NC	-	40	Not Connection	
				Total: 9 Pins

5.4 Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD	
AVDD2	I	38	Analog VDD	
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
DVDD1	I	1	Digital VDD (3.3V)	
DVDD2	I	9	Digital VDD (3.3V)	
DVSS1	I	4	Digital GND	
DVSS2	I	7	Digital GND	
				Total: 8 Pins

6. Registers

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0. X=Reserved bit.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0190h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	RM*	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone volume	Mute	X	HPL5	HPL4	HPL3	HPL2	HPL1	HPL0	RM*	X	HPR5	HPR4	HPR3	HPR2	HPR1	HPR0	8000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	F7	F6	F5	F4	F3	F2	F1	F0	PB3	PB2	PB1	PB0	X	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	BGO1	BGO0	X	BC	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	RM*	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	RM*	X	X	CR4	CR3	CR2	CR1	CR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	RM*	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	RM*	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	ADC Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
1Eh	MIC ADC Record Gain	Mute	X	X	X	LMRG3	LMRG2	LMRG1	LMRG0	X	X	X	X	RMRG3	RMRG2	RMRG1	RMRG0	8000h
20h	General Purpose	POP	X	3D	X	DRSS1	DRSS0	MIX	MS	LBK	X	X	X	X	X	X	X	0400h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	DP2	DP1	DP0	0000h
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	0000h
26h	Power Down Ctrl/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	X	X	X	X	X	X	SPDIF	DRA	VRA	0A07h
2Ah	Extended Audio Status	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	DRA	VRA	0000h
2Ch	PCM front Out Sample Rate	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8	FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0	BB80h
32h	PCM Input Sample Rate	ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0	BB80h
34h	MIC Input Sample Rate	MSR15	MSR14	MSR13	MSR12	MSR11	MSR10	MSR9	MSR8	MSR7	MSR6	MSR5	MSR4	MSR3	MSR2	MSR1	MSR0	BB80h
3Ah	S/PDIF Ctl	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h
60h/6Eh	Vendor Define	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
76h	GPIO Setup	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
78h	GPIO Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	414Ch
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0	4770h

6.1.1 MX00 Reset
Default: 0190h

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values, then the written data is ignored. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15		**Reserved**
14:10	R	Return 00000b
9	R	Read as 0 (No support for 20-bit ADC)
8	R	Read as 1 (Support for 18-bit ADC)
7	R	Read as 1 (Support for 20-bit DAC)
6	R	Read as 0 (No support for 18-bit DAC)
5	R	Read as 0 (No support for Loudness)
4	R	Read as 1 (Headphone output support)
3	R	Read as 0 (No simulated stereo; for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	**Reserved,** Read as 0
0	R	Read as 0 (No dedicated MIC PCM input)

6.1.2 MX02 Master Volume
Default: 8000h

These registers control the overall volume level of the output functions. Each step on the left and right channels corresponds to a 1.5dB increase/decrease in volume.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14		**Reserved**
13:8	R/W	**Master Left Volume** (MLV[5:0]) in 1.5 dB steps
7:6		**Reserved**
5:0	R/W	**Master Right Volume** (MRV[5:0]) in 1.5 dB steps

❶ For MRV/MLV: 00h 0 dB attenuation
3Fh 94.5 dB attenuation

6.1.3 MX04 Headphone
Default: 8000h

Register 04h controls the headphone (ALC203) output volume. Each step in bits 5:0 and 13:8 corresponds to a 1.5dB increase/decrease in volume, allowing 63 levels of volume, from 000000 to 111111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14		**Reserved**
13:8	R/W	**Headphone/True Line Output Left Volume** (HPL[5:0]) in 1.5 dB steps
7:6		**Reserved**
5:0	R/W	**Headphone/True Line Output Right Volume** (HPR[5:0]) in 1.5 dB steps

❶ For HPR/HPL: 00h 0 dB attenuation
3Fh 94.5 dB attenuation

6.1.4 MX06 MONO_OUT Volume
Default: 8000h

Register 06h controls the mono volume output. Mono output is the same data sent on all output channels. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5		**Reserved**
4:0	R/W	**Mono Master Volume** (MMV[4:0]) in 1.5 dB steps

❶ For MMV: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

6.1.5 MX0A PC BEEP Volume
Default: 8000h

This register controls the input volume for the PC beep signal. Each step in bits 4:1 corresponds to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC203, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the LINE-OUTL & R pins. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:5	R/W	**Internal PCBEEP Frequency, F[7:0]** The internal PCBEEP frequency is the result of dividing the 48KHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48KHz/(255*4)=47Hz. The highest tone is 48KHz/(1*4)=12KHz. A value of 00h in F[7:0] disables internal PCBEEP generator and allows external PCBEEP input.
4:1	R/W	**PC Beep Volume** (PBV[3:0]) in 3 dB steps
0		**Reserved**

❶ For PBV: 00h 0 dB attenuation
0Fh 45 dB attenuation

6.1.6 MX0C PHONE Volume
Default: 8008h

Register 0Ch controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5		**Reserved**
4:0	R/W	**Phone Volume** (PV[4:0]) in 1.5 dB steps

❶ For PV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.7 MX0E MIC Volume
Default: 8008h

Register 0Eh controls the microphone input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Bit 6 enables/disables a boost in volume to a magnification based on bits 9:8.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:10		**Reserved**
9:8	R/W	**Boost Gain Option** (BGO) 00: 20 dB 01: 6 dB 10: 12 dB 11: 29.5 dB (V=30*Vmic-in)
7		**Reserved**
6	R/W	**Boost Control** (BC) 0: Disable 1: Enable Boost
5		**Reserved**
4:0	R/W	**Mic Volume** (MV[4:0]) in 1.5 dB steps

❶ For MV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

❷ If 29.5dB boost gain is selected, input resistor can be reduced to save area of feedback resistor.

6.1.8 MX10 LINE_IN Volume
Default: 8808h

Register 10h controls the LINE_IN input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**Line-In Left Volume** (NLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Line-In Right Volume** (NRV[4:0]) in 1.5 dB steps

❶ For NLV/NRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.9 MX12 CD Volume
Default: 8808h

Register 12h controls the CD input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**CD Left Volume** (CLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**CD Right Volume** (CRV[4:0]) in 1.5 dB steps

❶ For CLV/CRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.10 MX16 AUX Volume
Default: 8808h

Register 16h controls the auxiliary input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**AUX Left Volume** (ALV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**AUX Right Volume** (ARV[4:0]) in 1.5 dB steps

❶ For ALV/ARV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.11 MX18 PCM_OUT Volume
Default: 8808h

Register 18h controls the PCM_OUT output volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**PCM Volume** (PLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**PCM Right Volume** (PRV[4:0]) in 1.5 dB steps

❶ For PLV/PRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.12 MX1A Record Select
Default: 0000h

Register 1Ah controls the record input source. Each bit in bits 2:0 selects a recording source for the right channel. Each bit in bits 10:8 selects a recording source for the left channel.

Bit	Type	Function
15:11		**Reserved**
10:8	R/W	**Left Record Source Select** (LRS[2:0])
7:3		**Reserved**
2:0	R/W	**Right Record Source Select** (RRS[2:0])

❶ For LRS

0	MIC
1	CD LEFT
2	Muted
3	AUX LEFT
4	LINE LEFT
5	STEREO MIXER OUTPUT LEFT
6	MONO MIXER OUTPUT
7	PHONE

❷ For RRS

0	MIC
1	CD RIGHT
2	Muted
3	AUX RIGHT
4	LINE RIGHT
5	STEREO MIXER OUTPUT RIGHT
6	MONO MIXER OUTPUT
7	PHONE

6.1.13 MX1C Record Gain for Stereo ADC
Default: 8000h

Register 1Ch controls the record gain. Each step in bits 3:0 corresponds to a 1.5dB increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 corresponds to a 1.5dB increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:12		**Reserved**
11:8	R/W	**Left Record Gain Select** (LRG[3:0]) in 1.5 dB steps
7:4		**Reserved**
3:0	R/W	**Right Record Gain Select** (RRG[3:0]) in 1.5 dB steps

❶For LRG/RRG:

0Fh	+22.5dB
00h	0 dB (No Gain)

6.1.14 MX1E Record Gain for MIC ADC
Default: 8000h

Register 1Eh controls the record gain. Each step in bits 3:0 corresponds to a 1.5dB increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 corresponds to a 1.5dB increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:12		**Reserved**
11:8	R/W	**Left Record Gain Select** (LMRG[3:0]) in 1.5 dB steps
7:4		**Reserved**
3:0	R/W	**Right Record Gain Select** (RMRG[3:0]) in 1.5 dB steps

❶For LRG/RRG: 0Fh +22.5dB
00h 0 dB (No Gain)

6.1.15 MX20 General Purpose Register
Default: 0000h

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the MIC selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Bit	Type	Function
15:14		**Reserved**, Read as 0
13	R/W	**3D Control** 1: On 0: Off
12:9		**Reserved**, Read as 0
8	R/W	**MIC Select** 0: MIC 1 1: MIC 2
7	R/W	**AD to DA Loop-back Control** 0: Disable 1: Enable
6:0		**Reserved**

6.1.16 MX22 3D Control
Default: 0000h

This register is used to control the 3D stereo enhancement function built into the AC'97 component. The register bits, DP2-DP0 are used to control the separation ratios in the 3D control for both LINE_OUT and DAC_OUT.

The 3D stereo enhancement function provides for a deeper and wider sound experience with a potential 6-speaker arrangement. Note that the 3D bit in the general purpose register (bit 13) must be set to 1 to enable this function.

Bit	Type	Function
15:3		**Reserved**, Read as 0
2:0	R/W	**Depth Control** (DP[2:0])

❶3D effect control

DP[2:0]	Function	DP[2:0]	Function
000	0% (off*)	100	50%
001	12.5%	101	67.5%
010	25%	110	75%
011	37.5	111	100%

6.1.17 MX24 Audio interrupt and Paging
Default: 0000h

Bit	Type	Function
15		**Interrupt Status, I4** 0: Interrupt is clear 1: Interrupt was generated Interrupt event and status are clear by writing a 1 to this bit. The status will change regardless of interrupt enable (I0).
14	R	**Interrupt Cause, I3** I3=0: GPIO, SPDIF-IN and Jack-Detect interrupt status in MX78 are not changed. 1: GPIO, SPDIF-IN and Jack-Detect interrupt status in MX78 are changed. I3= (MX78.14|MX78.13|MX78.12|MX78.6|MX78.5|MX78.4) This bit reflects the cause of the **first** interrupt event generated. Software should read it after interrupt status (I4) has been confirmed as interrupting. I3 will be zero when I4 is cleared.
13	R	**Interrupt Cause, I2** I2=0: Sense value in page ID-01h MX6A.[12:8] has not changed. 1: Sense cycle completed or new sense value in page ID-01h MX6A.[12:8] is available. This bit reflects the cause of the **first** interrupt event generated. Software should read it after interrupt status (I4) has been confirmed as interrupting. I2 will be zero when I4 is cleared.
12	R/W	**Sense Cycle, I1** 0: Sense cycle not in progress 1: Sense cycle start Writing a '1' to this bit causes a sense cycle start. If a sense cycle is in progress, writing a '0' to this bit will abort the sense cycle. Whether the data in the sense result register (page ID-01h MX6A) is valid or not is determined by the IV bit in MX6A, Page ID-1h.
11	R/W	**Interrupt Enable, I0** 0: Interrupt is masked, interrupt status (I4) will not be shown in bit 0 in Slot 12 in SDATA-IN. 1: Interrupt is un-masked, interrupt status (I4) will be shown in bit 0 in Slot 12 in SDATA-IN.
10:4	NA	Reserved, read as 0
3:0	R/W	**Page Selector, PG[3:0]** 0000b: Vendor Specific 0001b: Page ID 01 (AC'97 2.3 Discovery Descriptor Definition) Others: Reserved. This register is used to select a descriptor of 16 word pages between registers MX60 to MX6F. Value of 0 is used to select vendor specific space to maintain compatibility with AC'97 2.2 vendor specific register. Once PG[3:0] is not 0000b and 0001b, ALC203 will return zero data for ACLINK mixer read command.

6.1.18 MX26 Powerdown Control/Status
Default: 000Fh

This read/write register is used to program power-down states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7 and bit 15.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control /status register to determine exactly which subsections, if any, are ready.

Bit	Type	Function
15	R/W	**PR7 External Amplifier Power Down** (EAPD) 0: Normal 1: Power down
14	R/W	**PR6** 0: Normal 1: Power down Headphone Out (HP-OUT, pin-39/41)
13	R/W	**PR5** 0: Normal 1: Disable internal clock
12	R/W	**PR4** 0: Normal 1: Power down AC-Link
11	R/W	**PR3** 0: Normal 1: Power down Mixer (Vref off)
10	R/W	**PR2** 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	**PR1** 0: Normal 1: Power down PCM DAC
8	R/W	**PR0** 0: Normal 1: Power down PCM ADC and input MUX
7:4		**Reserved**, Read as 0
3	R	**Vref Status** 1: Vref is up to normal level 0: Not yet ready
2	R	**Analog Mixer Status** 1: Ready 0: Not yet ready
1	R	**DAC Status** 1: Ready 0: Not yet ready
0	R	**ADC Status** 1: Ready 0: Not yet ready

❶Truth table for power down mode :

	ADC	DAC	Mixer	Verf	ACLINK	Int CLK	HP-OUT	EAPD
PR0=1	PD							
PR1=1		PD						
PR2=1			PD				PD	
PR3=1	PD	PD	PD	PD			PD	
PR4=1	PD	PD			PD			
PR5=1	PD	PD				PD		
PR6=1							PD	
PR7=1								PD

PD: Power down Blank: Don't care

❷If Mixer is power down (PR2=1 or PR3=1), the LINE-OUT (pin-35/36) is shut down and its output is floated.
❸If Headphone-Out is power down (PR6=1), the HP-OUT (pin-39/41) is shut down and its output is floated.

6.1.19 MX28 Extended Audio ID
Default: 0605h

The Extended Audio ID register is a read only register used to communicate information to the digital controller on two functions. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 45 and 46 externally. "00" returned defines the CODEC as the primary CODEC, while any other code identifies the CODEC as one of three secondary CODEC possibilities.

Bit	Type	Function
15	R	**ID1**
14	R	**ID0**
13:12		**Reserved**, Read as 0
11:10	R	REV[1:0]=10 to indicate that the ALC203 is AC'97 rev2.3 compliant
9	R	**AMAP** read as 1 (DAC mapping based on ID)
8:6		**Reserved**, Read as 0
5:4	R/W	**DAC Slot Assignment** DSA[1:0] (Default value depends on ID[1:0]) DSA[1:0] Controls the DAC slot assignment, as described in AC'97 rev2.2.
3		**Reserved**, Read as 0
2	R	**SPDIF** Read as 1 (S/PDIF is supported)
1	R	**DRA** Read as 1
0	R	**VRA** Read as 1 (Variable Rate Audio is supported)

❶ ID[1:0] depend on the states of pins 46, 45, 44, and 43 when power-on reset or AC97_RESET# is active. Refer to section 9.1 for detailed information on configuration of ID[1:0].

❷ The ALC203 maps DAC slot according to the following table: (default maps to AC'97 spec. rev2.3)

DSA[1:0]	Left DAC slot #	Right DAC slot #	Comment
0,0	3	4	Default when ID[1:0]=00
0,1	7	8	Default when ID[1:0]=01,10
1,0	6	9	Default when ID[1:0]=11
1,1	10	11	-

6.1.20 MX2A Extended Audio Status and Control, Default: 0000h

This register contains two active bits for power-down and status of the surrounding DACs. Bits 0, 1, and 2 are read/write bits which are used to enable or disable VRA, DRA, and SPDIF respectively. Bits 4 and 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bit 10 is a read-only bit which tells the controller if the S/PDIF configuration is valid.

Bit	Type	Function
15	R/W	**Validity Configuration of S/PDIF Output** (VCFG) Combines with MX3A.15 to decide validity control in S/PDIF output signal.
14:11	NA	**Reserved**
10	R	**S/PDIF Configuration Valid** (SPCV) 0: Current S/PDIF configuration {SPSA, SPSR,DAC/slot rate} is not valid. 1: Current S/PDIF configuration {SPSA, SPSR,DAC/slot rate} is valid.
9:6		**Reserved**
5:4	R/W	**SPSA[1:0], S/PDIF Slot Assignment when DRS=0** 00: S/PDIF source data assigned to AC-LINK slot3/4 01: S/PDIF source data assigned to AC-LINK slot7/8 (Default when ID=00) 10: S/PDIF source data assigned to AC-LINK slot6/9 (Default when ID=01,10) 11: S/PDIF source data assigned to AC-LINK slot10/11 (Default when ID=11) **SPSA[1:0], S/PDIF-Out Slot Assignment when DRS=1(for 96K S/PDIF-Out)** 01: S/PDIF-Out source is from AC-LINK slot 3/4 + slot 7/8.
3		**Reserved**
2	R/W	**SPDIF** 1: Enable 0: Disable (SPDIFO is in high impedance)
1	R/W	**DRA** 1: Enable 0: Disable
0	R/W	**VRA** 1: Enable 0: Disable

❶ If VRA = 0, the ALC203's ADC/DAC operate at a fixed 48KHz sampling rate. Otherwise, they operate at a variable sampling rate defined in MX2C and MX32. VRA also controls the write operation of MX2Cand MX32.

❷ DRA can be written when (ID=00)&(DSA=00), otherwise it is always 0.
If DRA = 1, DAC operates at a fixed 96KHz sampling rate. The PCM(n) and PCM(n+1) data is captured in the same frame. In this mode, MX2C is fixed at BB80h, MX32 and ADC is still controlled by VRA.

❸**SPCV** is a read-only bit that indicates whether the current S/PDIF-Out configuration is supported or not. If the configuration is supported, SPCV is set as 1 by H/W. So driver can check this bit to determine the status of the S/PDIF transmitter system. SPCV is always operating, independent of the SPDIF enable bit (MX2A.2). The S/PDIF output is active if MX2A.2 is set in spite of SPCV. Once S/PDIF output is enabled but SPCV is invalid (SPCV=0), channel status is still output, but the output data bits will be all zero.

6.1.21 MX2C PCM DAC Rate
Default: BB80h

The ALC203 allows adjustment of the output sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**Output Sampling Rate** FOSR[15:0]

❶ The ALC203 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling rate	FOSR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

❷Note that If the value written is not support, the closest value is returned.
When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

6.1.22 MX32 PCM ADC Rate
Default: BB80h

The ALC203 allows adjustment of the input sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**Output Sampling Rate** FISR[15:0]

❶ The ALC203 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling rate	FISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

❷Note that if the value written is not supported, the closest value is returned.
When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

6.1.23 MX3A S/PDIF Out Channel Status/Control
Default: 2000h

Bit	Type	Function
15	R/W	**Validity Control** (control V bit in Sub-Frame) 0: The V bit (valid flag) in the sub-frame depends on whether the S/PDIF data is under-run or over-run. 1: The V bit in sub-frame is always sent as 1 to indicate the invalid data is not suitable for receiver.
14	R	**DRS (Double Rate S/PDIF)** 0: 32K, 44.1K, 48K S/PDIF-Out 1: 96K S/PDIF-Out *This bit can only be set when SPSR is 10b.*
13:12	R/W	**S/PDIF Sample Rate** SPSR[1:0] 00: Sample rate set to 44.1KHz, Fs[**0:3**]=0000 01: Reserved 10: Sample rate set to 48.0KHz, Fs[**0:3**]=0100 (default) 11: Sample rate set to 32.0KHz, Fs[**0:3**]=1100
11	R/W	**Generation Level** (LEVEL)
10:4	R/W	**Category Code (**CC[6:0])
3	R/W	**Preemphasis** (PRE) 0: None 1: Filter pre-emphasis is 50/15 µsec
2	R/W	**Copyright** (COPY) 0: Not asserted 1: Asserted
1	R/W	**Non-Audio Data type** (/AUDIO) 0: PCM data 1: AC3 or other digital non-audio data
0	R	**Professional or Consumer format** (PRO) 0: Consumer format 1: Professional format The ALC203 supports consumer channel status format, so this bit is always 0.

❶The consumer channel status block (bit0~bit31):

0	1	2	3	4	5	6	7
PRO=0	/AUDIO	COPY	PRE	0	0	0	0
8	9	10	11	12	13	14	15
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
16	17	18	19	20	21	22	23
0	0	0	0	0	0	0	0
24	25	26	27	28	29	30	31
Fs0	Fs1	Fs2	Fs3	0	0	0	0

❷ The “V” bit in the sub-frame is determined by Validity control (MX3A.15) and VCFG (MX2A.15):

Validity	VCFG	Operation
0	0	If S/PDIF FIFO is under-run, the “V” bit in the sub-frame is set to indicate that the S/PDIF data is invalid.
0	1	If S/PDIF FIFO is under-run, the “V” bit in the sub-frame is always 0, and pads the data with “0”s.
1	0	The “V” bit is always 1, and data bits (bit 8 ~ bit 27) should be forced to 0.
1	1	The “V” bit in sub-frame is always “0”, and the S/PDIF output data should be forced to zero.

6.2 Vendor Defined Registers (Page-00h)

These registers are available to Realtek and Realtek customers for specialized functions.

6.2.1 Page -0h, MX60 S/PDIF In Status [15:0]
Default: 0000h

The data in MX60 are captured from channel status [15:0] of S/PDIF-IN signal.

Bit	Type	Function
15	R	LEVEL (Generation Level)
14:8	R	CC[6:0] (Category Code)
7:6	R	Mode[1:0]
5:3	R	PRE[2:0] (Pre-Emphasis)
2	R	COPY (Copyright) 0: asserted 1: Not asserted
1	R	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	PRO (Professional or Consumer format) 0: consumer format 1: professional format

6.2.2 Page -0h, MX62 S/PDIF In Status [29:15]
Default: 0000h

The data in MX62 are captured from channel status [29:16] of S/PDIF-IN signal.

Bit	Type	Function
15	R	"V" bit in sub-frame of SPDIFI 0: Data X and Y are valid 1: At least one of data X and Y is invalid This bit is real-time updated, and it is meaning when S/PDIF-IN is locked
14	R	S/PDIF-IN Input Signal Locked by hardware 0: Unlocked 1: Locked
13:12	R	Ca[1:0] (Clock Accuracy)
11:8	R	Fs[3:0]. (Sample Frequency in channel status) 0000: 44.1KHz 0010: 48 KHz 0011: 32 KHz Others: Reserved
7:4	R	Cn[3:0] (Channel Number)
3:0	R	Sn[3:0] (Source Number)

6.2.3 Page -0h, MX6A Data Flow Control
Default: 0000h

Bit	Type	Function
15	NA	Reserved
14	R/W	**Direct DAC Mode** 0: Analog output is from summation of DAC and analog inputs. 1: Analog output is from DAC.
13:12	R/W	**S/PDIF Out Source** 00:S/PDIF data is from ACLINK controller 01: Reserved. 10:Directly bypass S/PDIF-In signal to S/PDIF-Out. 11: Reserved.
11	R/W	**Recorded PCM Data to ACLINK**

Bit	Type	Function
		0: Recorded PCM data to host is from original ADC 1: Recorded PCM data to host is from S/PDIF-IN
10:8	NA	Reserved
7	R/W	**MIC2 Source** 0: MIC2 1: (MIC1+MIC2)/2.
6	R/W	**ADC MIC Source** 0: Mono duplicated. (Default) 1: Stereo.
5:2	NA	Reserved
1	R/W	**S/PDIF-In Enable** 0: Disable 1: Enable
0	R/W	**S/PDIF-In Monitoring Control** 0: Disable, SPDIFI data is not added into PCM data to DAC. (Default) 1: Enable, SPDIFI data will be added into PCM data to DAC after SPDIFI is locked.

6.3 Discovery Descriptor (Page ID-01h)

These registers are defined in Ac'97 2.3 for sensing and analog plug & play functions.

6.3.1 Page -1h, MX62 PCI Sub System ID Default: FFFFh

Bit	Type	Function
15:0	R/W	**PCI Sub System Vendor ID** This register can be written once only after power on, and **is not affected by AC97 cold reset**. The system manufacture's BIOS can set its own sub-system ID. The default value FFFFh means this register is implemented and data is not set by BIOS.

6.3.2 Page -1h, MX64 PCI Sub Vendor ID Default: FFFFh

Bit	Type	Function
15:0	R/W	**PCI Vendor ID** This register can be written once only after power on, and **is not affected by AC97 cold reset**. The system manufacture's BIOS can set its own sub-vendor ID. The default value FFFFh means this register is implemented and data is not set by BIOS.

6.3.3 Page -1h, MX66 Sense Function Select
Default: 0000h

Bit	Type	Function
15:5		Reserved
4:1	R/W	**Function Code bits, FC[3:0]** These bits specify the type of audio function described in page ID-01h MX66, MX68 and MX6A. 0h: LINE OUT 1h: HP OUT 5h: MIC1 In 6h: MIC2 In 7h: LINE In Others: Not supported
0	R/W	**Tip or Ring Selection, T/R** This bit sets which jack conductor the sense value is measured from. It is combined with FC[3:0]. 0: Tip (Left channel) 1: Ring (Right channel)

6.3.4 Page -1h, MX68 Sense Function
Default: 02F1h

Bit	Type	Function
15:11	R/W	**Gain bits, G[4:0]** These bits are updated by BIOS to tell driver the gain supported by external amplifier. 1 LSB = 1.5dBV 00000b: 0dBV, 00001b: +1.5dBV,… 01111b:+24dBV 10000b: 0dBV, 10001b: -1.5dBV,… 11111b: -24dBV
10	R/W	**Inversion bit, INV** 0: No inversion reported 1: Inverted.
9:5	R/W	**Buffer delays, DL[4:0]** Delay measurement for the signal from inputs to outputs channels in 20.83µsec (1/48000 second) units.
4	R/W	**Information Valid bit, IV** 0: After a sense cycle is completed, indicates that **no** information is provided on the sensing method 1: After a sense cycle is completed, indicates that information is provided on the sensing method Clearing this bit by writing "1", writing "0" to this bit has no effect.
3:1	NA	Reserved
0	R	**Function Information Present, FIP** This bit when set to a '1' indicates that the G[4:0], INV, DL[4:0] and ST[2:0] bits are supported and are Read/Write capable.

6.3.5 Page -1h, MX6A Sense Detail
Default: 0000h

Bit	Type	Function
15:13	R/W	**Connection/Jack Location bits, ST[2:0]** 000b: Rear I/O Panel (Default) 001b: Front Panel 010b: Motherboard 011b: Dock/External 100b ~ 110b: Reserved 111b: Unused I/O. These bits should be written by the BIOS to let the driver know where the specified I/O FC[3:0] are located.
12:8	R	**Sense bits, S[4:0]** (Default value depends on sensed result after Cold Reset) For output devices: 02h: Not specificed or unknown 05h: Powered speaker 06h: Earphone or passive speaker Other: Not supported For input deices: 12h: Not specified or unknown 13h: Mono Microphone 15h: Stereo Line-In Other: Not supported This field reports the type of output/input peripheral plugged in the jack after sensing.
7:0	R	Always read as 0.

6.4 Extension Registers

6.4.1 MX76 GPIO & Interrupt Setup

Default: 0000h

Bit	Type	Function
15	R/W	**GPIO Status Indication in SDATA_IN** 0:The status of GPIO0/GPIO1/JD and its valid tag are not indicated in SDATA_IN. 1: The status of GPIO0/GPIO1/JD and its valid tag are indicated in SDATA_IN
14	R/W	**SPDIFI Valid Interrupt Enable** 0:Disable 1: Enable
13	R/W	**SPDIFI Lock Interrupt Enable** 0:Disable 1: Enable
12	R/W	**JD2 (Jack-Detect 2) interrupt Enable** 0: Disable 1: Enable. A low to high transaction will trigger the JD2 interrupt in bit0 of SDATA_IN's slot-12.
11:7		Reserved
6	R/W	**JD1 (Jack-Detect 1) interrupt Enable** 0: Disable 1: Enable. A low to high transaction will trigger the JD interrupt in bit0 of SDATA_IN's slot-12.
5	R/W	**GPIO1 interrupt Enable** (when GPIO1 is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
4	R/W	**GPIO0 interrupt Enable** (when GPIO0 is used as input) 0: Disable 1: Enable. A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
3:2		Reserved
1	R/W	**GPIO1Primitive Control** 0: Set GPIO1 as input pin. 1: Set GPIO1 as output pin.
0	R/W	**GPIO0 Primitive Control** 0: Set GPIO0 as input pin. 1: Set GPIO0 as output pin.

6.4.2 MX78 GPIO & Interrupt Status
Default: 0000h

Bit	Type	Function
15	NA	Reserved
14	R/W	**S/PDINF-In Valid Interrupt Status (SPDIFIN_VIS)**. 0: No SPDIFI Valid Interrupt. 1: SPDIFI Valid interrupt. Write 1 to clear this status bit and its interrupt.
13	R/W	**S/PDINF-In Lock Interrupt Status (SPDIFIN_LIS)**. 0: No SPDIFI Lock interrupt. 1: SPDIFI LOCK interrupt. Write 1 to clear this status bit and its interrupt.
12	R/W	**JD2 Interrupt Status (JD2_IS)** 0: No JD2 interrupt. 1: JD2 interrupt. Write 1 to clear this status bit.
11:10	NA	Reserved
9	R/W	**GPIO1 Output Control** 0: Drive GPIO1 low. 1: Drive GPIO1 high.
8	R/W	**GPIO0 Output Control** 0: Drive GPIO0 as low. 1: Drive GPIO0 as high.
7	NA	Reserved
6	R/W	**JD1 Interrupt Status (JD1_IS)** 0: No JD1 interrupt. 1: JD1 interrupt. Write 1 to clear this status bit.
5	R/W	**GPIO1 Interrupt Status (GPIO1_IS)**. (When GPIO1 is used as input) 0: No GPIO1 interrupt. 1: GPIO1 interrupt. Write 1 to clear this status bit.
4	R/W	**GPIO0 Interrupt Status (GPIO0_IS)**. (When GPIO0 is used as input) 0: No GPIO0 interrupt. 1: GPIO0 interrupt. Write 1 to clear this status bit.
3	NA	Reserved
2	R	**Jack-Detect Event (JDEVT)** 0: No Jack-Detect event occurs. 1: Jack-Detect event occurs. ***JDEVT = JDS1 | JDS2*** Software can check this bit and MX7A.1 to know the status of JDx. When MX7A.5=0, MX7A.1=JDS1. When MX7A.5=1, MX7A.1=JDS2.
1	R	**GPIO1 Input Status** 0: GPIO1 is driven low by external device (input). 1: GPIO1 is driven high by external device (input).
0	R	**GPIO0 Input Status** 0: GPIO0 is driven low by external device (input). 1: GPIO0 is driven high by external device (input).

6.4.3 MX7A Miscellaneous Control
Default: 0000h

Bit	Type	Function
15:11	NA	Reserved
10	R/W	**Pin-37 Function Selection (MONO-OUT or Vrefout3)** 0: Vrefout3 1: MONO-OUT
9	R/W	**Vrefout Off Control** 0: Vrefout is normal on (output of buffered Vref). 1: Vrefout is off. (In High-Z).
8	R/W	**Vrefout / Vrefout2 / Vrefout3 Level Control** 0: 2.5V 1: 4.0V
7:6	NA	Reserved
5	R/W	**Source of Jack-Detect status for MX7A.1** 0: MX7A.1 indicates the status of Jack-Detect 1 1: MX7A.1 indicates the status of Jack-Detect 2
4	R/W	**HP-OUT Control** 0: Normal 1: HP-OUT is muted by H/W when MX7A.1=1
3	R/W	**MONO-OUT Control** 0: Normal 1: MONO-OUT is muted by H/W when MX7A.1=1
2	R/W	**SPDIF Output Gating** 0: SPDIF output is not gated with MX7A.1 1: SPDIF output is gated with MX7A.1. (SPDIFO is forced to 0 if MX7A.1=0)
1	R	**Status of Jack-Detect 1 or 2 (JDSx)** 0: JDSx is pull low 1: JDSx is floating or pull high
0	R/W	**LINE-OUT Output Control** 0: Normal 1: LINE-OUT output is muted by H/W when MX7A.1=1

6.4.4 MX7C Vendor ID1

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC203. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4770h, which is the third of the Microsoft ID code

Default: 414Ch

Bit	Type	Function
15:0	R	**Vendor ID "AL"**

6.4.5 MX7E Vendor ID2
Default: 4770h

Bit	Type	Function
15:8	R	**Vendor ID - "G"**
7:0	R	**Device ID** – 70h for ALC203

7. Electrical Characteristics

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital	DVDD	3.0	3.3	3.6	V
Analog	AVDD**	3.3	5.0	5.5	V
Operating Ambient Temperature	Ta	0	-	+70	^{o}C
Storage Temperature	Ts			+125	^{o}C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
Pin 9	4500 V				
Other Pins	5000 V				

*Note ** : The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Realtek technical support.*

7.1.2 Threshold Hold Voltage

Dvdd= 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage (XTLIN, SYNC, SDOUT, RESET#, BITCLK, GPIO, S/PDIF-IN)	V_{IL}	-	-	0.5Dvdd	V
High level input voltage (XTLIN, SYNC, SDOUT, RESET#, BITCLK, GPIO, S/PDIF-IN)	V_{IH}	0.5DVdd	-	-	V
High level output voltage	V_{OH}	0.9DVdd		-	V
Low level output voltage	V_{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	µA
Output leakage current (Hi-Z)	-	-10	-	10	µA
Output buffer drive current	-	-	5	-	mA
Internal pull up resistance	-	30k	50k	100k	Ω

7.1.3 Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+- 0.20		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+- 0.20		dB

7.1.4 S/PDIF output Characteristics

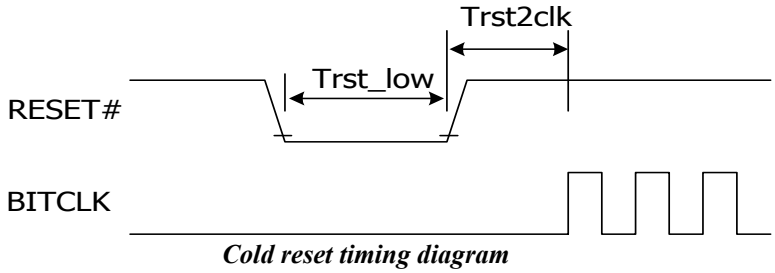
Dvdd= 3.3V, $T_{ambient}$=25^{0}C, with 75Ω external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
High level output voltage	V_{OH}	3.0	3.3		V
Low level output voltage	V_{OL}	-	0	0.3	V

7.2 AC Timing Characteristics

7.2.1 Cold Reset

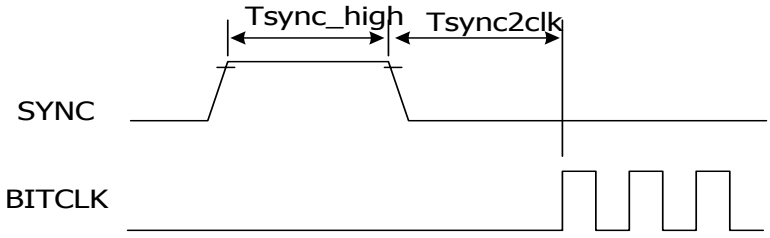
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns



Cold reset timing diagram

7.2.2 Warm Reset

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns



Warm reset timing diagram

7.2.3 AC-Link Clocks

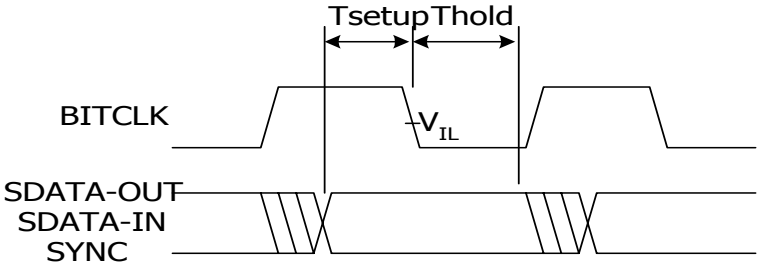
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Note 1: Worse case duty cycle restricted to 45/55.					

7.2.4 Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. Note 2: 50pF external load					

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output.					

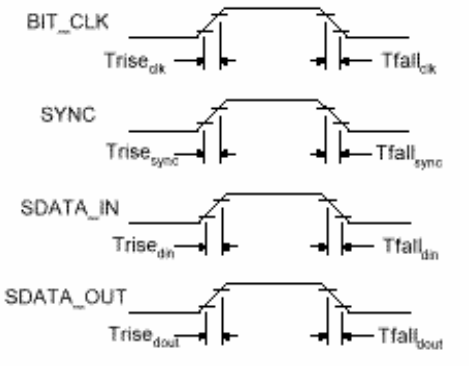
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					



Data Output and Input timing diagram

7.2.5 Signal Rise and Fall Timing

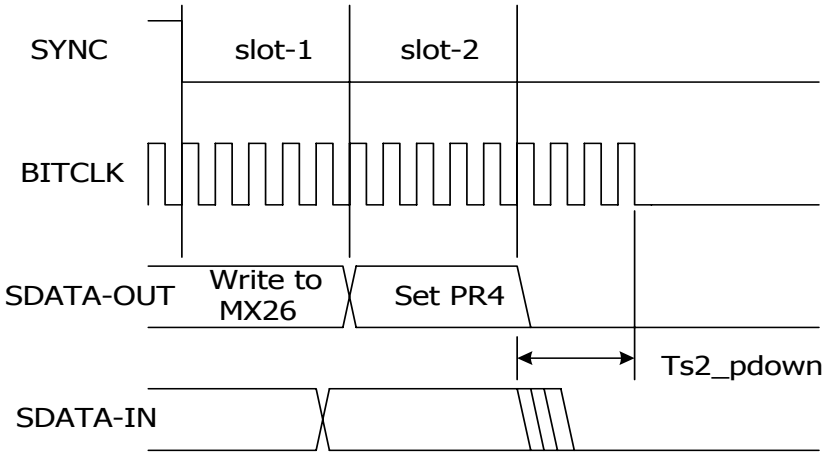
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	-	-	6	ns
SYNC rise time	$Trise_{sync}$	-	-	6	ns
SYNC fall time	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	-	-	6	ns
Note 1: 75pF external load (50 pF in AC'97 rev2.1) Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					



Signal Rise and Fall timing diagram

7.2.6 AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

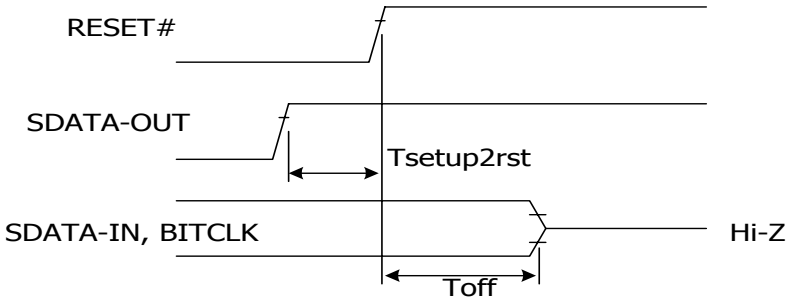


AC-Link low power mode timing diagram

7.2.7 ATE Test Mode

To meet AC'97 rev2.3 specifications, EAPD, SPDIFO, BIT_CLK, and SDATA_IN should be floating in test mode.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns



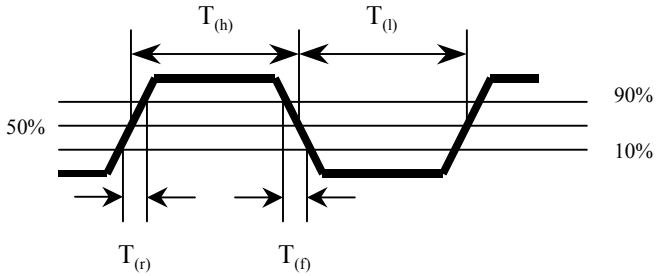
ATE test mode timing diagram

7.2.8 AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9 SPDIF Output

SPDIF_OUT	Minimum	Typical	Maximum	Units
Rise time/fall time	0		10	%
Duty cycle	45		55	%



Notes: Rise time = 100 * $T_{(r)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Fall time = 100 * $T_{(f)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Duty cycle = 100 * $T_{(h)}$/ ($T_{(l)}$+ $T_{(h)}$)%

8. Analog Performance Characteristics

Standard test conditions: $T_{ambient}=25^0C$, Dvdd=3.3V ±5%,Avdd=5.0V±5%
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Test bench Characterization BW: 10Hz~22KHz
0dB attenuation; tone and 3D disabled

Parameter	Minimum	Typical	Maximum	Units
Full scale input voltage: Line inputs (Mixers)	-	1.6	-	
Line inputs (A/D)	-	1.0	-	Vrms
Mic input (0 dB)	-	1.6	-	
Mic input (20 dB boost)	-	0.16	-	
Full scale output voltage				
LINE-OUT	-	1.25	-	Vrms
HP-OUT	-	1.25	-	Vrms
Analog to Analog S/N: CD to LINE-OUT	-	100	-	dB
Other to LINE-OUT	-	100	-	
Analog frequency response	10	-	22,000	Hz
S/N (A-weighted): D/A	-	100	-	dB
A/D	-	90	-	
Total Harmonic Distortion: D/A	-	-92	-	dB
A/D	-	-85	-	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-75	-	-	dB
Out-of-Band Rejection	-	-65	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-40	-	dB
MIC Boost Gain	6		30	dB
Master Volume (LINE- / HP-OUT): 64 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-94.5	dB
Master Volume (MONO-OUT): 32 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-46.5	dB
PC Beep Volume 16 steps:				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	-45	dB
Analog Mixer Volume 32 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB
Record Gain 16 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
DC Volume Control: 32 step				
Gain Control Range	0	-	-43	dB
0 dB DC voltage	-	-	0.1	V
Mute DC voltage	4.7	-	-	V
Input impedance (gain = 0dB, mixer = off)				
LINE-IN, CD-IN, AUX-IN, MIC1 / MIC2	-	64	-	KΩ
PCBEEP, PHONE	-	16	-	KΩ

cont…

Output Impedance LINE-OUT HP-OUT MONO-OUT	 - - -	 200 6 500	 - - -	 Ω Ω Ω
Amplifier Maximum Output Power @20Ω load	-	-	50	mW
Power Supply Current VA=5.0V VA=3.3V VD=3.3V	 - - -	 50 36 26	 - - -	 mA mA mA
Power Down Current VA=5.0V / 3.3V VD=3.3V	 - -	 - -	 1000 700	 uA uA
Vrefout/Vrefout2/Vrefout3	-	2.50	4.0	V
Vrefout Drive Current	-	8	-	mA

9. Design Suggestions

9.1 Clocking

The clock source is decided by XTLSEL and ID0# latched from pin-46/45 when **power-on reset and AC97_RESET# trailing edge.** The clock source of different configuration is listed below:

Configuration	**Operation & ID0**		
Pin-46(XTLSEL) / 45(ID0#)	**ID0**	**BIT-CLK**	**Clock source**
NC / NC	0 (Primary)	Output 12.288MHz	Crystal or ext. 24.576MHz is attached at XTL-IN
Low / NC	0 (Primary)	Output 12.288MHz	Crystal or ext. 14.318MHz is attached at XTL-IN
NC / NC	0 (Primary)	Input	*12.288M input at BIT-CLK*❶
X / Low	1 (Secondary)	Input	*12.288M input at BIT-CLK*
Low / Low	11 (Secondary)	Input	*12.288M input at BIT-CLK*❷

*Low: Pulled low by a 0 ohm resistor. NC: Not connected or pulled high. X: Don't care

**Pin-46 and pin-45 are internally pulled high by weak resistors.

❶According to AC'97 ver 2.3, the primary mode while RESET# is asserted, if a clock is present at BIT-CLK pin for at least 5 cycles before RESET# is de-asserted, ALC203 is a consumer of BITCLK. ALC203 should use external 12.288MHz BITCLK as its clock source.

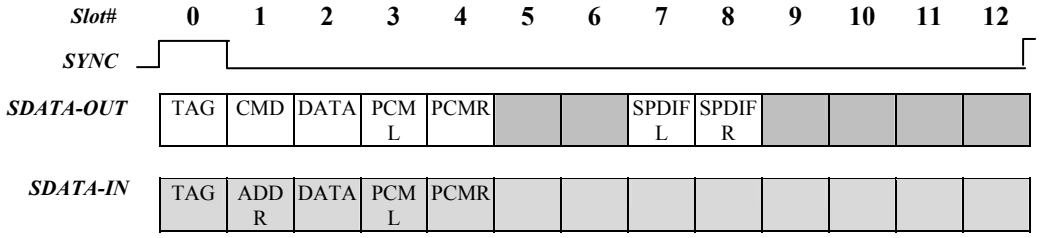
❷Standard secondary mode, ALC203 receive external 12.288MHz clock from BIT-CLK pin.
ALC203 E version and later versions do not support secondary mode as pin-45 is re-defined as Jack-Detect pin 0 (JD0) for auto MIC jack sensing.

9.2 AC-Link

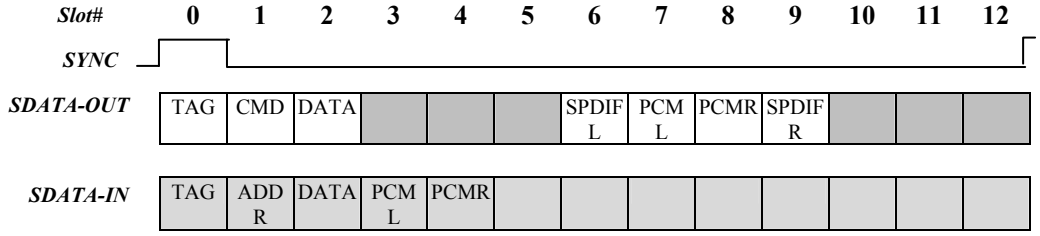
When the ALC203 receives serial data from the AC97 controller, it samples SDATA_OUT on the falling edge of BIT_CLK. When the ALC203 sends serial data to the AC97 controller, it starts to drive SDATA_IN on the rising edge of BIT_CLK.

The ALC203 will return any uninstalled bits or registers with 0 for read operations. The ALC203 also stuffs the unimplemented slot or bit with 0 in SDATA_IN. Note that AC-LINK is MSB-justified.

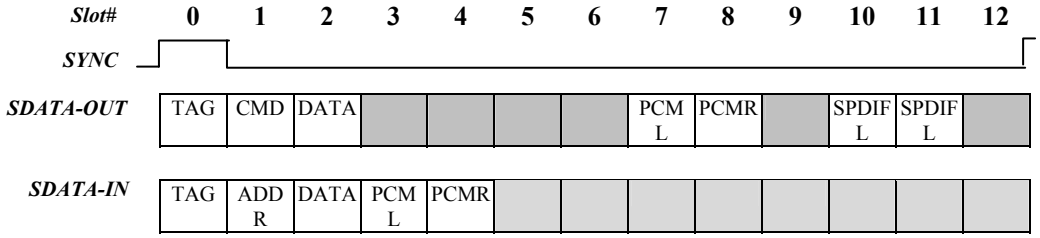
Refer to 'Audio CODEC '97 Component Specification Revision 2.1/2.2/2.3' for details.



Default ALC203 Slot Arrangement – CODEC ID = 00



Default ALC203 Slot Arrangement – CODEC ID = 01,10



Default ALC203 slot arrangement – CODEC ID = 11

9.3 Reset

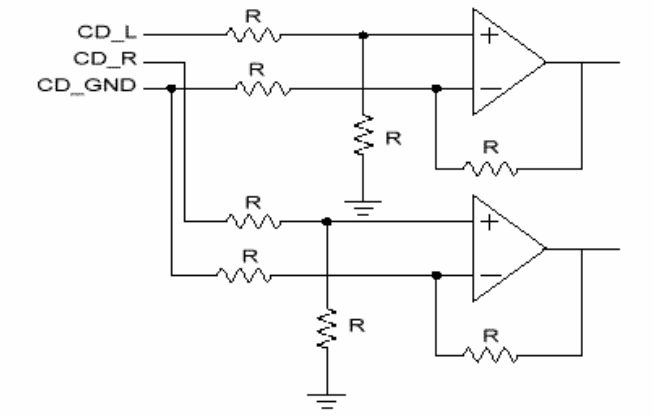
There are 3 types of reset operations: Cold, Register, and Warm.

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to its default value.
Register	Write register indexed 00h	Reset all registers to its default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA_OUT low during the period of RESET# assertion to guarantee that the ALC203 has reset successfully.

9.4 CD Input

It is important to pay attention to differential CD input. Below is an example of differential CD input.



Example of differential CD input

9.5 Odd Addressed Register Access

The ALC203 will return “0000h” when odd-addressed and unimplemented registers are read.

9.6 Power-down Mode

It is important to pay special attention to the power down control register (index 26h), especially PR4 (powerdown AC-link).

9.7 Test Mode

To provide compatibility with AC’97 rev2.2, the ALC203 will float its digital output pins in both ATE and Vendor-Specific test modes. Please refer to AC’97 rev2.2 section 9.2 for a detailed description of the test modes.

9.7.1 ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode, the ALC203 will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

9.7.2 Vendor Specific Test Mode

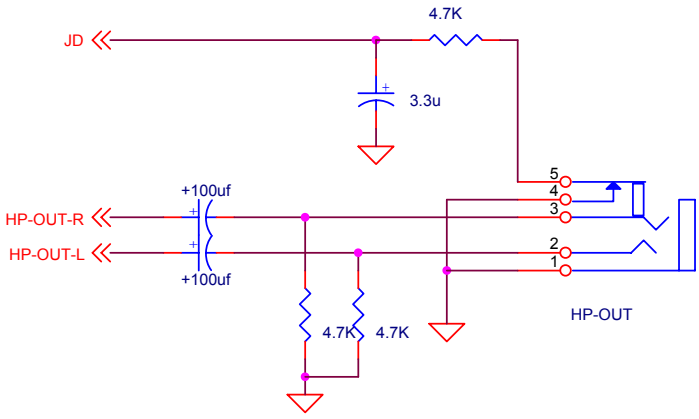
The Vendor Specific Test mode is no longer supported.

9.8 Jack-Detect Function & Assignment for Jack

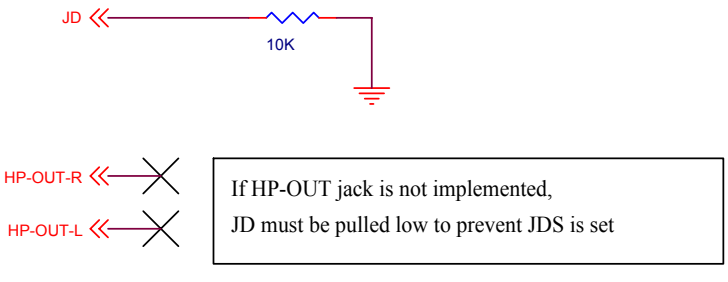
JD (Jack-Detect) is an internal, pulled high input pin used to decide if LINE_OUT should be auto muted. If JDE (Jack Detect Enable) is set and ALC203 detects the JD is floating or pull high (JDS=1), the ALC203 will disable the analog output of LINE_OUT even when the MX02 is not muted.

The first figure below shows an example of jack detect which can implement this function. If no audio plug is inserted in HP_OUT jack, JD is detected as low, and LINE output is normal. If an audio plug is inserted, the ALC203 disables the LINE output, , S/PDIF output, MONO_OUT, HP_OUT. This is useful for some PC applications, such as notebook and home based computers.

If a headphone output jack is not implemented and HP_OUT is kept as floating, once JDE is enabled, LINE_OUT will be muted unless JD is pulled low by a 10KΩ resistor (See second figure below). To resolve this, the Jack-Detect mute LINE_OUT function is disabled after power up (default JDE is 0). This makes the ALC203 compatible with other AC'97 devices. Therefore, it is the responsibility of software to enable this function if headphone jack detection is implemented.



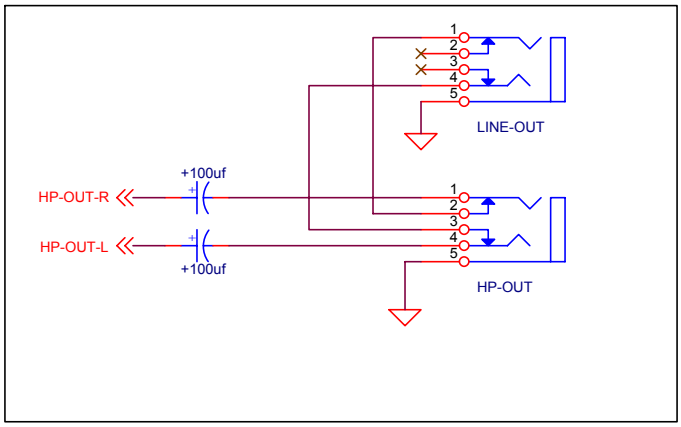
Example of a Jack Detect Circuit



JD is Pulled Low by a 10KΩ Resistor

The figure below shows another simple way to implement the jack detect function without using the JD pin of the ALC203. It is a good circuit for motherboard makers, as it is only a layout issue and no extra components are needed.

Once the HP_OUT jack is plugged in, output signals to LINE_OUT will be isolated, and no signals will be output to the LINE_OUT jack. The only drawback to this plan is that software will not sense that the HP_OUT jack is plugged in. It may be inconvenient for software to pay attention to this special application.



Implementing the Jack-Detect Function Without Using the JD Pin

*To accommodate driver and hardware design, the following Jack-Detect pin assignment is recommended.

For ALC203 D version:
Pin 17(JD1) = for UAJ1 (HP-OUT)
Pin 16(JD2) = for UAJ2 (AUX)
no pin for MIC-IN
Pin 43(GPIO0) = for HP-OUT or LINE-OUT
Pin 44(GPIO1) = for LINE-IN

For ALC203 E and later versions:
Pin 17(JD1) = for UAJ1 (HP-OUT)
Pin 16(JD2) = for UAJ2 (AUX)
Pin 45(JD0) = for MIC-IN
Pin 43(GPIO0) = for HP-OUT or LINE-OUT
Pin 44(GPIO1) = for LINE-IN

9.9 DC Voltage Volume Control

The ALC203 has a 32-step internal volume control that is controlled by the DC voltage applied to the 'DC Vol' pin (pin-33). The volume control input range is from GND to AVDD. A low-speed counter ramp ADC transmits the DC voltage into a 5-bit volume code to attenuate the master volume (real MX02), headphone volume (real MX04) and mono-out volume (real MX06). A higher DC voltage means more attenuation related to output volume. The table below shows the relation between input DC voltage and the 5-bit volume code.

Input DC Voltage	Volume Code	Note	Input DC Voltage	Volume Code	Note
95%=< DC	1F	**DCMute=1**	47%< DC <= 50%	F	
92%< DC <= 95%	1E	DCMute=0	44%< DC <= 47%	E	
89%< DC <= 92%	1D		41%< DC <= 44%	D	
86%< DC <= 89%	1C		38%< DC <= 41%	C	
83%< DC <= 86%	1B		35%< DC <= 38%	B	
80%< DC <= 83%	1A		32%< DC <= 35%	A	
77%< DC <= 80%	19		29%< DC <= 32%	9	
74%< DC <= 77%	18		26%< DC <= 29%	8	
71%< DC <= 74%	17		23%< DC <= 26%	7	
68%< DC <= 71%	16		20%< DC <= 23%	6	
65%< DC <= 68%	15		17%< DC <= 20%	5	
62%< DC <= 65%	14		14%< DC <= 17%	4	
59%< DC <= 62%	13		11%< DC <= 14%	3	
56%< DC <= 59%	12		8%< DC <= 11%	2	
53%< DC <= 56%	11		5%< DC <= 8%	1	
50%< DC <= 53%	10		DC <= 5%	0	DCMute=0

Input DC Voltage is ratio of AVDD (+5VA).

- This 5-bit volume code adds extra attenuation for master volume and headphone volume, the absolute maximum volume is determined by MX02, MX04 and MX06.
  Once the sum of MX value and volume code exceeds 3Fh, the real MX value is 3Fh.
  Example 1: (Normal case)
  MX02=0002h, MX04=0300h, MX06=0001h, Volume Code=2h,
  then Master Volume=0204h, Headphone Volume=0502h, Mono-Out=0003h

  Example 2: (The sum exceeds 3Fh for MX02/MX04, 1Fh for MX06)
  MX02=2F2Fh, MX04=2E2Eh, MX06=0002h, Volume Code=1Eh,
  then Master Volume=3F3Fh, real Headphone Volume=3D3Dh, Mono-Out=001Fh

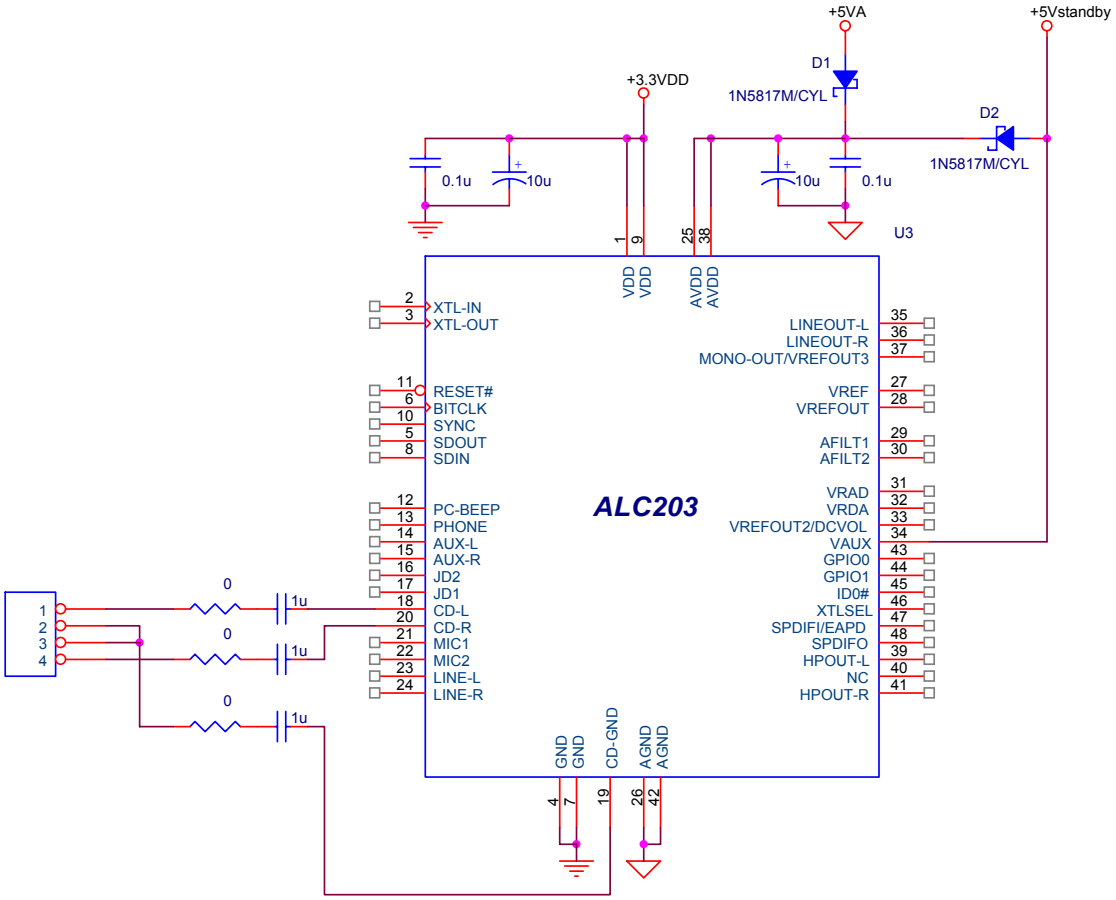
  Example 3: (Volume code is 1Fh, DCMute=1, real MXs should be muted)
  MX02=0000h, MX04=2020h, MX06=0010h, Volume Code=1Fh,
  then Master Volume=9F1Fh, Headphone Volume=BF3Fh, Mono-Out=801Fh

9.10 POWER OFF CD Function

The 'POWER OFF CD' function describes a state where, after the system has been shut down and a +5V analog power is supplied at VAUX(pin-34), the ALC203 will turn on the CD-IN op and output amplifier. It is possible to design a system which will save op-amp circuitry and bypass CD output directly to the speaker.

The figure below indicates the system application circuitry to support the 'POWER OFF CD' function. The operation mode is defined by +3.3VCC and +5Vaux.

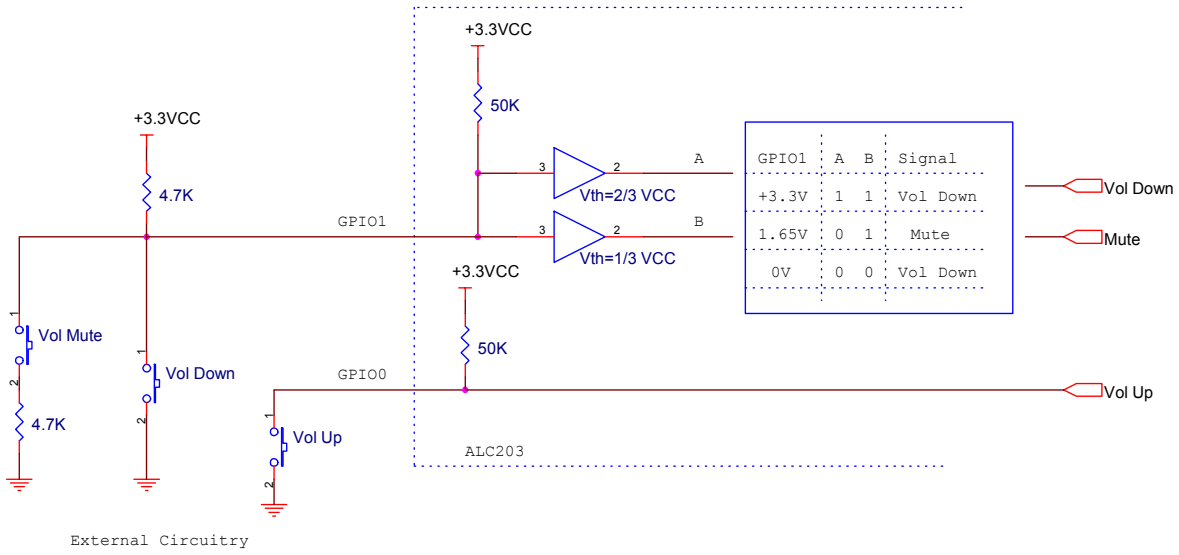
+3.3VCC	+5Vaux	Operation Mode
No (0)	No (0)	Shut Down
No (0)	Yes (1)	Power Off CD
Yes (1)	No (0)	Normal (+5Vaudio must be on)
Yes (1)	Yes (1)	Normal (+5Vaudio must be on)



POWER OFF CD Circuitry

9.11 GPIO Smart Volume Control

A 5-bit volume code is controlled by GPIO0 (volume up) and GPIO1 (volume down) when Smart GPIO Volume Control is selected. The single step and consecutive step (0.11Sec/step) of volume control (up, down and mute) can be implemented by GPIO0 and GPIO1.

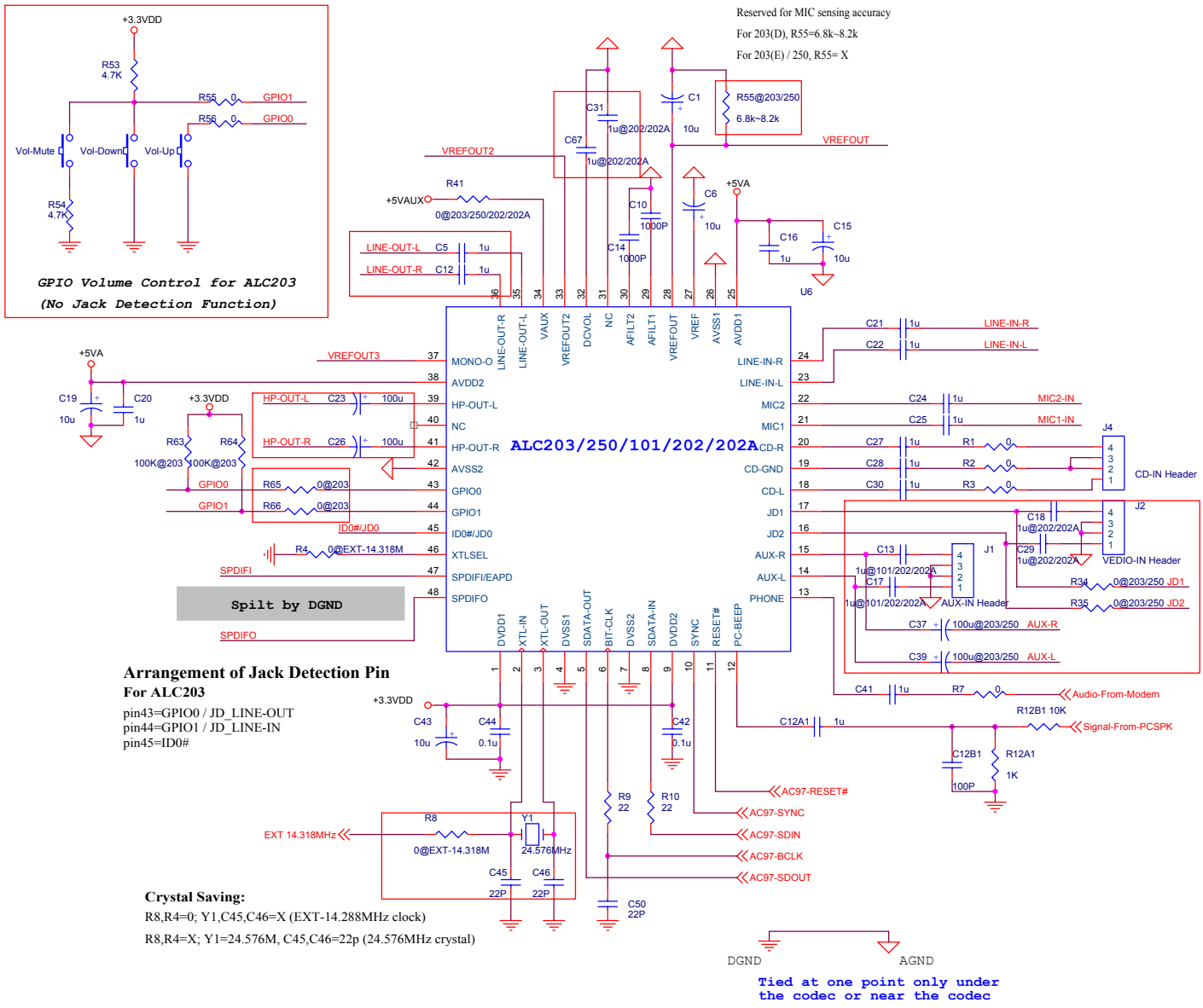


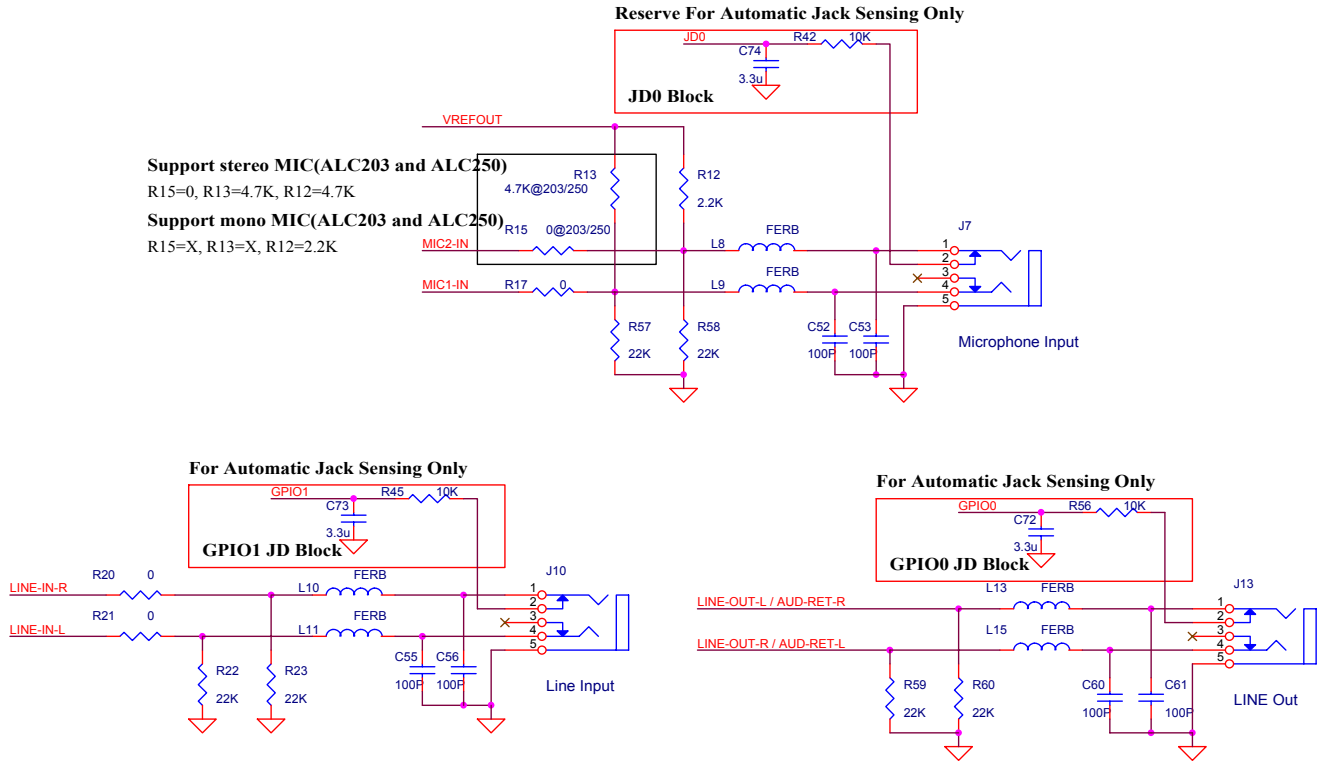
External Circuits for Volume Up/Down/Mute

10. Application Circuit

The application circuit is for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits should be confirmed by Realtek.

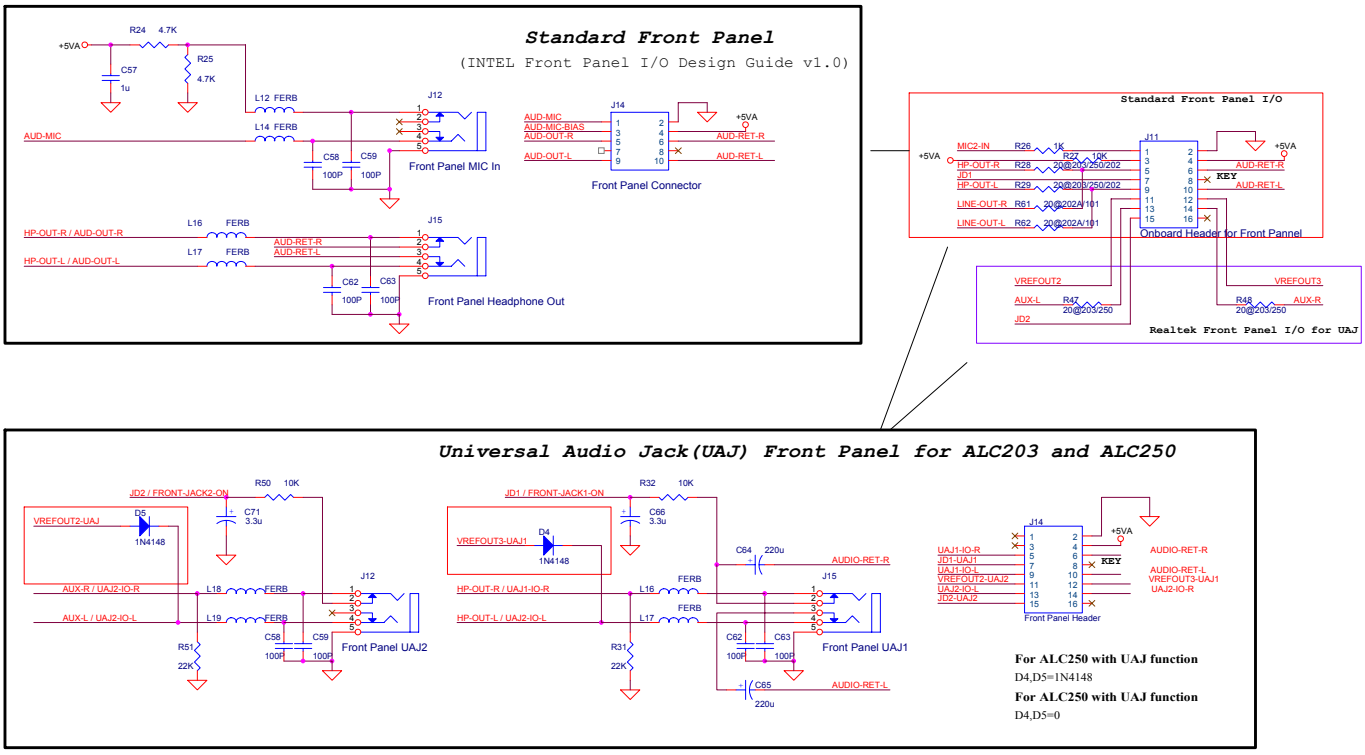
Filter Connection Schematic

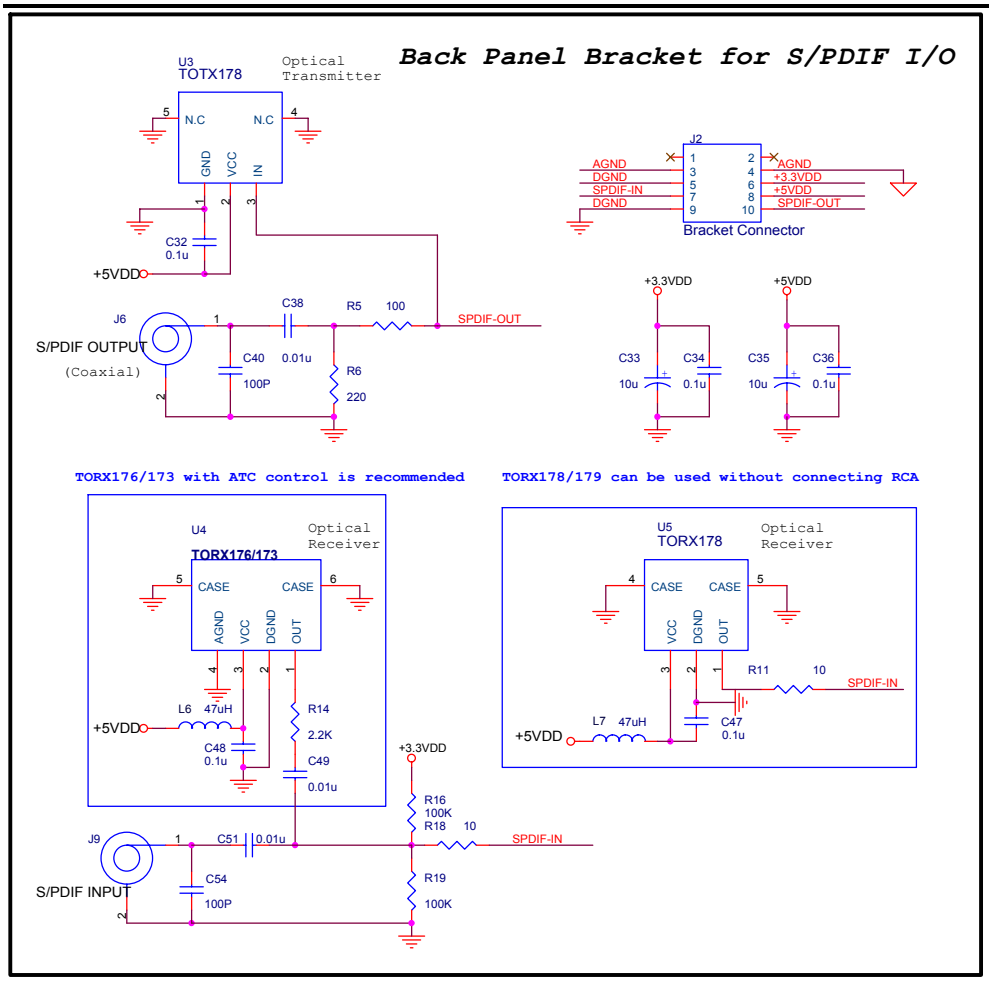




I/O Connection Schematic

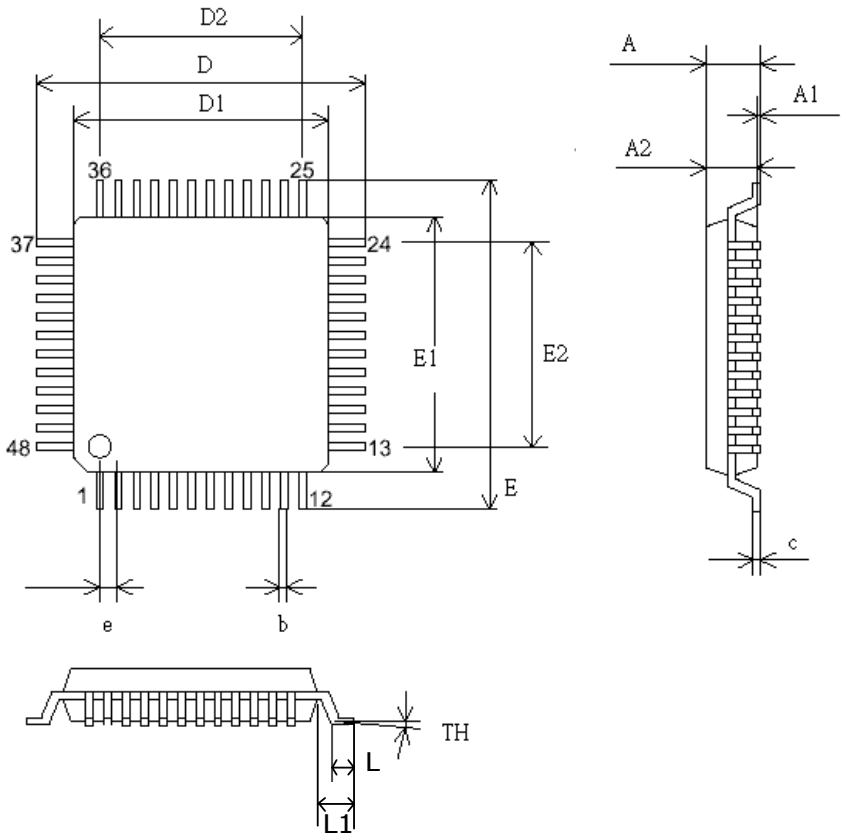
Onboard Header and Reference Front Panel I/O Schematic





Onboard Header and Reference Back Panel Schematic for S/PDIF I/O

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.016 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

12. Ordering Information

Part Number	Package	Status
ALC203	Standard product. LQFP-48	
ALC203-LF	ALC203 with Lead (Pb)-Free LQFP-48 package	

Note 1: See page 4 for lead (Pb)-free package and version identification.

Note 2: Above parts are tested under AVDD =5.0V. If customers have a lower AVDD request, please contact Realtek sales representatives or agents.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw