



REALTEK

ALC861-VD-GR

7.1 CHANNEL HIGH DEFINITION AUDIO CODEC

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC861-VD-GR Audio Codec chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2006/05/24	First release.
1.1	2006/10/18	JDREF resistor must be 20k with 1% accuracy (Table 3, page 6).

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1. General Description

The ALC861 version D (ALC861-VD-GR), 7.1 Channel High Definition Audio codec with UAA (Universal Audio Architecture), features four stereo DACs, one stereo ADC, mixing, mute, and gain control functions to provide an integrated audio solution for multimedia PC systems.

All analog IO (except CD-IN and PCBEEP) are input and output capable, and three headphone amplifiers are also integrated to drive earphones on front and rear panels.

Compared with previous versions of the ALC861, the ALC861-VD-GR features two GPIOs to support customized applications, one EAPD to control an external audio amplifier on laptop platforms, and its HDA bus is scalable IO ready for support of future chipsets.

The ALC861-VD-GR supports S/PDIF output function and a sampling rate of up to 96kHz. It offers easy connection of PCs to high quality consumer electronic products such as digital decoders and speakers.

The ALC861-VD-GR supports host/soft audio from any HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and software utilities like Karaoke mode, environment emulation, software equalizer, and HRTF 3D positional audio, the ALC861-VD-GR provides an excellent entertainment package and game experience for PC users.

2. Features

2.1. *Hardware Features*

- Four Stereo DACs support 16/20/24-bit PCM format for 7.1 channel audio solution
- One stereo ADC supports 16/20/24-bit PCM format
- Front/Surround/Cen/LFE/Side Surround-DACs support independent 44.1k/48k/96kHz sample rate
- ADC supports 44.1k/48k/96kHz sample rate
- All analog jack port (A~H) are stereo input and output re-tasking
- High-quality differential CD input
- Two jack detection pins: each supports detection of up to 4 jacks
- Supports 44.1k/48k/96kHz S/PDIF output
- Supports analog PCBEEP input
- Integrates digital BEEP generator
- Supports two GPIO pins (general purpose input and output)
- Supports EAPD (external amplifier power down) control for external amplifier
- Supports anti-pop mode when analog power AVDD is on and digital power is off
- 48-pin LQFP ‘Green’ package

2.2. *Software Features*

- Meets Microsoft WHQL/WLP 2.0 audio requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio
- Emulation of 26 sound environments to enhance gaming experience
- 10 Software Equalizer Bands
- Voice Cancellation and Key Shifting in Karaoke mode

3. System Applications

- Multimedia PCs
- Information Appliances (IA)

4. Block Diagram

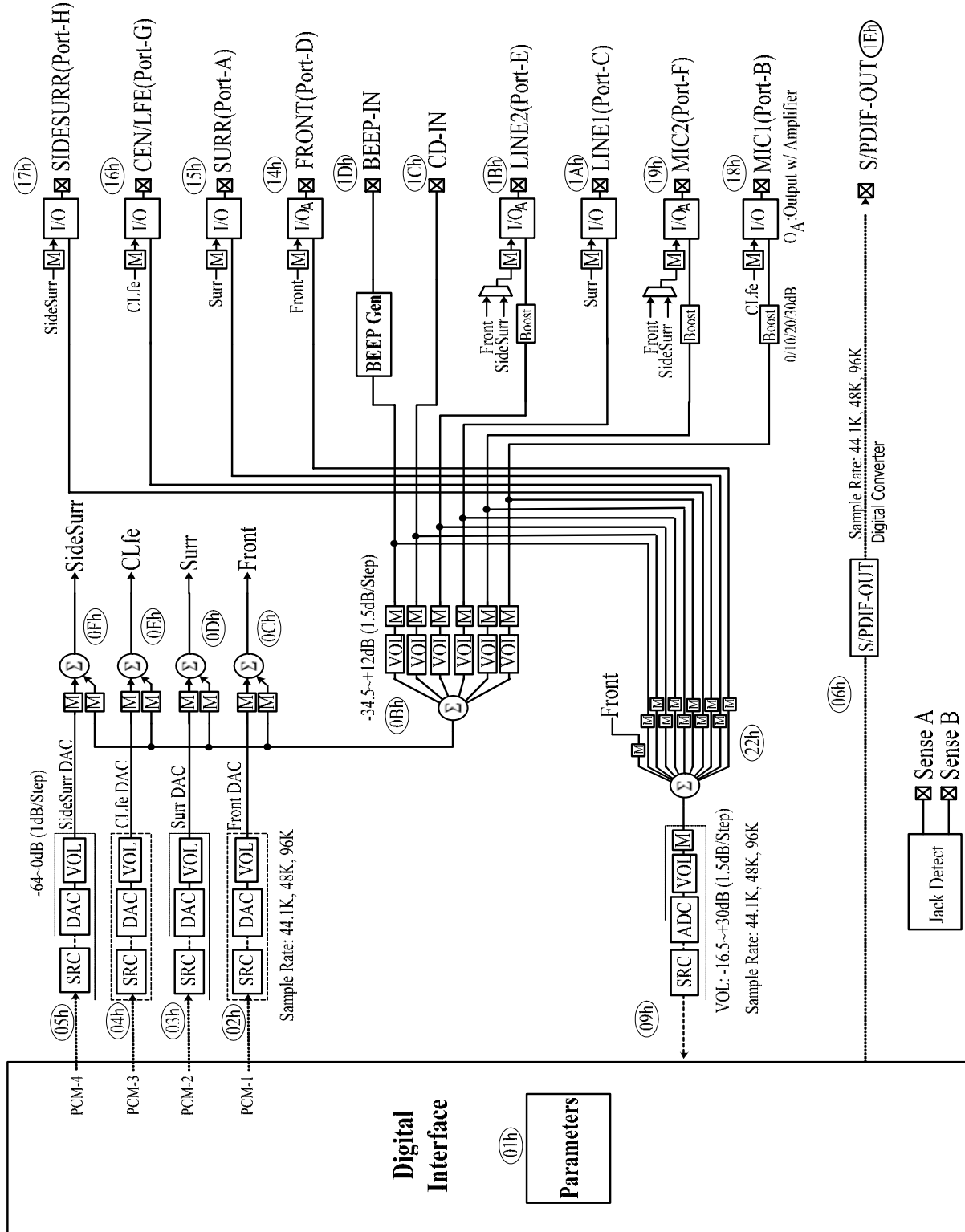


Figure 1. Block Diagram

5. Pin Assignments

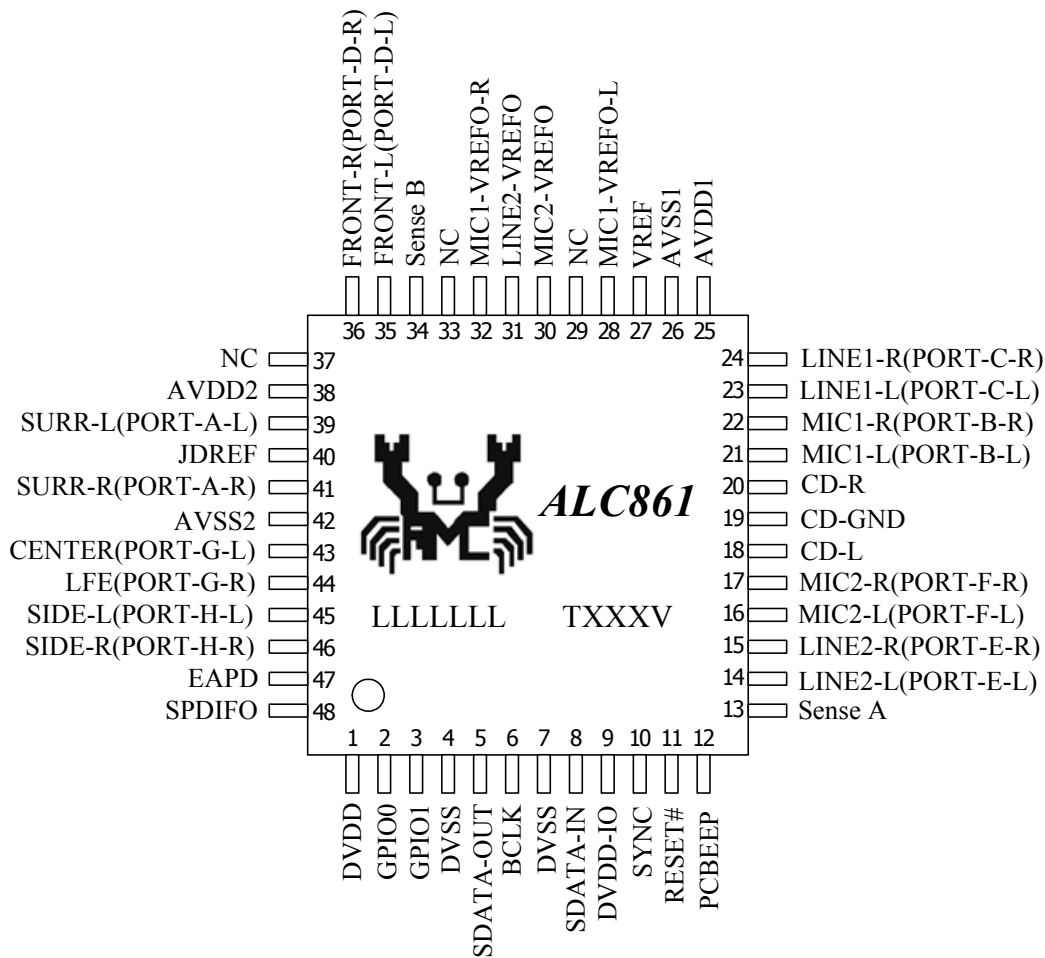


Figure 2. Pin Assignments

5.1. Package and Version Identification

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 2. The version number is shown in the location marked ‘V’.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
RESET#	I	11	H/W reset	$V_i=0.5*DVDDIO$
SYNC	I	10	Sample Sync (48kHz)	$V_i=0.5*DVDDIO$
BCLK	I	6	24MHz Bit clock input	$V_i=0.5*DVDDIO$
SDATA-OUT	I	5	Serial TDM data input	$V_i=0.5*DVDDIO$
SDATA-IN	O	8	Serial TDM data output	In: $V_i=0.5*DVDDIO$; Out: $V_{OH}=DVDDIO, V_{OL}=DVSS$
SPDIFO	O	48	S/PDIF output	TTL output has 12mA@75Ω driving capability
EAPD	O	47	External amplifier power down	$V_{OH}=DVDDIO, V_{OL}=DVSS$
GPIO0	IO	2	General purpose input/output 0	In: $V_i=0.5*DVDD$; Out: $V_{OH}=DVDD, V_{OL}=DVSS$
GPIO1	IO	3	General purpose input/output 1	In: $V_i=0.5*DVDD$; Out: $V_{OH}=DVDD, V_{OL}=DVSS$
				Total: 9 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LINE2-L	IO	14	2 nd line input left channel	Analog input/output. Default is input (JACK-E-L)
LINE2-R	IO	15	2 nd line input right channel	Analog input/output. Default is input (JACK-E-R)
MIC2-L	IO	16	2 nd stereo microphone input left channel	Analog input/output. Default is input (JACK-F-L)
MIC2-R	IO	17	2 nd stereo microphone input right channel	Analog input/output. Default is input (JACK-F-R)
CD-L	I	18	CD input left channel	Analog input. 1.6Vrms of full scale input
CD-GND	I	19	CD input reference ground	Analog input. 1.6Vrms of full scale input
CD-R	I	20	CD input right channel	Analog input. 1.6Vrms of full scale input
MIC1-L	IO	21	1 st stereo microphone input left channel	Analog input/output. Default is input (JACK-B-L)
MIC1-R	IO	22	1 st stereo microphone input right channel	Analog input/output. Default is input (JACK-B-R)
LINE1-L	IO	23	1 st line input left channel	Analog input/output. Default is input (JACK-C-L)
LINE1-R	IO	24	1 st line input right channel	Analog input/output. Default is input (JACK-C-R)
PCBEEP	I	12	External PCBEEP input	Analog input. 1.6Vrms of full scale input
FRONT-L	IO	35	Front output left channel	Analog output (JACK-D-L)
FRONT-R	IO	36	Front output right channel	Analog output (JACK-D-R)
SURR-L	IO	39	Surround out left channel	Analog output (JACK-A-L)
SURR-R	IO	41	Surround out right channel	Analog output (JACK-A-R)
CENTER	O	43	Center output	Analog output (JACK-G-L)
LFE	O	44	Low Frequency output	Analog output (JACK-G-R)

Name	Type	Pin	Description	Characteristic Definition
SIDE-L	O	45	Side Surround output left channel	Analog output (JACK-H-L)
SIDE-R	O	46	Side Surround output right channel	Analog output (JACK-H-R)
Sense A	I	13	Jack Detect pin 1	Jack resistor network input 1
Sense B	I	34	Jack Detect pin 2	Jack resistor network input 2
				Total: 22 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
VREF	-	27	Reference voltage	Typical 2.25V, 10uF capacitor to analog ground
MIC1-VREFO-L	O	28	Bias voltage for MIC1 jack	2.5V/3.2V reference voltage
MIC2-VREFO	O	30	Bias voltage for MIC2 jack	2.5V/3.2V reference voltage
LINE2-VREFO	O	31	Bias voltage for LINE2 jack	2.5V/3.2V reference voltage
MIC1-VREFO-R	O	32	Bias voltage for MIC1 jack	2.5V/3.2V reference voltage
JDREF	-	40	Reference resistor for Jack detection	20K, 1% external resistor to analog ground
				Total: 6 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
AVDD1	I	25	Analog VDD	Analog power for mixer and amplifier
AVSS1	I	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	I	38	Analog VDD	Analog power for DACs and ADCs
AVSS2	I	42	Analog GND	Analog ground for DACs and ADCs
DVDD	I	1	Digital VDD	Digital power for core
DVSS	I	4	Digital GND	Digital ground for core
DVDD-IO	I	9	Digital VDD	Digital power for HDA link
DVSS	I	7	Digital GND	Digital ground for HDA link
				Total: 8 Pins

6.5. NC (Not Connected) Pins

Table 5. Not Connected Pins

Symbol	Type	Pin	Description
NC		29, 33, 37	Not Connected.
			Total: 3 Pins

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 3 shows the basic concept of the HDA link protocol.

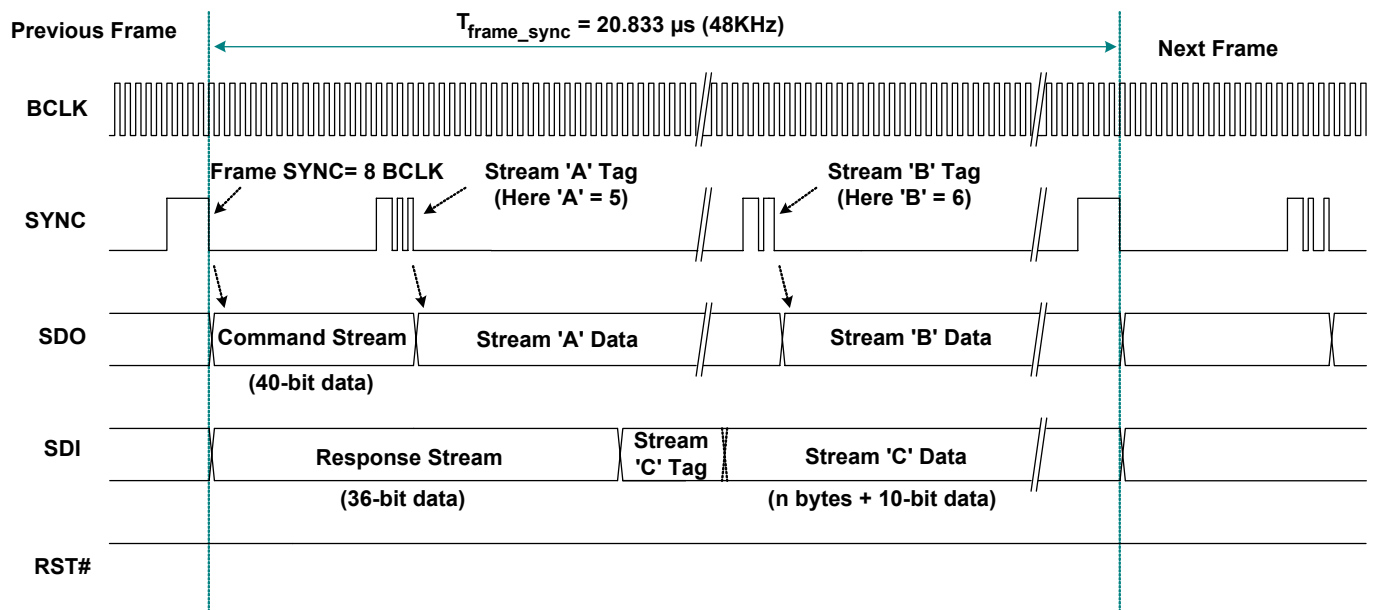


Figure 3. HDA Link Protocol

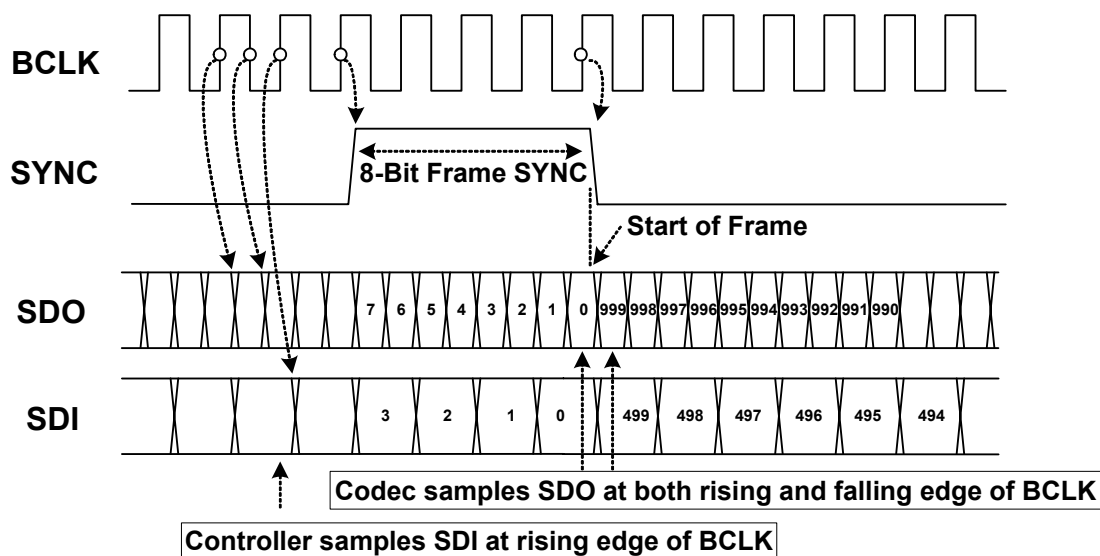
7.1.1. Signal Definitions

Table 6. Link RESET#

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connecting to all codecs.
SYNC	A 48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial Data Output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double-pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial Data Input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI. Up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RESET#	Active low reset signal. Asserted to reset the codec to default power-on state. RESET# is sourced from the HDA controller and connects to all codecs.

Table 7. HDA Signal Definitions

Signal Name	Source	Type for Controller	Description
BCLK	Controller	Output	Global 24.0MHz bit clock.
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal.
SDO	Controller	Output	Serial data output from controller.
SDI	Codec/Controller	Input/Output	Serial data input from codec. Weakly pulled down by the controller.
RESET#	Controller	Output	Global active low reset signal.


Figure 4. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RESET#, BCLK, SYNC, SDO0, and SDO1 are driven by the controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 5, on page 9, shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, and a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 9, describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 5 can be implemented concurrently in an HDA system. The ALC861-VD-GR is designed to receive a single SDO stream.

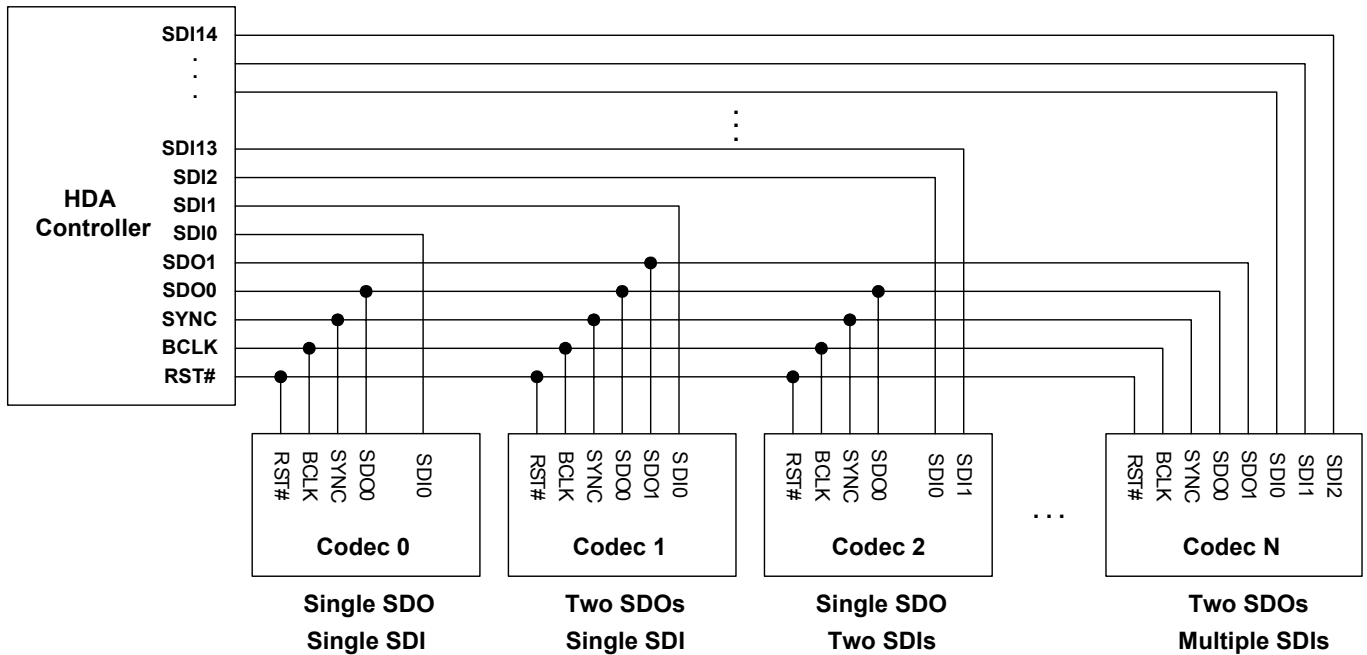


Figure 5. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 6).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 7).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

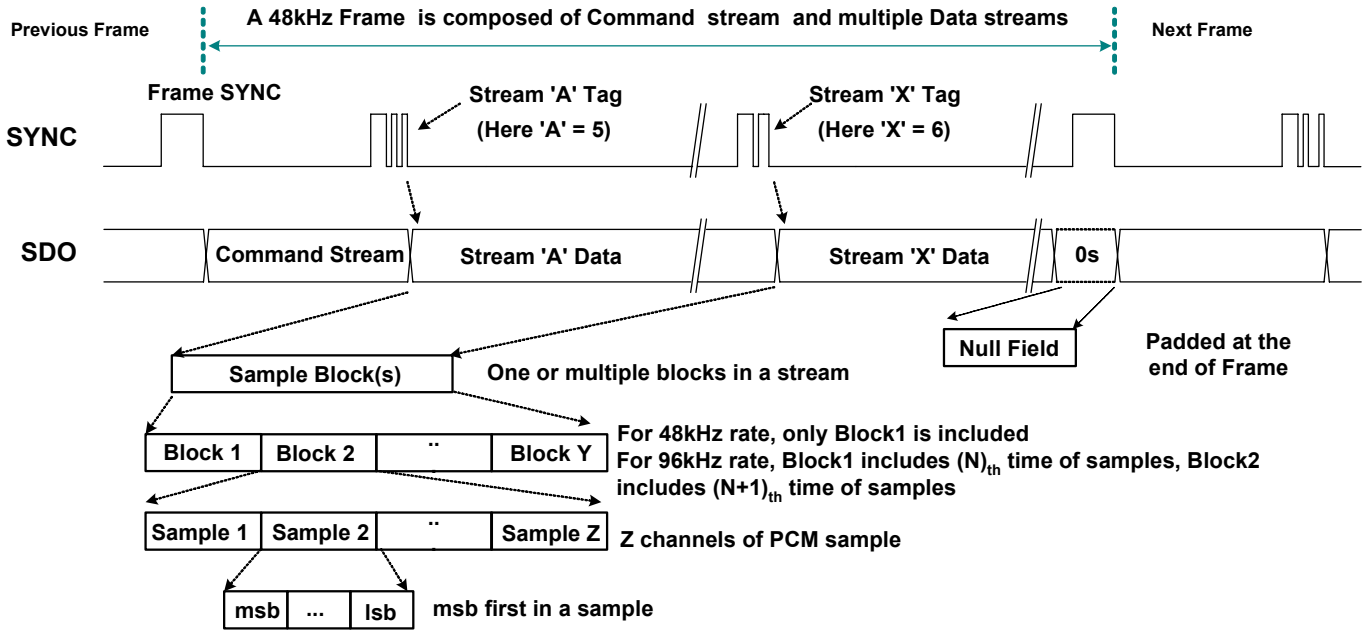


Figure 6. SDO Outbound Frame

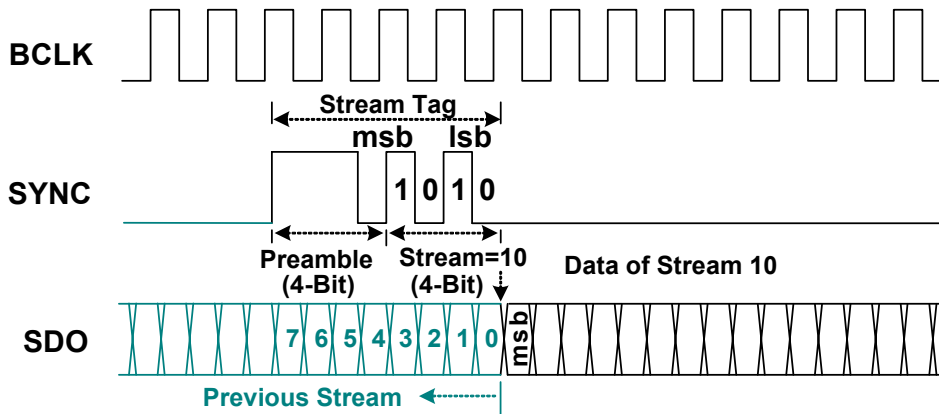


Figure 7. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines that the target codec supports multiple SDO capability, it enables the ‘Stripe Control’ bit in the controller’s Output Stream Control Register to initiate a specific stream (Stream ‘A’ in Figure 8) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To ensure that all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

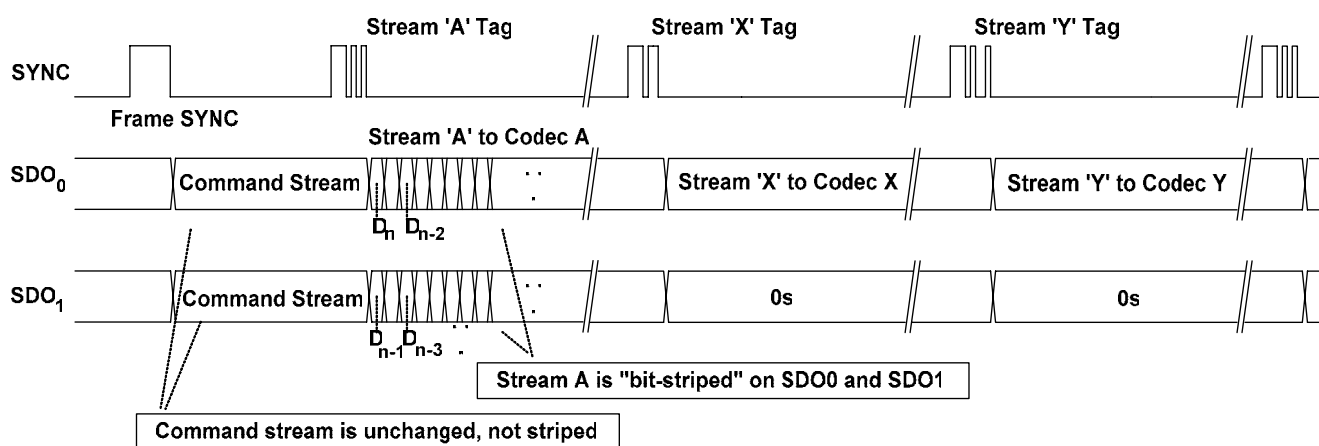


Figure 8. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – Single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 9).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 10).

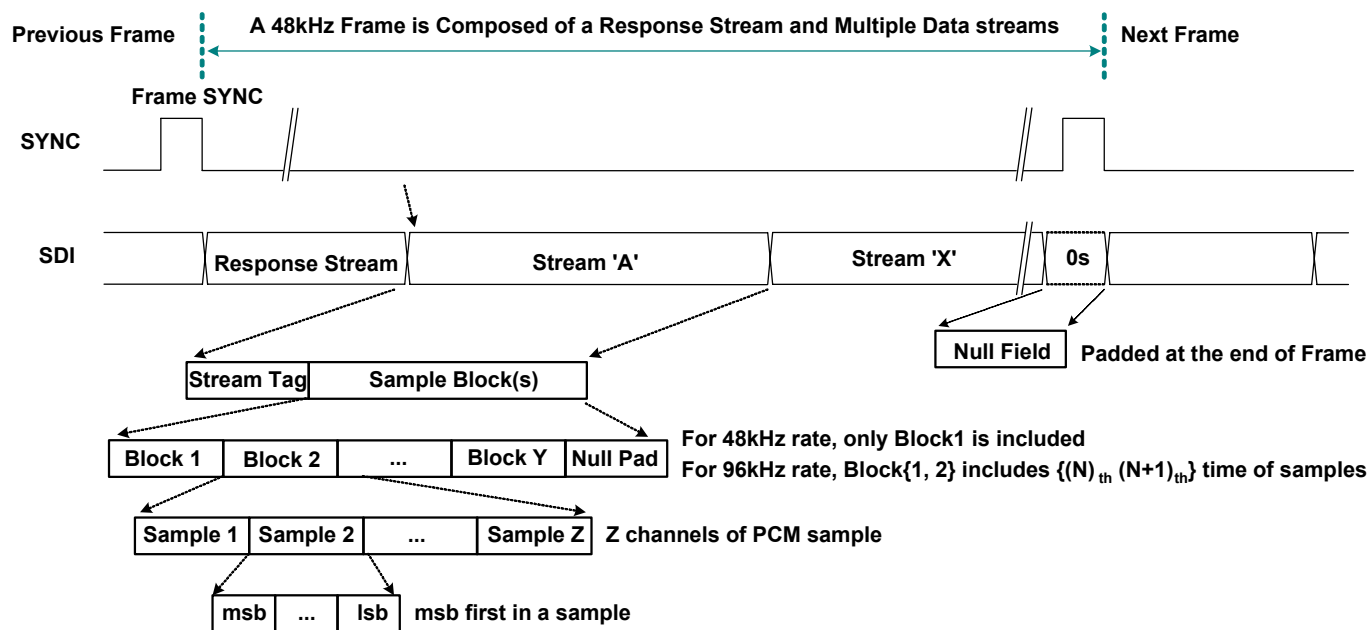


Figure 9. SDI Inbound Stream

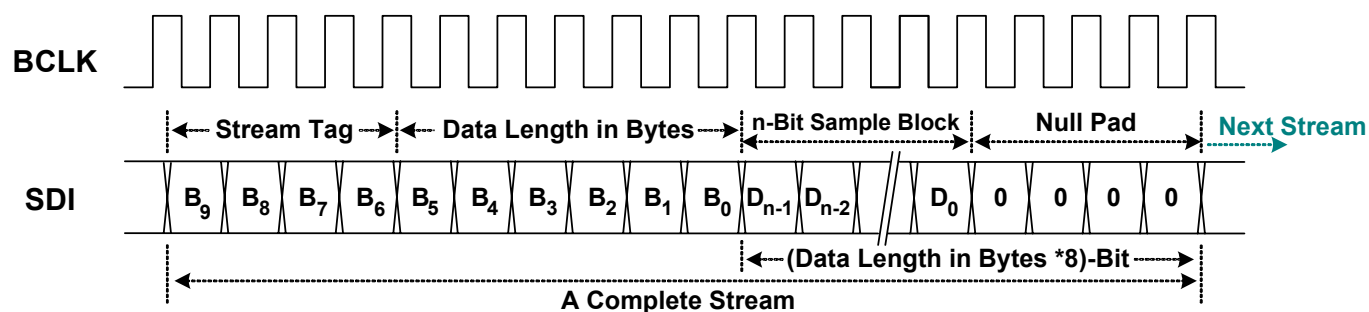


Figure 10. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data onto separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

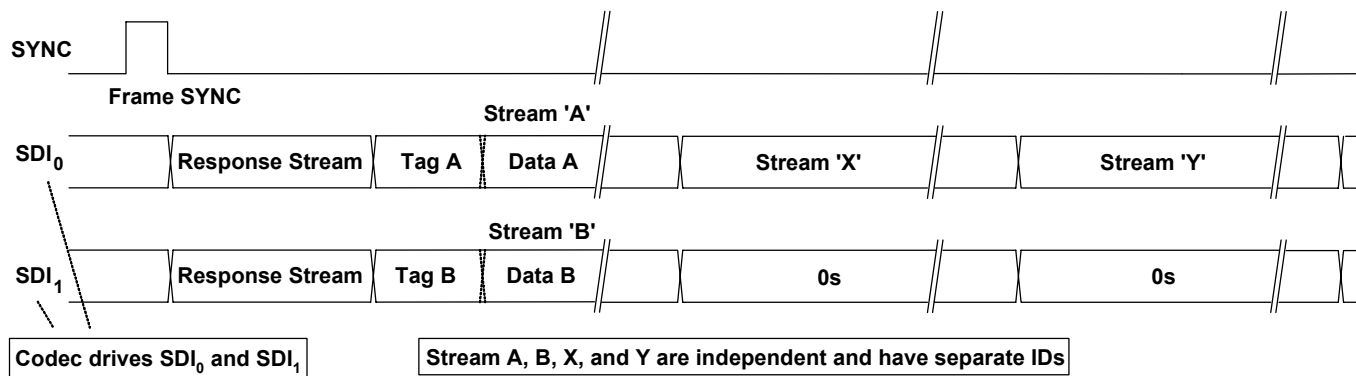


Figure 11. Codec Transmits Data Over Multiple SDI

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable sample rates are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 8, page 14, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 9, page 14, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames. The cadence

“12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)”
interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 10, page 14).

Table 8. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	
1/2		22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 9. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y ² NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y ² (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y ⁴ (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame
 Y: One sample block in a frame
 Y^x: X sample blocks in a frame

Table 10. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} (repeat)
22.05kHz	{12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} {12} {-} {11} {-} {11} {-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² - (repeat)
174.4kHz	12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ - (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNY
 {11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNN
 {-} =NNNN
 22.05kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYNYNYNYNYNY
 {11}=YNY
 {-} =NN

44.1kHz	12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.
88.2kHz	12 ² - =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.
174.4kHz	12 ⁴ - =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- **Link Reset.**
Generated by assertion of the RESET# signal. All codecs return to their power-on state
- **Codec Reset.**
Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset
2. Codec Reset
3. Codec changes its power state, e.g., hot docking a codec to an HDA system

7.3.1. Link Reset

A link reset may be caused by any of the following three events:

1. The HDA controller asserts RESET# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 12, page 16, shows the 'Link Reset' timing including the 'Enter' sequence (①~⑤) and 'Exit' sequence (⑥~⑨)

Enter 'Link Reset':

- ❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ As the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RESET# signal to low, and enters the 'Link Reset' state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

- ❻ If BCLK is re-started for any reason (codec, wake-up event, power management, etc.)
- ❼ Software is responsible for de-asserting RESET# after a minimum of 100 μ s BCLK running time (the 100 μ sec provides time for the codec PLL to stabilize)
- ❽ Minimum of 4 BCLKs after RESET# is de-asserted, the controller starts to signal normal frame SYNC
- ❾ The codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC)

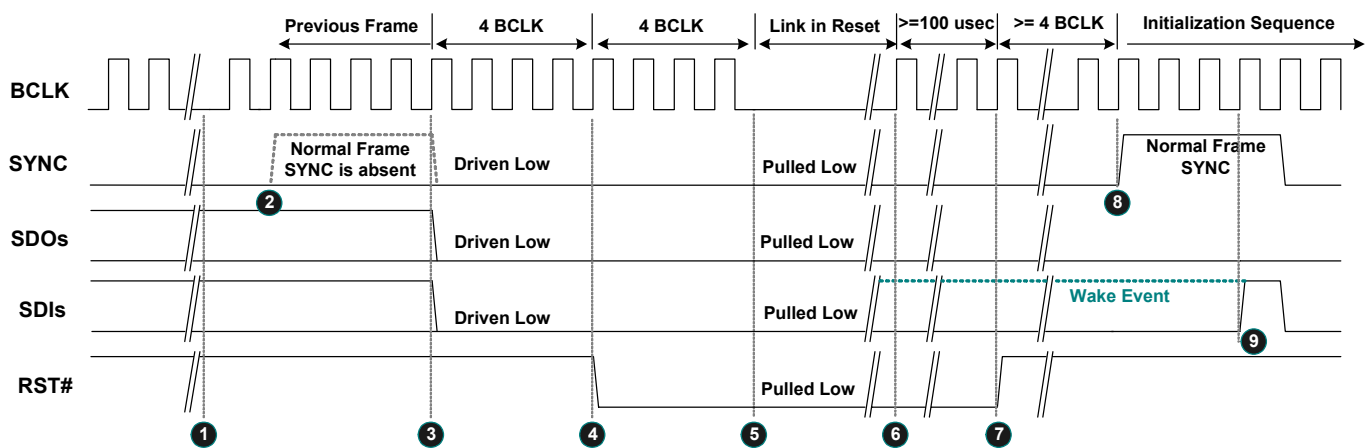


Figure 12. Link Reset Timing

7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec stops driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operating state

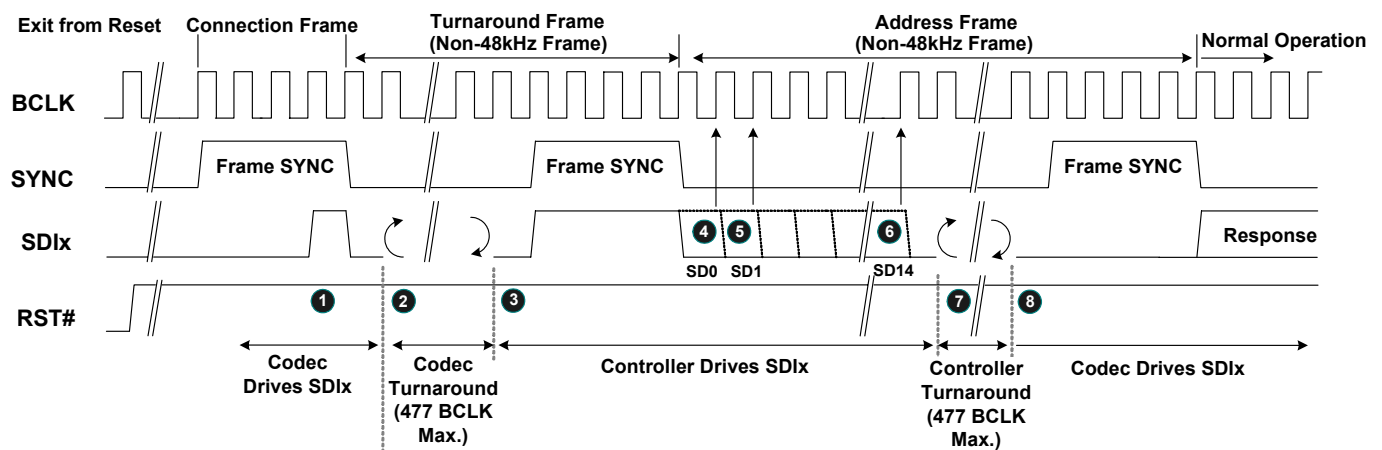


Figure 13. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 11 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 12 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 11. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 12. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The ‘Tag’ in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 13. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 14. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a ‘Valid’ bit to indicate the response is ‘Ready’. Bit-34 is set to indicate that an unsolicited response was sent.

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC861-VD-GR. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget, some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, page 18, for detailed information about supported parameters.

Table 15. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]	32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 16. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format	
Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID)
15:0	Device ID=0862h (ALC861-VD-GR)

Note 1: The Root Node (NID=00h) supports this parameter.

Note 2: For backward compatibility with Realtek's audio function driver, the 'DEVICE ID' is changed to 0862h in order to uniquely identify the ALC861 version D silicon.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 17. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:20	MajRev=1h. The major version number (in decimal) of the HDA Specification
19:16	MinRev=0h. The minor version number (in decimal) of the HDA Specification
15:8	Revision ID. The vendor's revision number <i>Note: 00h indicates ALC861-VD-GR silicon.</i>
7:0	Stepping ID. The vendor's stepping number within the given Revision ID

Note: The Root Node (NID=00h) supports this parameter.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

Table 18. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:16	Starting Node Number The starting node number in the sequential widgets
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes For a root node, this is the total number of function groups in the root node For a function group, this is the total number of widget nodes in the function group

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 19. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's
8	UnSol Capable 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 20. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's
16	Beep Generator A '1' indicates the presence of an integrated Beep generator within the Audio Function Group
15:12	Reserved. Read as 0's
11:8	Input Delay Number of samples delay from analog input to HDA link
7:4	Reserved. Read as 0's
3:0	Output Delay Number of samples delay from HDA link to analog output

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 21. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:20	Widget Type 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets
15:12	Reserved. Read as 0's
11:	L-R Swap 0: Left channel and right channel swapping is not supported 1: Left channel and right channel swapping is supported
10	Power Control 0: Power control is not supported on this widget 1: Power control is supported on this widget
9	Digital 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List 0: Connected to HDA link. No Connection List Entry will be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0
4	Format Override <i>Note: The ALC861-VD-GR supports 16/20/24-bit with 44.1kHz, 48kHz and 96kHz sample rate. The format (parameter ID=0Ah) must be queried</i>
3	AmpParOvr (AMP Param Override) Override amplifier parameters (Gain Control) in individual output Pin Complexes, ADCs, and Mixer widgets
2	OutAmpPre (Out AMP Present)
1	InAmpPre (In AMP Present) There are amplifiers (Gain Control) in individual ADCs and Mixer widgets
0	Stereo 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameters in audio functions provide default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

Table 22. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's
20	B32. 32-bit audio format support 0: Not supported 1: Supported
19	B24. 24-bit audio format support 0: Not supported 1: Supported
18	B20. 20-bit audio format support 0: Not supported 1: Supported
17	B16. 16-bit audio format support 0: Not supported 1: Supported
16	B8. 8-bit audio format support 0: Not supported 1: Supported
15:12	Reserved. Read as 0's
11	R12. 384kHz (=8*48kHz) rate support 0: Not supported 1: Supported
10	R11. 192kHz (=4*48kHz) rate support 0: Not supported 1: Supported
9	R10. 176.4Hz (=4*44.1kHz) rate support 0: Not supported 1: Supported
8	R9. 96kHz (=2*48kHz) rate support 0: Not supported 1: Supported
7	R8. 88.2kHz (=2*44.1kHz) rate support 0: Not supported 1: Supported
6	R7. 48kHz rate support 0: Not supported 1: Supported

Codec Response Format

Bit	Description
5	R6. 44.1kHz rate support 0: Not supported 1: Supported
4	R5. 32kHz (=2/3*48kHz) rate support 0: Not supported 1: Supported
3	R4. 22.05kHz (=1/2*44.1kHz) rate support 0: Not supported 1: Supported
2	R3. 16kHz (=1/3*48kHz) rate support 0: Not supported 1: Supported
1	R2. 11.025kHz (=1/4*44.1kHz) rate support 0: Not supported 1: Supported
0	R1. 8kHz (=1/6*48kHz) rate support 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

Table 23. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's
2	AC3 0: Not supported 1: Supported
1	Float32 0: Not supported 1: Supported
0	PCM 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 24. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description														
31:16	Reserved. Read as 0's														
15:8	VREF Control Capability '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD. <table border="1" data-bbox="347 589 1426 665"> <thead> <tr> <th>7:6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>100%</td> <td>80%</td> <td>Reserved</td> <td>Ground</td> <td>50%</td> <td>Hi-Z</td> </tr> </tbody> </table>	7:6	5	4	3	2	1	0	Reserved	100%	80%	Reserved	Ground	50%	Hi-Z
7:6	5	4	3	2	1	0									
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z									
7	Reserved														
6	Balanced I/O Pin '1' indicates this pin complex has balanced pins														
5	Input Capable '1' indicates this pin complex supports input														
4	Output Capable '1' indicates this pin complex supports output														
3	Headphone Drive Capable '1' indicates this pin complex has an amplifier to drive a headphone														
2	Presence Detect Capable '1' indicates this pin complex can detect whether there is a device plugged in														
1	Trigger Required '1' indicates whether a software trigger is required for an impedance measurement														
0	Impedance Sense Capable '1' indicates this pin complex can perform analog sense on the attached device to determine its type														

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 25. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. ‘0’ means the gain is fixed
7	Reserved. Read as 0
6:0	Offset Indicates which step is 0dB

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 26. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range. Each individual step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates 0.25dB steps. ‘127’ indicates 32dB steps.
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. ‘0’ means the gain is fixed
7	Reserved. Read as 0
6:0	Offset. Indicates which step is 0dB

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 27. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0
7	Short Form 0: Short Form 1: Long Form
6:0	Connect List Length Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (not a MUX widget)

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 28. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's
3	D3Sup 1: Power state D3 is supported
2	D2Sup 1: Power state D2 is supported
1	D1Sup 1: Power state D1 is supported
0	D0Sup 1: Power state D0 is supported

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 29. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's
15:8	NumCoeff. Number of Coefficient
7:1	Reserved. Read as 0's
0	Benign 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 30. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0 The ALC861-VD-GR does not support GPIO wake-up function
30	GPIUnsol=1 The ALC861-VD-GR supports GPIO unsolicited response
29:24	Reserved. Read as 0's
23:16	NumGPIs=00h No GPI pin is supported
15:8	NumGPOs=00h No GPO pin is supported
7:0	NumGPIOs=02h Two GPIO pins are supported

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 31. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

Bit	Description
31:8	Reserved. Read as 0's
7	Delta 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps The number of steps in the range of the Volume Control Knob

Note: The ALC61-VD does not support volume knob and will respond with 0s to this parameter.

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 32. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F01h	0's	Bit[7:0] are Connection Index

Codec Response for NID = 19h (MIC2, PORT-F)

Bit	Description
31:8	0's
7:0	Connection Index currently Set (Default value is 00h) 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Fh Other: Reserved

Codec Response for NID = 1Bh (LINE2, PORT-E)

Bit	Description
31:8	0's
7:0	Connection Index currently Set (Default value is 00h) 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Fh Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 33. Verb – Set Connection Select (Verb ID=701h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]	0's for all nodes

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 34. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F02h	Offset Index - N[7:0]	32-bit Response

Codec Response for NID=09h (ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 22h (Sum Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Bh (Mixer)

Bit	Description
31:24	Connection List Entry (N+3) Returns 1Bh (Pin Complex – LINE2) for N=0~3 Returns 00h for N>3
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Complex – LINE1) for N=0~3 Returns 00h for N>3
15:8	Connection List Entry (N+1) Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7 Returns 00h for N>7
7:0	Connection List Entry (N) Returns 18h (Pin Complex – MIC1) for N=0~3 Returns 1Ch (Pin Complex – CD) for N=4~7 Returns 00h for N>7

Codec Response for NID=0Ch (Front Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 02h (Front DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Dh (Surround Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 03h (Surround DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Eh (Cen/Lfe Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 04h (Cen/Lfe DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Fh (Side-Surr Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 05h (Front DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=14h (FRONT, Port-D)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Ch (Sum Widget NID=0Ch) for N=0~3 Returns 00h for N>3

Codec Response for NID=15h (SURR, Port-D)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Dh (Sum Widget NID=0Dh) for N=0~3 Returns 00h for N>3

Codec Response for NID=16h (CEN/LFE, Port-G)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Eh (Sum Widget NID=0Eh) for N=0~3 Returns 00h for N>3

Codec Response for NID=17h (SIDE, Port-H)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Fh (Sum Widget NID=0Fh) for N=0~3 Returns 00h for N>3

Codec Response for NID=18h (MIC1, Port-B)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Eh (Sum Widget NID=0Eh) for N=0~3 Returns 00h for N>3

Codec Response for NID=19h (MIC2, Port-F)

Bit	Description
31:16	Connection List Entry (N+3), (N+2) Returns 0000h for n>3
15:8	Connection List Entry (N+1) Returns 0Fh (Sum Widget NID=0Fh) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 0Ch (Sum Widget NID=0Ch) for N=0~3 Returns 00h for N>3

Codec Response for NID=1Ah (LINE1, Port-C)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1) Returns 000000h for n>3
7:0	Connection List Entry (N) Returns 0Dh (Sum Widget NID=0Dh) for N=0~3 Returns 00h for N>3

Codec Response for NID=1Bh (LINE2, Port-E)

Bit	Description
31:16	Connection List Entry (N+3), (N+2) Returns 0000h for n>3
15:8	Connection List Entry (N+1) Returns 0Fh (Sum Widget NID=0Fh) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 0Ch (Sum Widget NID=0Ch) for N=0~3 Returns 00h for N>3

Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 06h (S/PDIF-OUT Converter) for N=0~3 Returns 00h for N>3

Codec Response for NID=22h (Sum Widget)

Bit	Description
31:23	Connection List Entry (N+3) Returns 1Bh (Pin Widget LINE2, port-E) for N=0~3 Returns 15h (Pin Widget SURR, port-A) for N=4~7 Returns 00h for n>7
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Widget LINE1, port-C) for N=0~3 Returns 14h (Pin Widget FRONT, port-D) for N=4~7 Returns 00h for N>7
15:8	Connection List Entry (N+1) Returns 19h (Pin Widget MIC2, port-F) for N=0~3 Returns 1Dh (Pin Widget PCBEEP) for N=4~7 Returns 17h (Pin Widget SIDE, port-H) for N=8~11 Returns 00h for N>11
7:0	Connection List Entry (N) Returns 18h (Pin Widget MIC1, port-B) for N=0~3 Returns 1Ch (Pin Widget CD) for N=4~7 Returns 16h (Pin Widget CEN/LFE, port-G) for N=8~11 Returns 00h for N>11

Codec Response for Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 35. Verb – Get Processing State (Verb ID=F03h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F03h	0's	32-bit response

Codec Response for All NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.6. Verb – Set Processing State (Verb ID=703h)

Table 36. Verb – Set Processing State (Verb ID=703h)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]	0's for all nodes	

Codec Response for all NID	
Bit	Description
31:0	0's

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 37. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID=Dh	0's	Bit [15:0] are Coefficient Index	

Codec Response for NID=20h (Realtek Define Registers)	
Bit	Description
31:16	Reserved. Read as 0's
15:0	Coefficient Index

Codec Response for Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 38. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]	0's for all nodes	

Codec Response for All NID	
Bit	Description
31:0	0's

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 39. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Define Registers)

Bit	Description
31:16	Reserved. Read as 0's
15:0	Processing Coefficient

Codec Response for Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 40. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 41. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID=Bh	'Get' payload [15:0]	Bit[7:0] are responsible for 'Get'	

'Get' Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0
13	Get Left/Right 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0's
3:0	Index[3:0] for Input Source Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored.

Codec Response for 02h (FRONT DAC), 03h (SURR DAC), 04h (CEN/LFE DAC) and 05h (SIDE DAC)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. (No Input Amplifier Mute) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0. (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0]. 7-bit step value (0~64) specifying the volume from -64B~0dB in 1dB steps

Codec Response for 09h (ADC)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0. (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from -16.5B~+30dB in 1.5dB steps Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute)

Codec Response for NID=0Bh (MIXER Sum Widget)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0. (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from -34.5dB~+12dB in 1.5dB steps Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute)

Codec Response for NID=0Ch~0Fh (Sum Widget: Front, Surr, Cen/Lfe, Side Sum)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)

Codec Response for NID=14h, 15h, 16h, 17h and 1Ah (Pin Widget: FRONT/SURR/CEN/SIDE/LINE1)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute) Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute, 0:Unmute, 1:Mute (Default=1)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)

Codec Response for NID=18h, 19h and 1Bh (Pin Widget: MIC1/MIC2/LINE2)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute) Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute, 0:Unmute, 1:Mute (Default=1)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0] specifying the boost from 0dB/10dB/20dB/30dB in 10dB per step. (Default=0, 0dB) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)

Codec Response for NID=22h (Sum Widget)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute (Default=1 for all index) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)

Codec Response to Other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 42. Verb – Set Amplifier Gain (Verb ID=3h)
Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp 1: indicates output amplifier gain will be set
14	Set Input Amp 1 indicates input amplifier gain will be set
13	Set Left Amp 1 indicates left amplifier gain will be set
12	Set Right Amp 1 indicates right amplifier gain will be set
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets) 5-bit index offset in connection list is used to select the input gain that will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the 'Set Input Amp' bit is not set
7	Mute 0: Unmute 1: Mute ($-\infty$ gain)
6:0	Gain[6:0] A 7-bit step value specifying the amplifier gain

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 43. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=Ah	0's	Bit[15:0] are converter format

Codec Response for NID=02h~06h (Output Converters: FRONT, SURR, CEN/LFE, SIDE DAC, and S/PDIF-OUT).
 Codec Response for NID=09h (Input Converters: ADC)

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 Not supported. Always read as 000b
7	Reserved. Read as 0
6:4	Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels

Table 44. Get Converter Format Support

	BASE	MULT	DIV	BITS	Sample Rate
NID=02h (Front DAC)	0	000b,001b	000b	001,010b, 011b	48K, 96K
	1	000b	000b	001,010b, 011b	44.1K
NID=03h (Surr DAC)	0	000b,001b	000b	001,010b, 011b	48K, 96K
	1	000b	000b	001,010b, 011b	44.1K
NID=04h (Cen/Lfe DAC)	0	000b,001b	000b	001,010b, 011b	48K, 96K
	1	000b	000b	001,010b, 011b	44.1K
NID=05h (Side DAC)	0	000b,001b	000b	001,010b, 011b	48K, 96K
	1	000b	000b	001, 010b, 011b, 100b	44.1K
NID=06h (S/PDIF-OUT)	0	000b,001b	000b	001,010b, 011b	48K, 96K
	1	000b	000b	001,010b, 011b	44.1K
NID=09h (ADC)	0	000b,001b	000b	001b,010b,	48K, 96K
	1	000b	000b	001b,010b,	44.1K

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 45. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0
6:4	Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h)

Table 46. Verb – Get Power State (Verb ID=F05h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= F05h	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node.

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.16. Verb – Set Power State (Verb ID=705h)

Table 47. Verb – Set Power State (Verb ID=705h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=705h	Power State [7:0]	0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's
5:4	PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node
3:2	Reserved. Read as 0's
1:0	PS-Set. Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 48. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=F06h	0's	Stream & Channel [7:0]

Codec Response for NID=02h~06h (Output Converters: FRONT, SURR, CEN/LFE, SIDE DAC and S/PDIF-OUT)

Codec Response for NID=09h (Input Converters: ADC)

Bit	Description
31:8	Reserved. Read as 0's
7:4	Stream[3:0] The link stream used by the converter. 0000b is unused, 0001b is stream 1, etc.
3:0	Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 49. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's
7:4	Set Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 50. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh, 1Eh

(Pin Widget: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, S/PDIF-OUT)

Bit	Description
31:8	Reserved. Read as 0's
7	H-Phn Enable 0: Disabled 1: Enabled <i>Note: Only for NID=14h(FRONT), 19h(MIC2) and 1Bh(LINE2) support headphone amplifier.</i>
6	Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled <i>Note: NID=1Ch(CD-IN) and 1Dh(PCBEEP) do not support output are always read as 0.</i>
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled <i>Note: NID=1Eh(S/PDIF-OUT) does not support output is always read as 0.</i>
4:3	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled, default for all) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved <i>Note: Only NID=18h, 19h and 1Bh support reference output, other nodes will ignore this verb and response with 0.</i>

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 51. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0]: (NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh, 1Eh)

(Pin Widget: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, S/PDIF-OUT)

Bit	Description
31:8	Reserved. Read as 0's
7	H-Phn Enable 0: Disabled 1: Enabled <i>Note: Only for NID=14h(FRONT), 19h(MIC2) and 1Bh(LINE2) support headphone amplifier.</i>
6	Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled <i>Note: NID=1Ch(CD-IN) and 1Dh(PCBEEP) don't support output are always read 0.</i>
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled <i>Note: NID=1Eh(S/PDIF-OUT) does not support output are always read 0.</i>
4:3	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled, default for all) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved <i>Note: Only NID=18h, 19h, and 1Bh support reference output, other nodes will ignore this verb and response with 0.</i>

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real time event.

Table 52. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID= F08h	0's	32-bit Response	

Codec Response for NID=01h (GPIO), 14h~1Bh (Port jack detection)

Bit	Description
31:8	Reserved. Read as 0's
7	Unsolicited Response is Enabled 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's
3:0	Assigned Tag for Unsolicited Response The tag[3:0] is assigned by software to determine which widget generates unsolicited responses

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

Table 53. Verb – Set Unsolicited Response Control (Verb ID=708h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]	0's for all nodes

'EnableUnsol' in Command Bit [7:0]

Bit	Description
31:8	Reserved. Read as 0's
7	Unsolicited Response 0: Disable 1: Enable
6	Reserved. Read as 0's
5:0	Tag for Unsolicited Responses. Tag[5:0] is defined by software to assign a 6-bit tag for nodes that are enabled to generate unsolicited responses.

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 54. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID= F09h	0's	32-bit Response

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh

(Pin Widget: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2)

Bit	Description
31	Presence Detect Status 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance The ALC861-VD-GR does not support hardware impedance detect. This field is read as 0s.

Codec Response for other NID

Bit	Description
31:0	Not supported (returns 00000000h)

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 55. Verb – Execute Pin Sense (Verb ID=709h)

Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID= 709h	Right Channel[0]	0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's
0	Right (Ring) Channel Select 0: Sense Left channel (Tip) 1: Sense Right channel (Ring) The ALC861-VD-GR does not support hardware impedance detect and will ignore this control bit.

8.25. Verb – Get Configuration Default (Verb ID=F1Ch/F1Dh/F1Eh/F1Fh)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 56. Verb – Get Configuration Default (Verb ID=F1Ch/F1Dh/F1Eh/F1Fh)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=Xh	Verb ID= F1Ch	0's	32-bit Response

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh, 1Eh

(Pin Widget: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, S/PDIF-OUT)

Bit	Description
31:0	32-bit configuration information for each pin widget

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions (e.g., placement and expected default device) for the Pin Widgets NID=0B~0Fh, 10h, 11h, 1Fh, 20h, and 12h.

**Table 57. Verb – Set Configuration Default Bytes 0, 1, 2, 3
(Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)**

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]	0's for all nodes	

Note: Supported by Pin Widget NID=14~1Bh, 1Ch, 1Dh and 1Eh. Other widgets will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 58. Verb – Get BEEP Generator (Verb ID= F0Ah)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
CAd=X	Node ID=Xh	Verb ID= F1Bh	0's	Divider [7:0]	

'Response' for NID=23h

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$ The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$ A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input

Codec Response for Other NID

Bit	Description
31:0	0's

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 59. Verb – Set BEEP Generator (Verb ID= 70Ah)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=23h	Verb ID=71Bh	Divider [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$ The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$ A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input

Note: All nodes except BEEP generator (NID=23h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.29. Verb – Get GPIO Data (Verb ID= F15h)

Table 60. Verb – Get GPIO Data (Verb ID= F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Data The value written (output) or sensed (input) on the corresponding pin if it is enabled

Codec Response for Other NID

Bit	Description
31:0	0's

8.30. Verb – Set GPIO Data (Verb ID= 715h)

Table 61. Verb – Set GPIO Data (Verb ID= 715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Output Data The value written determines the value driven on a pin that is configured as an output pin

Codec Response for All NID

Bit	Description
31:0	0's

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 62. Verb – Get GPIO Enable Mask (Verb ID= F16h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=F16h	0's

Codec Response Format

Response [31:0]
EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Enable mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 63. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=01h	Verb ID=716h	Enable Mask [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Enable Mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 64. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=01h	Verb ID=F17h	0's	Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 65. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=01h	Verb ID=717h	Direction [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.35. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 66. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=01h	Verb ID=F19h	0's	UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Unsolicited Enable mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.36. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 67. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=01h	Verb ID=719h	UnsolEnable [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's

8.37. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

Table 68. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd=X	Node ID=06h	Verb ID=F0Dh/ F0Eh	0's	Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=07h (S/PDIF-OUT Converter) Response to 'Get verb' – F0Dh (Control for SIC bit[15:0])

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's
15	Reserved. Read as 0's
14:8	CC[6:0] (Category Code)
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's

8.38. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 69. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Dh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=06h	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Eh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=06h	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=07h (S/PDIF-OUT Converter)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

'Payload' in Set Control 2 for NID=07h (S/PDIF-OUT Converter)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's
6:0	CC[6:0] (Category Code)

8.39. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/D22h/F23h)

32-bit Read/Write register for Audio Function Group (NID=01h)

Table 70. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd = X	Node ID=01h	Verb ID=F20h	0s	32-bit Response

Codec Response for NID=01h

Bit	Description
31:16	Subsystem ID[23:8]. (Default=10ECh)
15:8	Subsystem ID[7:0]. (Default=08h).
7:0	Assembly ID[7:0]. (Default=62h).

8.40. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Table 71. Verb – Set Subsystem ID [31:0]
(Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd = X	Node ID=01h	Verb ID=723h, 722h, 721h, 720h	Label [7:0]	0s for all nodes

Codec Response for all NID

Bit	Description
31:0	0's

8.41. Verb – Get/Set EAPD Control (Verb ID=F0Ch for Get, 70Ch for Set)

Table 72. Verb – Get EAPD Control (Verb ID=F0Ch)

Get Command Format (NID=14h and 15h)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=F0Ch	0s

Codec Response Format

Response [31:0]
Bit[1] is EAPD Control

Codec Response for NID=14h (FRONT, port-D) and 15h (SURR, port-A)

Bit	Description
31:3	Reserved
2	L-R Swap The ALC861-VD-GR does not support swapping left and right channels. Read as 0.
1	EAPD Value 0: EAPD pin state is low 1: EAPD pin state is high
0	BTL Enable The ALC861-VD-GR does not support BTL output. Read as 0.

Codec Response for Other NID

Bit	Description
31:0	0's

Table 73. Verb – Set EAPD Control (Verb ID=70Ch)

Set Command Format (NID=14h and 15h)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=70Ch	Bit[1] is EAPD Control

Codec Response Format

Response [31:0]
0s

Payload in Set command for NID=14h (FRONT, port-D) and 15h (SURR, port-A)

Bit	Description
31:3	Reserved
2	L-R Swap The ALC861-VD-GR does not support swapping left and right channels. Read as 0.
1	EAPD Value 0: EAPD pin state is low 1: EAPD pin state is high. <i>Note: Only one physical logic for the EAPD signal.</i>
0	BTL Enable The ALC861-VD-GR does not support BTL output. Read as 0.

Codec Response

Bit	Description
31:0	0's

8.42. Verb – Function Reset (Verb ID=7FFh)

Table 74. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01h)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=7FFh	0's

Codec Response Format

Response [31:0]
0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's

Note: The Function Reset command causes all widgets to return to their power-on default state.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 75. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply:					
Digital power for core	DVDD	3.0	3.3	3.6	V
Digital power for HDA link	DVDD-IO*	1.5	3.3	3.6	V
Analog	AVDD**	3.3	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts			+125	°C
ESD (Electrostatic Discharge)					
Susceptibility Voltage					
All Pins				4000V	

Note*: The digital link power DVDD-IO must be lower than the digital core power DVDD.

Note** : The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Realtek technical support representatives for special testing support..

9.1.2. Threshold Voltage

DVDD=3.3V±5%, T_{ambient}=25°C, with 50pF external load.

Table 76. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V _{in}	-0.30	-	DVDD +0.30	V
Low Level Input Voltage (HDA link)	V _{IL}	-	-	0.30* DVDDIO	V
High Level Input Voltage (HDA link)	V _{IH}	0.65* DVDDIO	-	-	V
Low Level Input Voltage (S/PDIF-OUT)	V _{IL}	-	-	0.44*DVDD (1.45)	V
High Level Input Voltage (S/PDIF-OUT)	V _{IH}	0.56* DVDD (1.85)	-	-	V
High Level Output Voltage	V _{OH}	0.9*DVDD	-	-	V
Low Level Output Voltage	V _{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	μA
Output Leakage Current (Hi-Z)	-	-10	-	10	μA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	100k	Ω

9.1.3. S/PDIF Output Characteristics

DVDD= 3.3V, $T_{\text{ambient}}=25^{\circ}\text{C}$, with 75Ω external load.

Table 77. S/PDIF Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 78. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	μs
RESET# Inactive to BCLK Startup delay for PLL ready time	T_{PLL}	20	-	-	μs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time

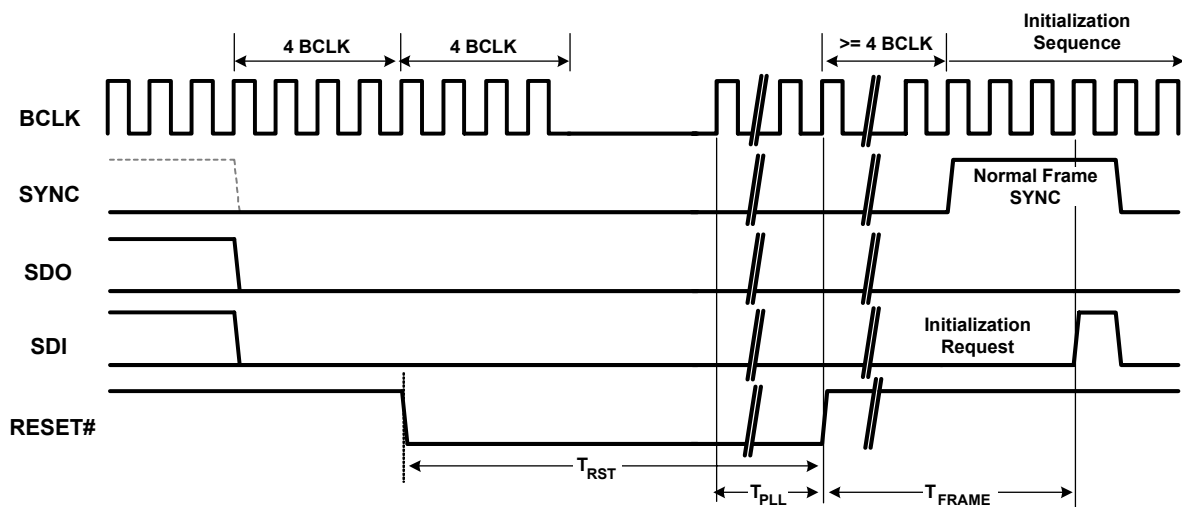
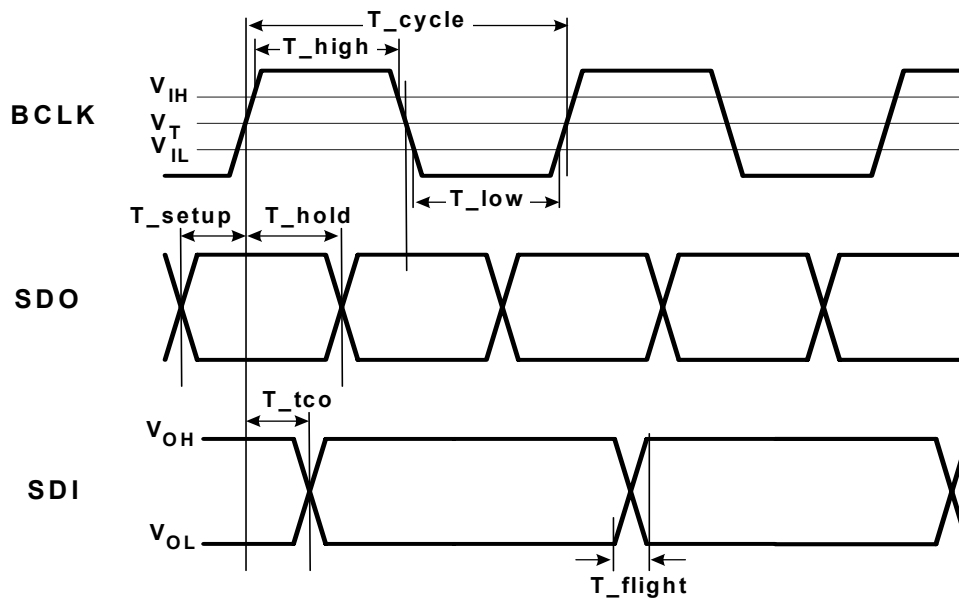


Figure 14. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 79. Link Timing Parameters at the Codec

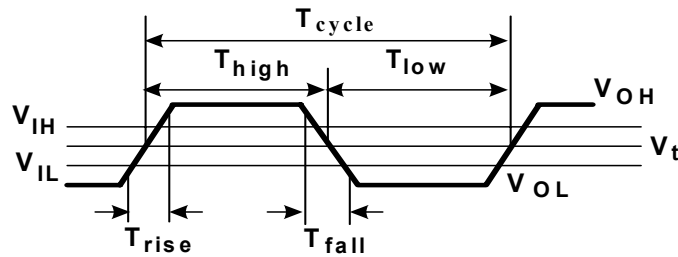
Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency		-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	T_{low}	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1: 50pF external load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns


Figure 15. Link Signal Timing

9.2.3. S/PDIF Output Timing

Table 80. S/PDIF Output Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency	-	-	3.072	-	MHz
S/PDIF-OUT Period	T_{cycle}	-	325.6	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns


Figure 16. Output Timing

9.2.4. Test Mode

Codec test mode and Automatic Test Equipment (ATE) mode are not supported.

9.3. Analog Performance

- Standard Test Conditions
- $T_{\text{ambient}}=25^{\circ}\text{C}$, DVDD= 3.3V $\pm 5\%$, AVDD=5.0V $\pm 5\%$
 - 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
 - 10K Ω /50pF load; Test bench Characterization BW: 10Hz~22kHz

Table 81. Analog Performance

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
All Inputs (gain=0dB)	-	1.6	-	Vrms
All ADC	-	1.2	-	Vrms
Full Scale Output Voltage				
All DAC	-	1.4	-	Vrms
S/N (A Weighted)				
All ADC	-	85	-	dB FSA
All DAC	-	95	-	dB FSA
THD+N				
ADC	-	-80	-	dB FS
All DAC	-	-90	-	dB FS
Frequency Response				
ADC (-3dB lower edge, -1dB higher edge)	10	-	20,000	Hz
DAC (-3dB lower edge, -1dB higher edge)	10	-	20,000	Hz
Pass band ripple for DAC and ADC	-0.20	-	+0.20	dB
Power Supply Rejection Ratio		-40		dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
20dB Gain is Selected	18	20	22	dB
Crosstalk Between Input Channels	-	-80		dB
Input Impedance (gain=0dB)		47		K Ω
Output Impedance				
Line Output		100		Ω
Amplified Output		-	1	Ω
Power Supply Current (normal operation)				
AVDD=5V / DVDD=3.3V	-	TBD	-	mA
Power Supply Current (power down mode)				
AVDD=5V / DVDD=3.3V	-	TBD	-	μA
VREFOUTx Output Voltage	-	2.5	-	V
VREFOUTx Output Current		5		mA

10. Application Circuits

Please contact Realtek to get the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications should be confirmed by Realtek. Realtek may update the latest application circuits onto our web site (www.realtek.com.tw) without modifying this data sheet.

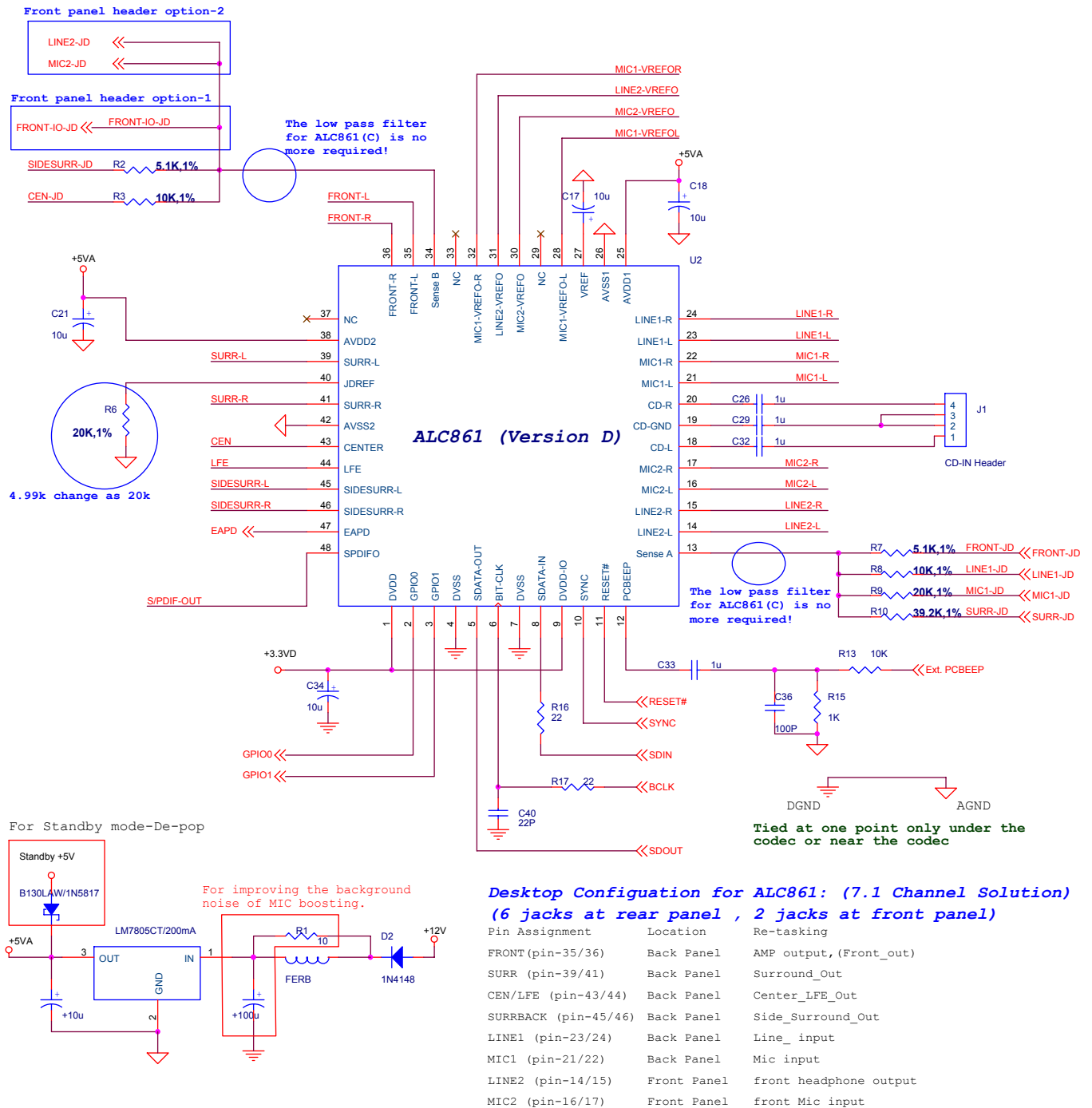


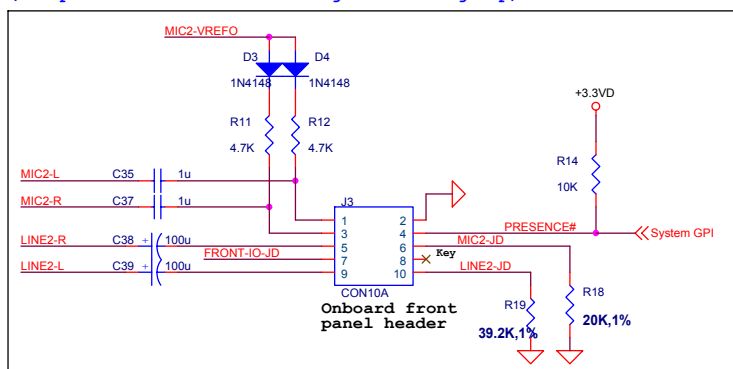
Figure 17. Filter Connection

The ALC861-VD-GR is pin-to-pin compatible with previous ALC861 versions and any board designed with previous versions of the ALC861 can utilize the ALC861-VD-GR directly.

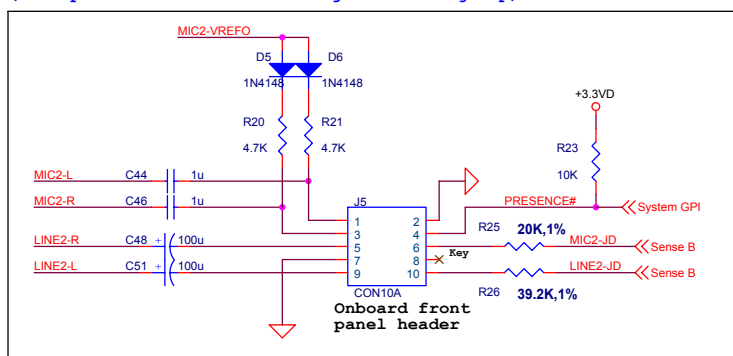
Figure 17, page 66, indicates the main different filter connections between previous ALC861 versions and the ALC861-VD-GR. The main items are listed below:

- (1) The JDREF resistor at pin 40 is changed to 20kΩ with 1% accuracy
- (2) The low-pass filters at Sense A (Pin 13) and Sense B (pin 34) are no longer required
- (3) The filter and jack detection circuits inside the ALC861-VD-GR have been modified to the same as that in other ALC series HD Audio Codecs, e.g., the ALC882 and ALC883

Option 1: Follow Intel's HD Audio front panel header design
(Two ports must be in the same jack detect group)



Option 2: A more flexible front panel header
(Each port can be in different jack detect group)



HD Audio Front Panel I/O Cable

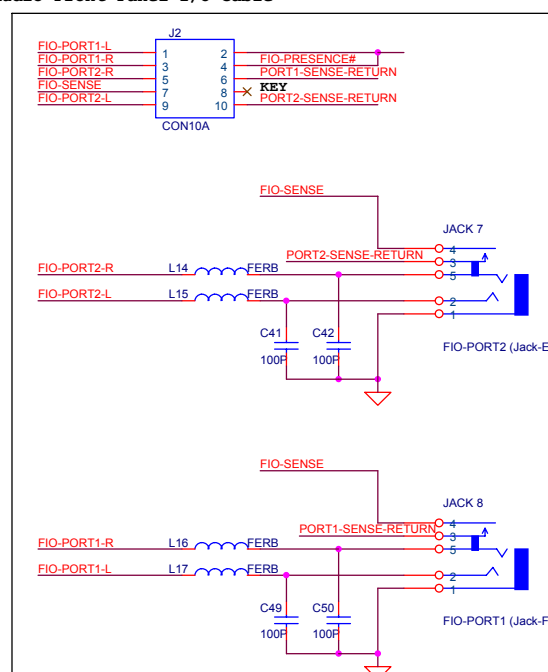


Figure 18. Front Panel Header Connection

Figure 18 shows an optional front panel header design (Option 2) that is also compatible with standard front panel I/O cable. The option 1 follows Intel's front panel IO connectivity design guide, the drawback is that the ports connected to the front panel must use the same jack detection pin. According to the HD Audio standard specification, ports A/B/C/D use 'Sense A'; ports E/F/G/H use 'Sense B' as the jack detect pin. This creates difficulties should the system integrator wish to use port-A (pin 39/41) and port-F (pin 16/17) as the front panel ports, as 'Sense A' and 'Sense B' cannot be tied together.

The option 2 header design allows any two ports to use any sense pin, and is compatible with current HD Audio front panel cabling.

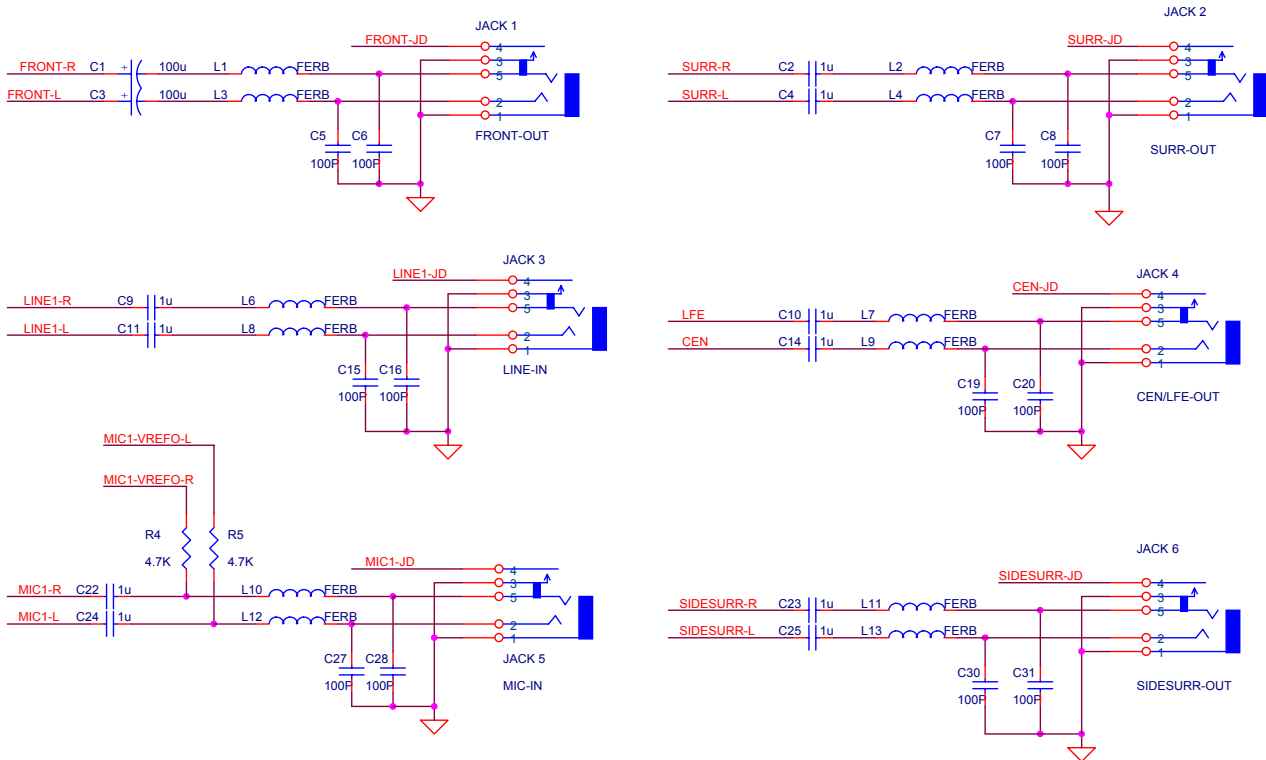
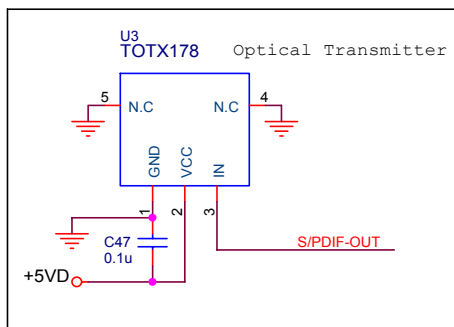


Figure 19. Jack Connection on Rear Panel

S/PDIF module option 1: Optical



S/PDIF module option 2: Coaxial

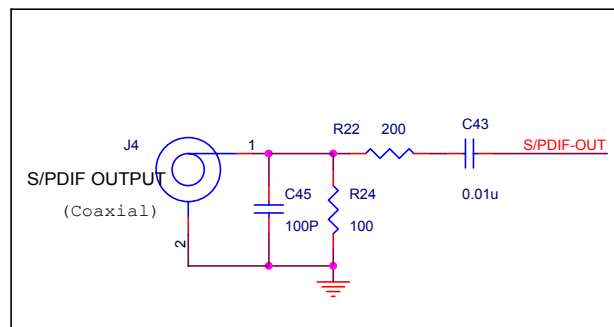
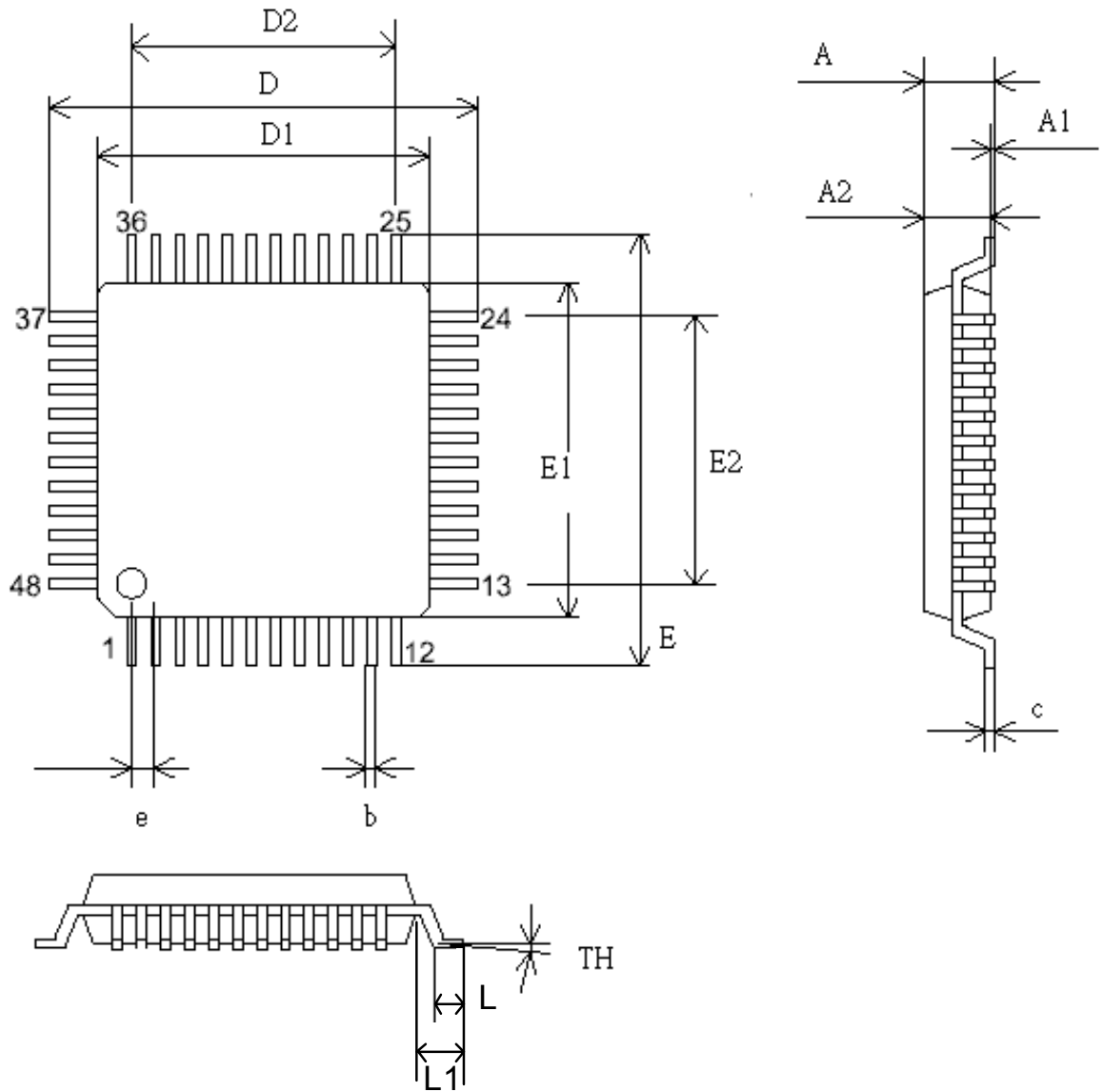


Figure 20. S/PDIF Output Connection

11. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

11.1. Mechanical Dimensions Notes

SYMBOL	MILLIMETER			INCH		
	MIN.	TYP	MAX.	MIN.	TYP	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm)		
PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKG-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

12. Ordering Information

Table 82. Ordering Information

Part Number	Package	Status
ALC861-VD-GR	LQFP-48 'Green' package	MP

Note 1: See page 4 for Green package and version identification.

Note 2: Above parts are tested under AVDD=5.0V. If customers have lower AVDD request, please contact Realtek sales representatives or agents.

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