

REALTEK

ALC880 Series

7.1 CHANNEL HIGH DEFINITION AUDIO CODEC

DATASHEET

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REALTEK

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC880(D) Audio Codec chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

| Revision | Release Date | Summary |
|----------|--------------|---|
| 1.0 | 2004/07/10 | First release. |
| 1.1 | 2004/08/30 | Add Power-Off CD control pin assignment information (Pin 33) |
| 1.2 | 2004/11/12 | 1. Power-Off CD mode not supported in ALC880-VH, ALC880D-VH, ALC880-VH-LF, ALC880D-VH-LF 2. Parameter ‘subsystem ID’ is read as 0s (Table 19, page 22) 3. Verb ‘subsystem verb’ is supported (Table 74, page 64, and Table 75, page 64) |
| 1.3 | 2005/01/25 | Add lead (Pb)-free and version package identification information on page 5 and in Table 84, on page 74. |
| 1.4 | 2005/09/01 | Update ordering information (see Table 84, on page 74). |

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1. General Description

The ALC880* and ALC880D** 7.1 Channel High Definition Audio codecs with UAA (Universal Audio Architecture), featuring four 24-bit two-channel DACs and three stereo 20-bit ADCs, are designed for high performance multimedia PC systems. The ALC880(D) incorporates proprietary converter technology to achieve 95dB sound quality; easily meeting PC2001 requirements and also bringing PC sound quality closer to consumer electronic devices.

The ALC880(D) provides 7.1 output channels, along with flexible mixing, mute, and fine gain control functions to provide a complete integrated audio solution for PCs. The DACs (with a highest sampling frequency of 192kHz) and Realtek proprietary hardware content protection are applicable for DVD-Audio, previously only implemented in high-end consumer electronics, and now achieved by PCs with the ALC880(D) inside. The ALC880(D) also integrates three stereo ADCs that can support a microphone array with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology simultaneously, significantly improving recording quality for conference calls. With this feature (3 stereo ADCs), the ALC880(D) can provide high-quality audio using S/PDIF to output analog data, or for multiple-source recording applications.

Realtek's proprietary impedance sensing and jack detect techniques allow device loads on inputs and outputs to be auto-detected. All analog IO are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched depending on the connected device type (Universal Audio Jack®).

The ALC880(D) supports 32-bit S/PDIF input and output functions and a sampling rate of up to 96kHz, offering easy connection of PCs to high quality consumer electronic products such as AC-3 decoders/speakers, and mini disk devices.

The ALC880(D) supports host/soft audio from the Intel ICH6 chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like Karaoke mode, environment emulation, software equalizer, HRTF 3D positional audio, and optional Dolby® Digital Live, the ALC880(D) provides an excellent entertainment package and game experience for PC users.

**Note: The ALC880 series covers all products listed in section 12 Ordering Information, page 74.*

***Note: D indicates Dolby Digital Live (software feature)*

2. Features

2.1. Hardware Features

- High-performance DACs with 95dB S/N ratio
- ADCs with S/N ratio greater than 85dB
- Meets performance requirements for audio on PC2001 systems
- 8 DAC channels support 16/20/24-bit PCM format for 7.1 audio solution
- 3 stereo ADCs support 16/20-bit PCM format, two for microphone array, one for legacy mixer recording
- Supports 44.1/48/96/192kHz DAC sample rate
- All ADCs support 44.1/48/96 kHz sample rate
- Applicable for 4-channel/192kHz and 6-channel/96kHz DVD-Audio solutions
- Up to four channels of microphone input are supported for AEC/BF application
- High-quality differential CD input
- Supports Power-Off CD function (ALC880/ALC880-LF & ALC880D/ALC880D-LF only)
- Supports external PCBEEP input and built-in BEEP generator
- PCBEEP Pass-Through when link is in RESET state (ALC880/ALC880-LF & ALC880D/ALC880D-LF only)
- Software selectable 2.5V/3.75V VREFOUT
- Six VREFOUTs are supported
- Two GPI (General Purpose Input) jack detection pins (each designed to detect 4 jacks)
- 16/20/24-bit S/PDIF-OUT supports 44.1/48/96kHz sample rate
- 16/20/24-bit S/PDIF-IN supports 44.1/48/96kHz sample rate
- Optional EAPD (External Amplifier Power Down) supported
- Power support: Digital: 3.3V; Analog: 3.3V/5.0V
- Power management and enhanced power saving features
- Compatible with AC'97
- 48-pin LQFP package (lead (Pb)-free package also available)
- Reserve analog mixer architecture for backward compatibility with AC'97
- -64dB ~ +30dB with 1dB resolution of mixer gain for finer volume control
- Impedance sensing capability for each re-tasking jack
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifier for each re-tasking jack
- Supports external volume knob control
- Supports 2 GPIOs (General Purpose Input/Output) for customized applications
- Hardware de-scrambling for DVD-Audio Content protection

2.2. Software Features

- Meets Microsoft WHQL/WLP 2.0 audio requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio
- Emulation of 26 sound environments to enhance gaming experience
- 10 Software Equalizer Bands
- Voice Cancellation and Key Shifting in Karaoke mode
- Realtek Media Player
- Enhanced Configuration Panel and device sensing wizard to improve user experience
- Microphone Acoustic Echo Cancellation (AEC) and Beam Forming (BF) technology for voice application
- Mono/Stereo Microphone noise suppression
- ALC880D features Dolby® Digital Live output for consumer equipment

3. System Applications

- Multimedia PCs
- 3D PC Games
- Information Appliances (IA)
- Voice Recognition
- Audio Conferencing

4. Block Diagram

ALC880 - High Definition Audio (HDA) Codec

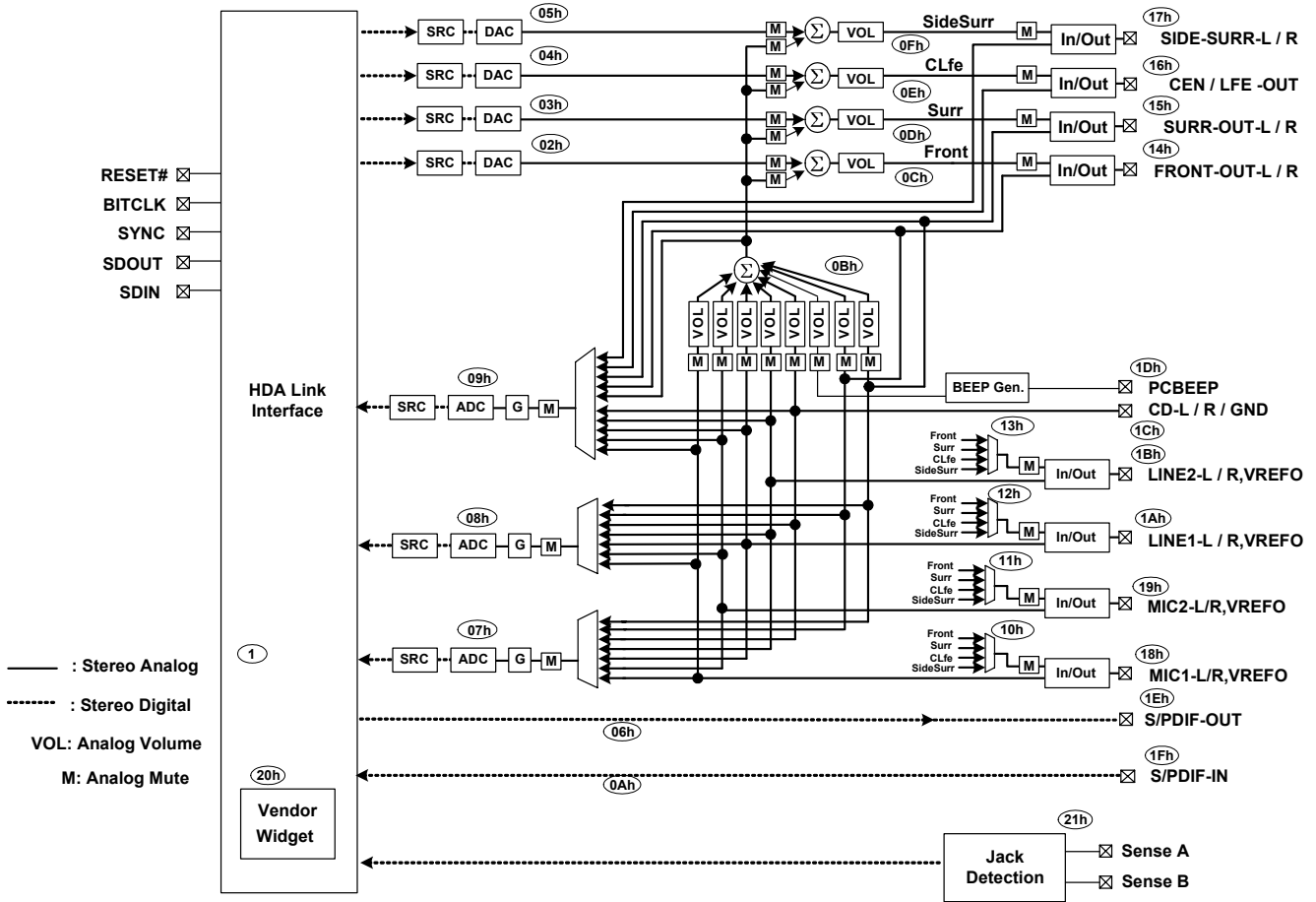


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin Complex widgets NID=14h~1Bh re-tasking IO.

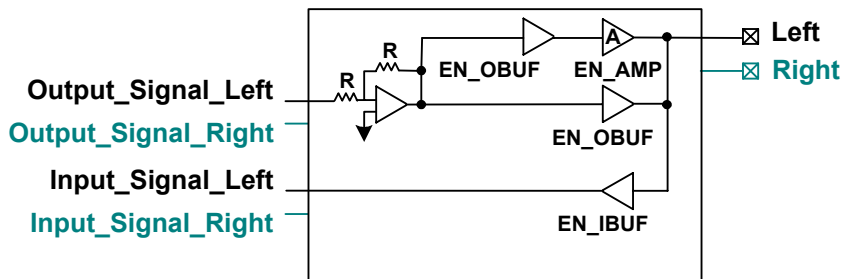


Figure 2. Analog Input/Output Unit

5. Pin Assignments

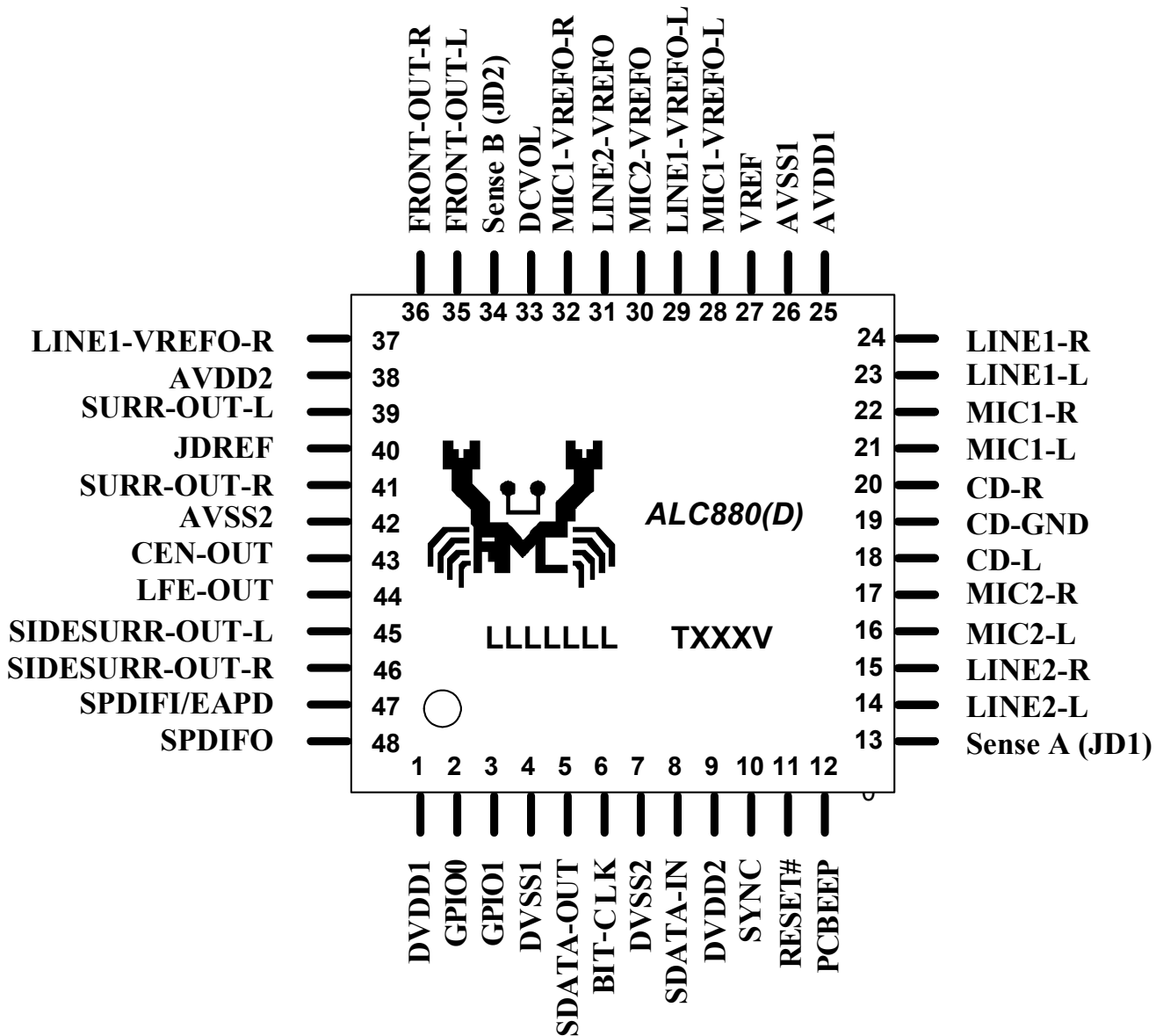


Figure 3. Pin Assignments

5.1. Lead (Pb)-Free Package and Version Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'V'.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

| Name | Type | Pin No. | Description | Characteristic Definition |
|------------------|------|---------|--|---|
| RESET# | I | 11 | H/W reset | Schmitt trigger input, $V_{IL}=1.0V$, $V_{IH}=2.0V$ |
| SYNC | I | 10 | Sample Sync (48kHz) | Schmitt trigger input, $V_{IL}=1.0V$, $V_{IH}=2.0V$ |
| BITCLK | I | 6 | 24MHz Bit clock input | Schmitt trigger input, $V_{IL}=1.0V$, $V_{IH}=2.0V$ |
| SDATA-OUT | I | 5 | Serial TDM data input | Schmitt trigger input, $V_{IL}=1.0V$, $V_{IH}=2.0V$ |
| SDATA-IN | O | 8 | Serial TDM data output | Schmitt output, $V_{OH}=0.9*DVDD$, $V_{OL}=0.1*DVDD$ |
| SPDIFI / EAPD | I/O | 47 | S/PDIF Input/ Signal to power down ext. amp | Schmitt input ($V_{IL}=1.45V$, $V_{IH}=1.85V$) / TTL output |
| SPDIFO | O | 48 | S/PDIF output | TTL output has 12mA@75Ω driving capability |
| GPIO0 | I/O | 2 | General Purpose Input/Output 0 | Schmitt input/output, $V_{IL}=1.45V$, $V_{IH}=1.85V$ |
| GPIO1 | I/O | 3 | General Purpose Input/Output 1 | Schmitt input/output, $V_{IL}=1.45V$, $V_{IH}=1.85V$ |
| | | | | Total: 9 Pins |

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

| Name | Type | Pin No. | Description | Characteristic Definition |
|-----------------|------|---------|--|---|
| LINE2-L | IO | 14 | 2 nd line input left channel | Analog input/output. Default is input (JACK -E) |
| LINE2-R | IO | 15 | 2 nd line input right channel | Analog input/output. Default is input (JACK -E) |
| MIC2-L | IO | 16 | 2 nd stereo microphone input left channel | Analog input/output. Default is input (JACK -F) |
| MIC2-R | IO | 17 | 2 nd stereo microphone input right channel | Analog input/output. Default is input (JACK -F) |
| CD-L | I | 18 | CD input left channel | Analog input. 1.6Vrms of full scale input |
| CD-G | I | 19 | CD input reference ground | Analog input. 1.6Vrms of full scale input |
| CD-R | I | 20 | CD input right channel | Analog input. 1.6Vrms of full scale input |
| MIC1-L | IO | 21 | 1 st stereo microphone input left channel | Analog input/output. Default is input (JACK -B) |
| MIC1-R | IO | 22 | 1 st stereo microphone input right channel | Analog input/output. Default is input (JACK -B) |
| LINE1-L | IO | 23 | 1 st line input left channel | Analog input/output. Default is input (JACK -C) |
| LINE1-R | IO | 24 | 1 st line input right channel | Analog input/output. Default is input (JACK -C) |
| PCBEEP | I | 12 | External PCBEEP input | Analog input. 1.6Vrms of full scale input |
| FRONT- OUT-L | IO | 35 | Front output left channel | Analog output (JACK -D) |
| FRONT- OUT-R | IO | 36 | Front output right channel | Analog output (JACK -D) |
| SURR-OUT-L | IO | 39 | Surround out left channel | Analog output (JACK -A) |

| Name | Type | Pin No. | Description | Characteristic Definition |
|----------------|------|---------|------------------------------------|---|
| SURR-OUT-R | IO | 41 | Surround out right channel | Analog output (JACK -A) |
| CEN-OUT | O | 43 | Center output | Analog output (JACK -G) |
| LFE-OUT | O | 44 | Low Frequency output | Analog output (JACK -G) |
| SIDESURR-OUT-L | O | 45 | Side Surround output left channel | Analog output (JACK -H) |
| SIDESURR-OUT-R | O | 46 | Side Surround output right channel | Analog output (JACK -H) |
| Sense A | I | 13 | Jack Detect pin 1 | Jack resistor network input 1 |
| Sense B | I | 34 | Jack Detect pin 2 | Jack resistor network input 2 |
| DCVOL | I | 33 | DC sense for volume control | Analog DC input for external volume control |
| | | | | Total: 23 Pins |

6.3. Filter/Reference

Table 3. Filter/Reference

| Name | Type | Pin No. | Description | Characteristic Definition |
|---------------|------|---------|---------------------------------------|--|
| VREF | - | 27 | 2.5V Reference voltage | 10uf capacitor to analog ground |
| MIC1-VREFO-L | O | 28 | Bias voltage for MIC1 jack | 2.5V/3.75Vreference voltage |
| LINE1-VREFO | O | 29 | Bias voltage for LINE1 jack | 2.5V/3.75Vreference voltage |
| MIC2-VREFO | O | 30 | Bias voltage for MIC2 jack | 2.5V/3.75Vreference voltage |
| LINE2-VREFO | O | 31 | Bias voltage for LINE2 jack | 2.5V/3.75Vreference voltage |
| MIC1-VREFO-R | O | 32 | Bias voltage for MIC1 jack | 2.5V/3.75Vreference voltage |
| LINE1-VREFO-L | O | 37 | Bias voltage for LINE1 jack | 2.5V/3.75Vreference voltage |
| JDREF | - | 40 | Reference resistor for Jack detection | 20K, 1% external resistor to analog ground |
| | | | | Total: 8 Pins |

6.4. Power/Ground

Table 4. Power/Ground

| Name | Type | Pin No | Description | Characteristic Definition |
|-------|------|--------|-------------------------|---------------------------------------|
| AVDD1 | I | 25 | Analog VDD (5V or 3.3V) | Analog power for mixer and amplifier |
| AVSS1 | I | 26 | Analog GND | Analog ground for mixer and amplifier |
| AVDD2 | I | 38 | Analog VDD (5V or 3.3V) | Analog power for DACs and ADCs |
| AVSS2 | I | 42 | Analog GND | Analog ground for DACs and ADCs |
| DVDD1 | I | 1 | Digital VDD (3.3V) | Digital power |
| DVSS1 | I | 4 | Digital GND | Digital ground |
| DVDD2 | I | 9 | Digital VDD (3.3V) | Digital power |
| DVSS2 | I | 7 | Digital GND | Digital ground |
| | | | | Total: 8 Pins |

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

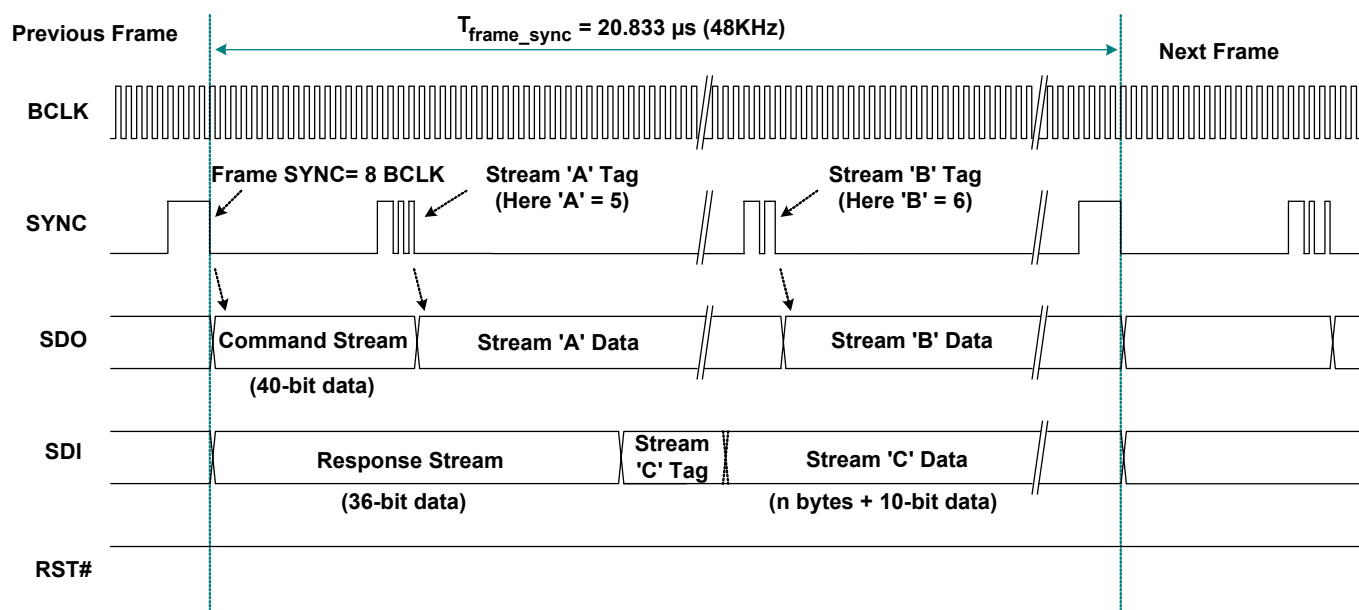


Figure 4. HDA Link Protocol

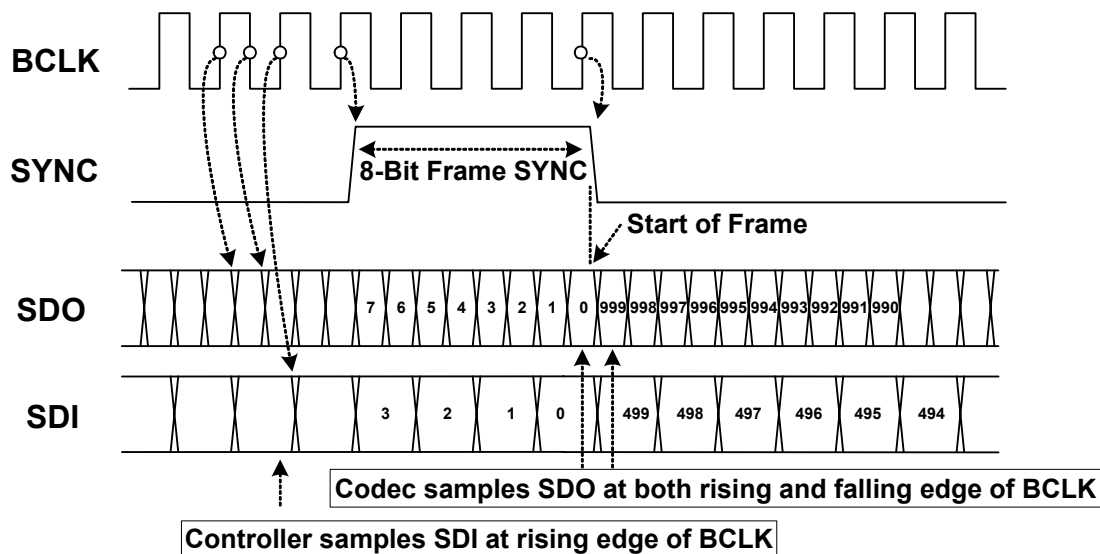
7.1.1. Signal Definitions

Table 5. Link Signal Definitions

| Item | Description |
|------|---|
| BCLK | 24.0MHz bit clock sourced from the HDA controller and connecting to all codecs. |
| SYNC | 48kHz signal is used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs. |
| SDO | Serial Data Output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double-pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported. |
| SDI | Serial Data Input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI. Up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID. |
| RST# | Active low reset signal. Asserted to reset the codec to default power-on state. RST# is sourced from the HDA controller and connects to all codecs. |

Table 6. HDA Signal Definitions

| Signal Name | Source | Type for Controller | Description |
|-------------|------------------|---------------------|---|
| BCLK | Controller | Output | Global 24.0MHz bit clock. |
| SYNC | Controller | Output | Global 48kHz Frame Sync and outbound tag signal. |
| SDO | Controller | Output | Serial data output from controller. |
| SDI | Codec/Controller | Input/Output | Serial data input from codec. Weakly pulled down by the controller. |
| RST# | Controller | Output | Global active low reset signal. |


Figure 5. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by the controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6, on page 10, shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, and a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 10, describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC880(D) is designed to receive a single SDO stream.

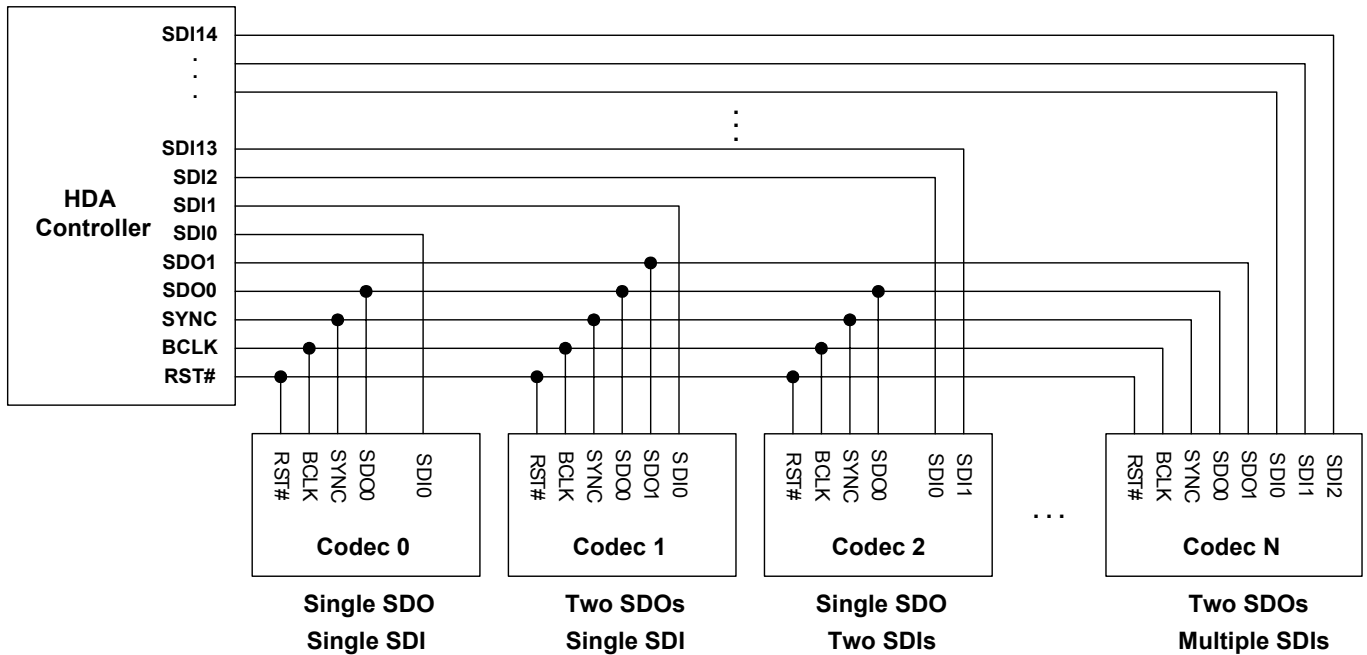


Figure 6. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

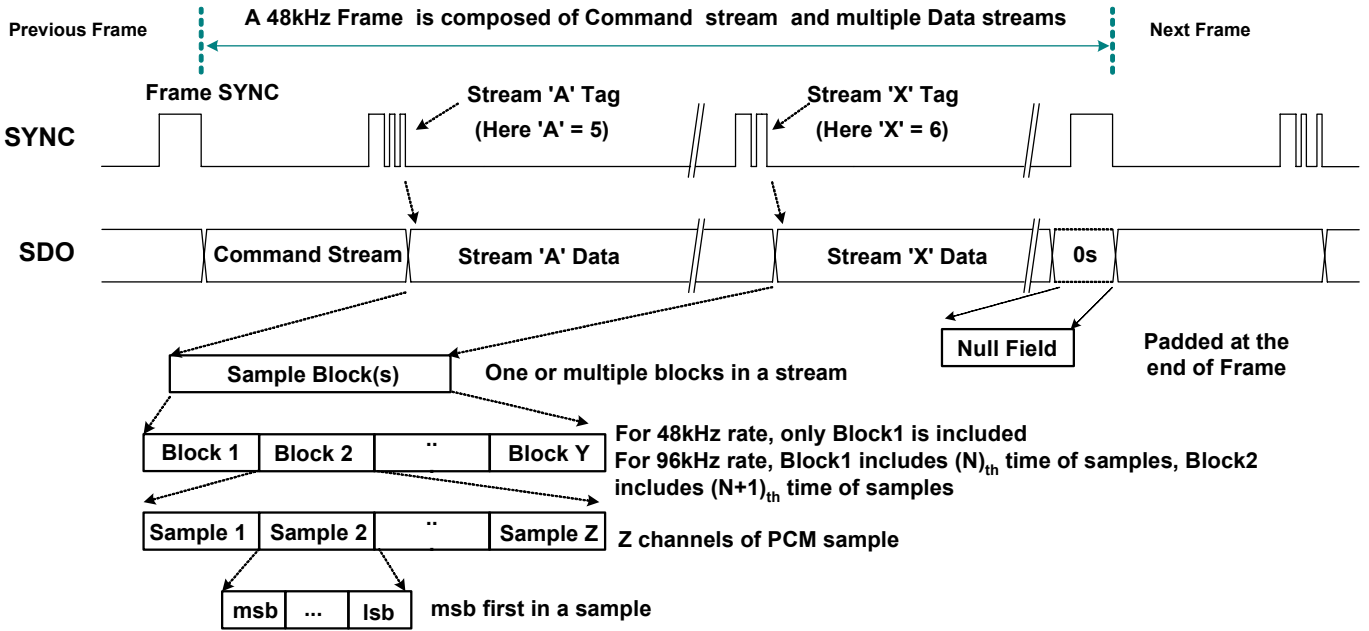


Figure 7. SDO Outbound Frame

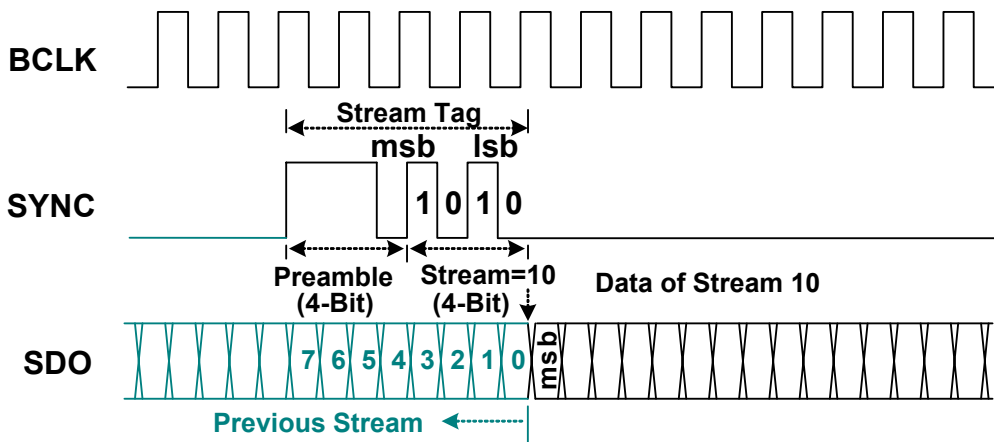


Figure 8. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to strip outbound data, completing transmission in less time to get more bandwidth. If software determines that the target codec supports multiple SDO capability, it enables the ‘Strip Control’ bit in the controller’s Output Stream Control Register to initiate a specific stream (Stream ‘A’ in Figure 9) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a stripped stream. The codec doesn’t support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not stripped. It is always transmitted on SDO0, and copied on SDO1.

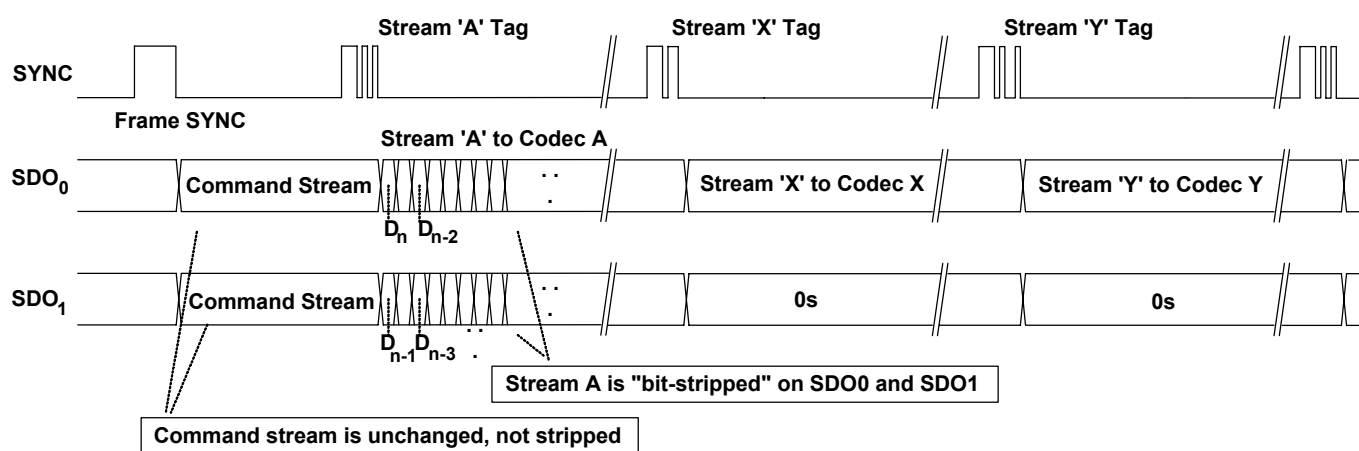


Figure 9. Stripped Stream on Multiple SDO

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – Single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 10).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 11).

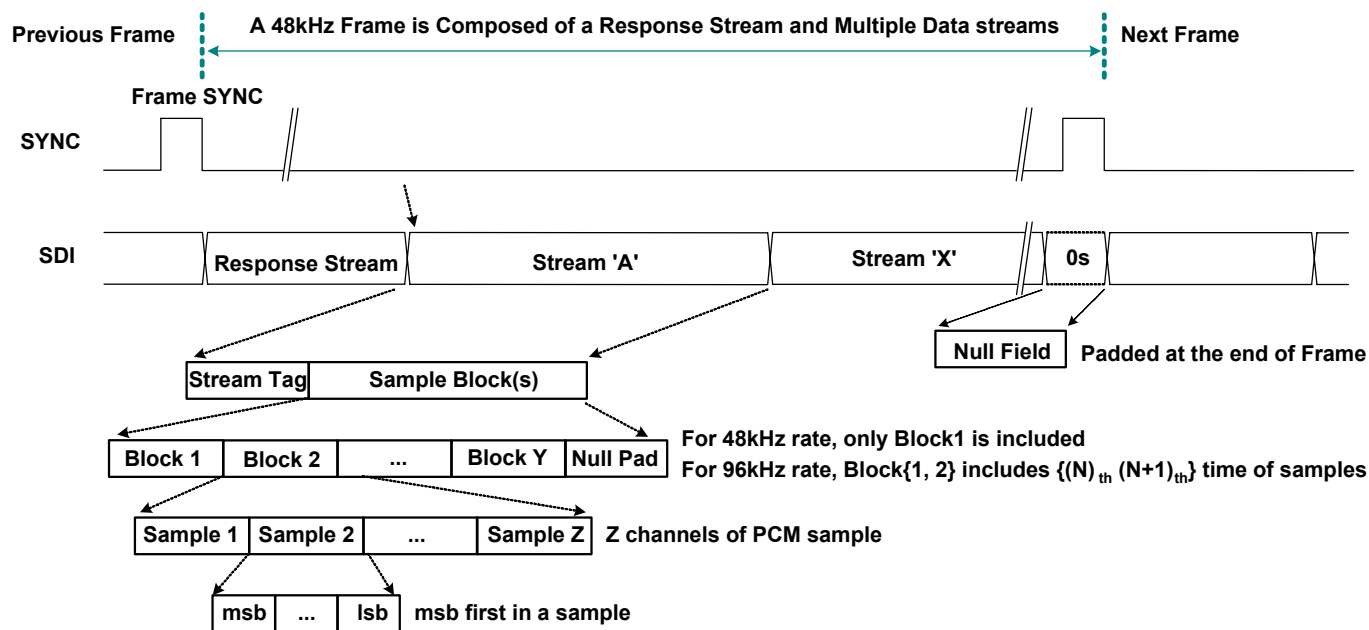


Figure 10. SDI Inbound Stream

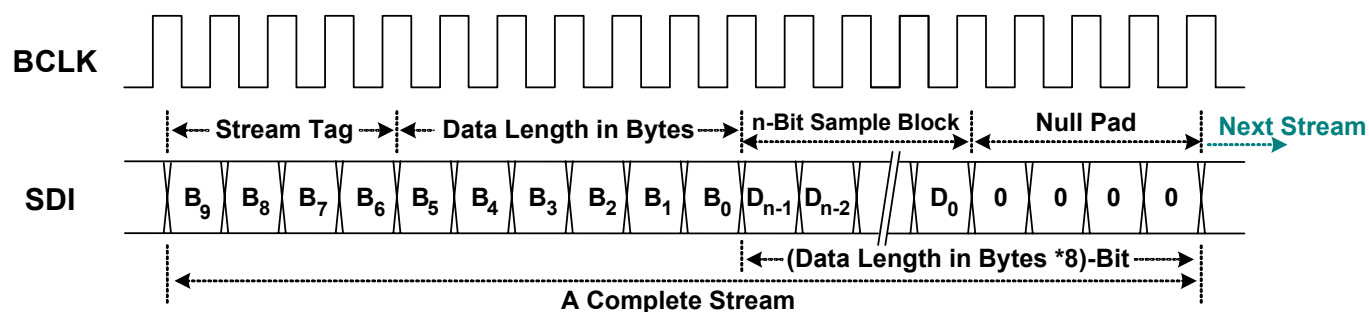


Figure 11. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data onto separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

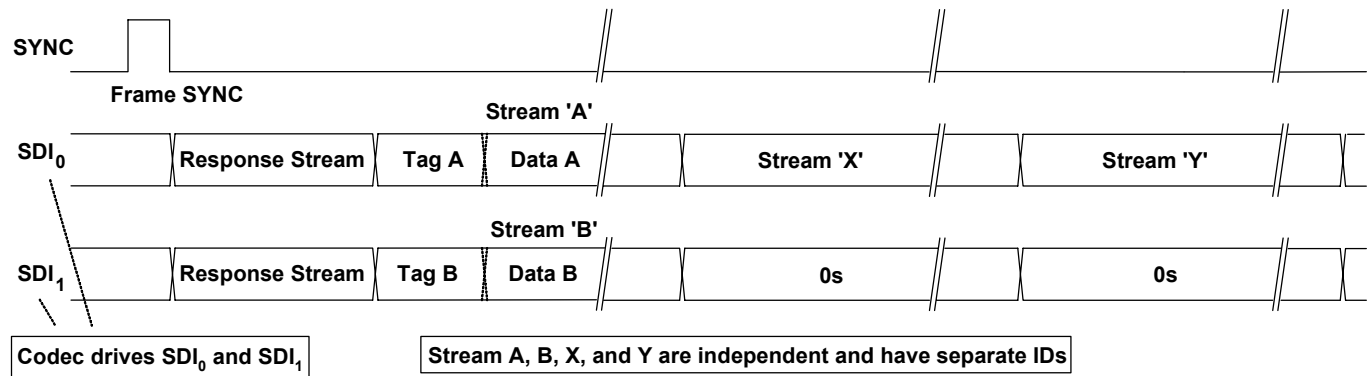


Figure 12. Codec Transmits Data Over Multiple SDI

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 15, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 15, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames. The cadence

“12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)”

interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 9, page 15).

| | |
|----------|--|
| 44.1kHz | 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block. |
| 88.2kHz | 12 ² - =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block. |
| 174.4kHz | 12 ⁴ - =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block. |

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- **Link Reset.**
Generated by assertion of the RST# signal. All codecs return to their power-on state
- **Codec Reset.**
Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset
2. Codec Reset
3. Codec changes its power state, e.g., hot docking a codec to an HDA system

7.3.1. Link Reset

A link reset may be caused by any of the following three events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the ‘CRST’ bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 13, page 17, shows the ‘Link Reset’ timing including the ‘Enter’ sequence (①~⑤) and ‘Exit’ sequence (⑥~⑨)

Enter 'Link Reset':

- ❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ As the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

- ❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)
- ❼ Software is responsible for de-asserting RST# after a minimum of 100µs BCLK running time (the 100µsec provides time for the codec PLL to stabilize)
- ❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC
- ❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC)

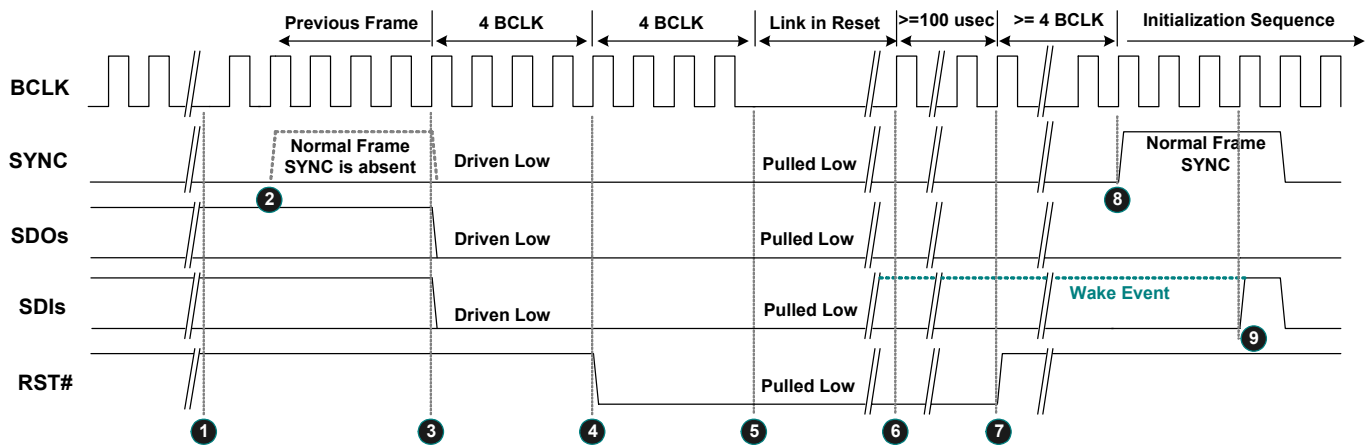


Figure 13. Link Reset Timing

7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec will stop driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operation state

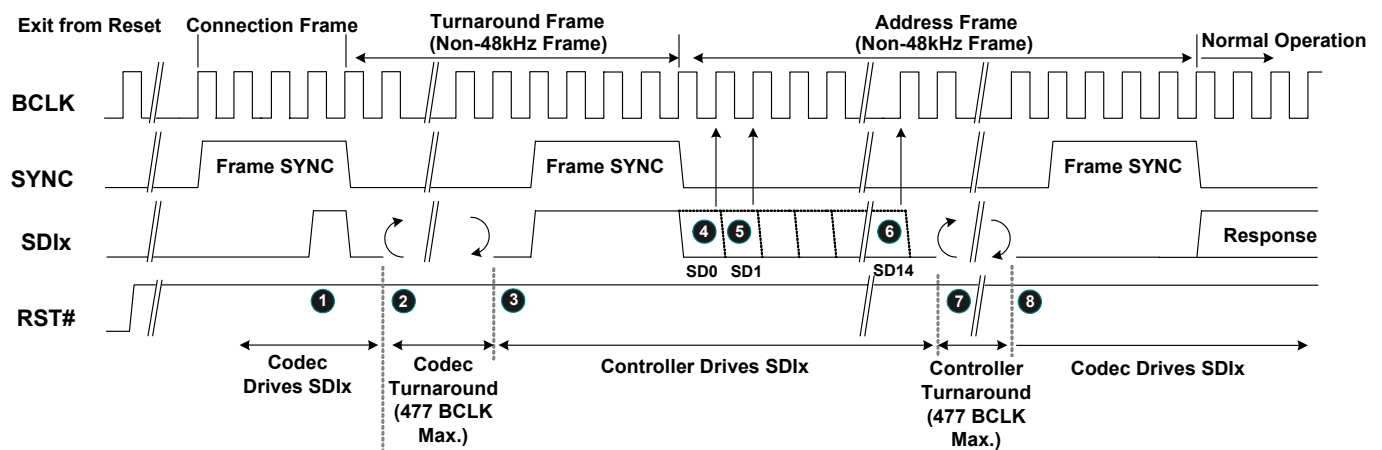


Figure 14. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 10 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 10. 40-Bit Commands in 4-Bit Verb Format

| Bit [39:32] | Bit [31:28] | Bit [27:20] | Bit [19:16] | Bit [15:0] |
|-------------|---------------|-------------|-------------|------------|
| Reserved | Codec Address | Node ID | Verb ID | Payload |

Table 11. 40-Bit Commands in 12-Bit Verb Format

| Bit [39:32] | Bit [31:28] | Bit [27:20] | Bit [19:8] | Bit [7:0] |
|-------------|---------------|-------------|------------|-----------|
| Reserved | Codec Address | Node ID | Verb ID | Payload |

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The ‘Tag’ in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:0] |
|----------|----------|-------------|------------|
| Valid | Unsol=0 | Reserved | Response |

Table 13. Unsolicited Response Format

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:28] | Bit [27:0] |
|----------|----------|-------------|-------------|------------|
| Valid | Unsol=1 | Reserved | Tag | Response |

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a ‘Valid’ bit to indicate the response is ‘Ready’. Bit-34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

Wake-Up events are not supported when in low-power mode. All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions.

Only the audio function (NID=01h) and widgets of output/input converters (NID=02h~05h, 06h~08h) support power control. Software may have various power states depending on system configuration.

Table 15 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) also have individual power control to supply fine-grained power control. Software can power-down individual converters when they are not being used.

Table 14. System Power State Definitions

| Power States | Definitions |
|--------------|---|
| D0 | All power on. Individual DACs and ADCs can be powered up or down as required |
| D1 | All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up |
| D2 | All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference is off (D1 + analog reference off) |
| D3 (Hot) | Power still supplied. The codec stops the internal clock. State is maintained |
| D3 (Cold) | All power removed. State lost |

Table 15. Power Controls in NID is 01h, 02h~05h, 07h~09h

| Item | Description | D0 | D1 | D2 | D3 | Link Reset |
|------------------------------------|-----------------------|--------|--------|--------|--------|------------|
| Audio Function (NID=01h) | LINK Response | Normal | Normal | Normal | PD | PD |
| | Front DAC | Normal | PD | PD | PD | PD |
| | Surr DAC | Normal | PD | PD | PD | PD |
| | Cen/Lfe DAC | Normal | PD | PD | PD | PD |
| | Surr Back DAC | Normal | PD | PD | PD | PD |
| | MIC ADC | Normal | PD | PD | PD | PD |
| | LINE ADC | Normal | PD | PD | PD | PD |
| | MIX ADC | Normal | PD | PD | PD | PD |
| | All Headphone Drivers | Normal | Normal | PD | PD | Normal |
| | All Mixers | Normal | Normal | PD | PD | Normal |
| All Reference | Normal | Normal | PD | PD | Normal | |
| Output Converters (NID=02h~05h) | Front DAC | Normal | PD | PD | PD | PD |
| | Surr DAC | Normal | PD | PD | PD | PD |
| | Cen/Lfe DAC | Normal | PD | PD | PD | PD |
| | Surr Back DAC | Normal | PD | PD | PD | PD |
| Input Converters (NID=07h~09h) | MIC ADC | Normal | PD | PD | PD | PD |
| | LINE ADC | Normal | PD | PD | PD | PD |
| | MIX ADC | Normal | PD | PD | PD | PD |

Note: PD=Powered Down

Table 16. Powered Down Conditions

| Condition | Description |
|-------------------------------|--|
| LINK Response powered down | Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. S/PDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied |
| Front DAC powered down | Analog block and digital filter are powered down |
| Surr DAC powered down | Analog block and digital filter are powered down |
| CEN/LFE DAC powered down | Analog block and digital filter are powered down |
| SIDESURR DAC powered down | Analog block and digital filter are powered down |
| MIC ADC powered down | Analog block and digital filter are powered down. Data on SDATA-IN is quiet |
| LINE ADC powered down | Analog block and digital filter are powered down. Data on SDATA-IN is quiet |
| MIX ADC powered down | Analog block and digital filter are powered down. Data on SDATA-IN is quiet |
| Headphone Driver powered down | All headphone drivers are powered down |
| Mixers powered down | All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive |
| Reference power down | All internal references, DC reference, and VREFOUTx at individual pin complexes are off |

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC880(D). If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget, some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, page 19, for detailed information about supported parameters.

Table 17. Verb – Get Parameters (Verb ID=F00h)

| Get Parameter Command Format | | | | Codec Response Format |
|------------------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=00h | Verb ID=F00h | Parameter ID[7:0] | 32-bit Response |

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

| Codec Response Format | |
|-----------------------|---|
| Bit | Description |
| 31:16 | Vendor ID=10ECh (Realtek's PCI vendor ID) |
| 15:0 | Device ID=0880h |

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Subsystem ID (Verb ID=F00h, Parameter ID=01h)

Table 19. Parameter – Subsystem ID (Verb ID=F00h, Parameter ID=01h)

| Codec Response Format | |
|-----------------------|---|
| Bit | Description |
| 31:0 | SubSystem ID=0880h The SubSystem ID is used to identify the function group |

Note1: The Audio Function Group Node (NID=01h) supports this parameter.

Note2: Only supported by the ALC880, ALC880D, ALC880-LF, and ALC880D-LF.

8.1.3. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 20. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:24 | Reserved. Read as 0's |
| 23:20 | MajRev. The major version number (in decimal) of the HDA Specification |
| 19:16 | MinRev. The minor version number (in decimal) of the HDA Specification |
| 15:8 | Revision ID. The vendor's revision number 00h is for the first silicon version, 01h is for the second version, etc. |
| 7:0 | Stepping ID. The vendor's stepping number within the given Revision ID |

Note: The Root Node (NID=00h) supports this parameter.

8.1.4. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

Table 21. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:24 | Reserved. Read as 0's |
| 23:16 | Starting Node Number The starting node number in the sequential widgets |
| 15:8 | Reserved. Read as 0's. |
| 7:0 | Total Number of Nodes For a root node, this is the total number of function groups in the root node For a function group, this is the total number of widget nodes in the function group |

8.1.5. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 22. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's |
| 7:0 | Function Group Type 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function |

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 23. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:17 | Reserved. Read as 0's |
| 16 | Beep Generator A '1' indicates the presence of an integrated Beep generator within the Audio Function Group |
| 15:12 | Reserved. Read as 0's |
| 11:8 | Input Delay |
| 7:4 | Reserved. Read as 0's |
| 3:0 | Output Delay |

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.7. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 24. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:24 | Reserved. Read as 0's |
| 23:20 | Widget Type 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget |
| 19:16 | Delay. Samples delayed between the HDA link and widgets |
| 15:11 | Reserved. Read as 0's |
| 10 | Power Control 0: Power control is not supported on this widget 1: Power control is supported on this widget |

Codec Response Format

| Bit | Description |
|-----|--|
| 9 | Digital 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.) |
| 8 | ConnList. Connection List 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried |
| 7 | UnsolCap. Unsolicited Capable 0: Unsolicited response is not supported 1: Unsolicited response is supported |
| 6 | ProcWidget. Processing Widget 0: No processing control 1: Processing control is supported |
| 5 | Reserved. Read as 0 |
| 4 | Format Override |
| 3 | AmpParOvr (AMP Param Override) |
| 2 | OutAmpPre (Out AMP Present) |
| 1 | InAmpPre (In AMP Present) |
| 0 | Stereo 0: Mono Widget 1: Stereo Widget |

8.1.8. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameter in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

Table 25. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:21 | Reserved. Read as 0's |
| 20 | B32. 32-bit audio format support 0: Not supported 1: Supported |
| 19 | B24. 24-bit audio format support 0: Not supported 1: Supported |
| 18 | B20. 20-bit audio format support 0: Not supported 1: Supported |
| 17 | B16. 16-bit audio format support 0: Not supported 1: Supported |

Codec Response Format

| Bit | Description |
|------------|---|
| 16 | B8. 8-bit audio format support 0: Not supported 1: Supported |
| 15:12 | Reserved. Read as 0's |
| 11 | R12. 384kHz (=8*48kHz) rate support 0: Not supported 1: Supported |
| 10 | R11. 192kHz (=4*48kHz) rate support 0: Not supported 1: Supported |
| 9 | R10. 176.4kHz (=4*44.1kHz) rate support 0: Not supported 1: Supported |
| 8 | R9. 96kHz (=2*48kHz) rate support 0: Not supported 1: Supported |
| 7 | R8. 88.2kHz (=2*44.1kHz) rate support 0: Not supported 1: Supported |
| 6 | R7. 48kHz rate support 0: Not supported 1: Supported |
| 5 | R6. 44.1kHz rate support 0: Not supported 1: Supported |
| 4 | R5. 32kHz (=2/3*48kHz) rate support 0: Not supported 1: Supported |
| 3 | R4. 22.05kHz (=1/2*44.1kHz) rate support 0: Not supported 1: Supported |
| 2 | R3. 16kHz (=1/3*48kHz) rate support 0: Not supported 1: Supported |
| 1 | R2. 11.025kHz (=1/4*44.1kHz) rate support 0: Not supported 1: Supported |
| 0 | R1. 8kHz (=1/6*48kHz) rate support 0: Not supported 1: Supported |

8.1.9. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

Table 26. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

| Bit | Description |
|------|---|
| 31:3 | Reserved. Read as 0's |
| 2 | AC3 0: Not supported 1: Supported |
| 1 | Float32 0: Not supported 1: Supported |
| 0 | PCM 0: Not supported 1: Supported |

Note: Input converters and output converters support this parameter.

8.1.10. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 27. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

| Bit | Description | | | | | | | | | | | | | | |
|----------|---|-----|----------|--------|-----|------|---|---|----------|------|-----|----------|--------|-----|------|
| 31:16 | Reserved. Read as 0's | | | | | | | | | | | | | | |
| 15:8 | VREF Control Capability '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>7:6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>100%</td> <td>80%</td> <td>Reserved</td> <td>Ground</td> <td>50%</td> <td>Hi-Z</td> </tr> </tbody> </table> | 7:6 | 5 | 4 | 3 | 2 | 1 | 0 | Reserved | 100% | 80% | Reserved | Ground | 50% | Hi-Z |
| 7:6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | |
| Reserved | 100% | 80% | Reserved | Ground | 50% | Hi-Z | | | | | | | | | |
| 7 | L-R Swap. Indicates left and right swap capability | | | | | | | | | | | | | | |
| 6 | Balanced I/O Pin '1' indicates this pin complex has balanced pins | | | | | | | | | | | | | | |
| 5 | Input Capable '1' indicates this pin complex supports input | | | | | | | | | | | | | | |
| 4 | Output Capable '1' indicates this pin complex supports output | | | | | | | | | | | | | | |
| 3 | Headphone Drive Capable '1' indicates this pin complex has an amplifier to drive a headphone | | | | | | | | | | | | | | |
| 2 | Presence Detect Capable '1' indicates this pin complex can detect whether there is a device plugged in | | | | | | | | | | | | | | |

Codec Response Format

| Bit | Description |
|-----|---|
| 1 | Trigger Required '1' indicates whether a software trigger is required for an impedance measurement |
| 0 | Impedance Sense Capable '1' indicates this pin complex can perform analog sense on the attached device to determine its type |

Note: Only Pin Complex widgets support this parameter.

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

| Bit | Description |
|-------|--|
| 31 | (Input) Mute Capable |
| 30:23 | Reserved. Read as 0 |
| 22:16 | Step Size Indicates the size of each step in the gain range. Permanently set to '3' (indicates a step of 1dB) |
| 15 | Reserved. Read as 0 |
| 14:8 | Number of Steps Indicates the number of steps in the gain range. '0' means the gain is fixed |
| 7 | Reserved. Read as 0 |
| 6:0 | Offset Indicates which step is 0dB |

8.1.12. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 29. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31 | (Output) Mute Capable |
| 30:23 | Reserved. Read as 0 |
| 22:16 | Step Size Indicates the size of each step in the gain range. Permanently set to ‘3’ (indicates a step of 1dB) |
| 15 | Reserved. Read as 0 |
| 14:8 | Number of Steps Indicates the number of steps in the gain range. ‘0’ means the gain is fixed |
| 7 | Reserved. Read as 0 |
| 6:0 | Offset. Indicates which step is 0dB |

8.1.13. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 30. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0 |
| 7 | Short Form 0: Short Form 1: Long Form |
| 6:0 | Connect List Length Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget) |

8.1.14. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 31. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

| Bit | Description |
|------|---|
| 31:4 | Reserved. Read as 0's |
| 3 | D3Sup 1: Power state D3 is supported |
| 2 | D2Sup 1: Power state D2 is supported |
| 1 | D1Sup 1: Power state D1 is supported |
| 0 | D0Sup 1: Power state D0 is supported |

8.1.15. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 32. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31:16 | Reserved. Read as 0's |
| 15:8 | NumCoeff. Number of Coefficient |
| 7:1 | Reserved. Read as 0's |
| 0 | Benign 0: Processing unit is not linear and not time invariant 1: Processing unit is linear and is time invariant |

8.1.16. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 33. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31 | GPIWake=0 The GPIO wake up function is not supported |
| 30 | GPIUnsol=1 The GPIO unsolicited response function is not supported |
| 29:24 | Reserved. Read as 0's |
| 23:16 | NumGPIs=00h No GPI pin is supported |
| 15:8 | NumGPOs=00h. No GPO pin is supported |
| 7:0 | NumGPIOs=02h. Two GPIO pins are supported |

8.1.17. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 34. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's |
| 7 | Delta 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob |
| 6:0 | NumSteps The number of steps in the range of the Volume Control Knob |

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 35. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=F01h | 0's |

Codec Response Format

| Response [31:0] |
|-------------------------------|
| Bit[7:0] are Connection Index |

Codec Response for NID=07h (MIC ADC)

| Bit | Description |
|------|--|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 00h) 00h: Pin complex - MIC1 01h: Pin complex - MIC2 02h: Pin complex - LINE1 03h: Pin complex - LINE2 04h: Pin complex - Analog CD-IN 05h: Pin complex - FRONT OUT 06h: Pin complex - SURR OUT Other: Reserved |

Codec Response for NID=08h (LINE ADC)

| Bit | Description |
|------|--|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 02h) 00h: Pin complex - MIC1 01h: Pin complex - MIC2 02h: Pin complex - LINE1 03h: Pin complex - LINE2 04h: Pin complex - Analog CD-IN 05h: Pin complex - FRONT OUT 06h: Pin complex - SURR OUT Other: Reserved |

Codec Response for NID=09h (MIX ADC)

| Bit | Description |
|------------|---|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 04h) 00h: Pin complex - MIC1 01h: Pin complex - MIC2 02h: Pin complex - LINE1 03h: Pin complex - LINE2 04h: Pin complex - Analog CD-IN 05h: Mixer (NID=0Bh, the summation of MIC1, MIC2, LINE1, LINE2, CD-IN and PCBEEP) 06h: Pin complex - FRONT OUT 07h: Pin complex - SURROUND OUT 08h: Pin complex - CEN/LFE OUT 09h: Pin complex - SURROUND BACK OUT Other: Reserved |

Codec Response for NID=10h (MIC1 Selector)

| Bit | Description |
|------------|--|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 00h) 00h: Front DAC Sum Widget (NID=0Ch) 01h: Surr DAC Sum Widget (NID=0Dh) 02h: Cen/Lfe DAC Sum Widget (NID=0Eh) 03h: SIDESURR DAC Sum Widget (NID=0Fh) Other: Reserved |

Codec Response for NID=11h (MIC2 Selector)

| Bit | Description |
|------------|--|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 00h) 00h: Front DAC Sum Widget (NID=0Ch) 01h: Surr DAC Sum Widget (NID=0Dh) 02h: Cen/Lfe DAC Sum Widget (NID=0Eh) 03h: SIDESURR DAC Sum Widget (NID=0Fh) Other: Reserved |

Codec Response for NID=12h (LINE1 Selector)

| Bit | Description |
|------|---|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 00h) 00h: Front DAC Sum Widget (NID=0Ch) 01h: Surr DAC Sum Widget (NID=0Dh) 02h: Cen/Lfe DAC Sum Widget (NID=0Eh) 03h: Side-Surr DAC Sum Widget (NID=0Fh) Other: Reserved |

Codec Response for NID=13h (LINE2 Selector)

| Bit | Description |
|------|---|
| 31:8 | 0's |
| 7:0 | Connection Index currently Set (Default value is 00h) 00h: Front DAC Sum Widget (NID=0Ch) 01h: Surr DAC Sum Widget (NID=0Dh) 02h: Cen/Lfe DAC Sum Widget (NID=0Eh) 03h: Side-Surr DAC Sum Widget (NID=0Fh) Other: Reserved |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 36. Verb – Set Connection Select (Verb ID=701h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|--------------------|
| CAd=X | Node ID=Xh | Verb ID=701h | Select Index [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for all nodes |

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 37. Verb – Get Connection List Entry (Verb ID=F02h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F02h | Offset Index - N[7:0] | 32-bit Response |

Codec Response for NID=07h (MIC ADC)

| Bit | Description |
|-------|---|
| 31:24 | Connection List Entry (N+3) Returns 1Bh (=27, Pin Complex - LINE2) for N=0~3 Returns 00h for n>3 |
| 23:16 | Connection List Entry (N+2) Returns 1Ah (Pin Complex - LINE1) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7 |
| 15:8 | Connection List Entry (N+1) Returns 19h (Pin Complex-MIC2) for N=0~3 Returns 14h (Pin Complex-FRONT) for N=4~7 Returns 00h for N>7 |
| 7:0 | Connection List Entry (N) Returns 18h (Pin Complex-MIC1) for N=0~3 Returns 1Ch (Pin Complex-CD) for N=4~7 Returns 00h for N>7 |

Codec Response for NID=08h (LINE ADC)

| Bit | Description |
|-------|---|
| 31:24 | Connection List Entry (N+3) Returns 1Bh (Pin Complex - LINE2) for N=0~3 Returns 00h for N>3 |
| 23:16 | Connection List Entry (N+2) Returns 1Ah (Pin Complex - LINE1) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7 |
| 15:8 | Connection List Entry (N+1) Returns 19h (Pin Complex-MIC2) for N=0~3 Returns 14h (Pin Complex-FRONT) for N=4~7 Returns 00h for N>7 |
| 7:0 | Connection List Entry (N) Returns 18h (Pin Complex-MIC1) for N=0~3 Returns 1Ch (Pin Complex-CD) for N=4~7 Returns 00h for N>7 |

Codec Response for NID=09h (MIX ADC)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3) Returns 1Bh (Pin Complex - LINE2) for N=0~3 Returns 15h (Pin Complex-SURR OUT) for N=4~7 Returns 00h for N>7 |
| 23:16 | Connection List Entry (N+2) Returns 1Ah (Pin Complex - LINE1) for N=0~3 Returns 14h (Pin Complex-FRONT OUT) for N=4~7 Returns 00h for N >7 |
| 15:8 | Connection List Entry (N+1) Returns 19h (Pin Complex-MIC2) for N=0~3 Returns 0Bh (Mixer) for N=4~7 Returns 17h (Pin Complex-SURROUND BACK OUT) for N =8~11 Returns 00h for N>11 |
| 7:0 | Connection List Entry (N) Returns 18h (Pin Complex-MIC1) for N =0~3 Returns 1Ch (Pin Complex-CD) for N =4~7 Returns 16h (Pin Complex-CEN/LFE OUT) for N =8~11 Returns 00h for N >11 |

Codec Response for NID=0Bh (Mixer)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3) Returns 1Bh (Pin Complex - LINE2) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7 |
| 23:16 | Connection List Entry (N+2) Returns 1Ah (Pin Complex - LINE1) for N=0~3 Returns 14h (Pin Complex - FRONT-OUT) for N=4~7 Returns 00h for N>7 |
| 15:8 | Connection List Entry (N+1) Returns 19h (Pin Complex - MIC2) for N=0~3 Returns 1Dh (Pin Complex - PCBEEP) for N=4~7 Returns 00h for N>7 |
| 7:0 | Connection List Entry (N) Returns 18h (Pin Complex - MIC1) for N=0~3 Returns 1Ch (Pin Complex - CD) for N=4~7 Returns 00h for N>7 |

Codec Response for NID=0Ch (Front Sum)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N) Returns 00h |
| 23:16 | Connection List Entry (N+2) Returns 00h |
| 15:8 | Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 02h (Front DAC) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=0Dh (Surround Sum)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N) Returns 00h |
| 23:16 | Connection List Entry (N+2) Returns 00h |
| 15:8 | Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 03h (Surround DAC) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=0Eh (Cen/Lfe Sum)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N) Returns 00h |
| 23:16 | Connection List Entry (N+2) Returns 00h |
| 15:8 | Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 04h (Cen/Lfe DAC) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=0Fh (Side-Surr Sum)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N) Returns 00h |
| 23:16 | Connection List Entry (N+2) Returns 00h |
| 15:8 | Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 05h (Front DAC) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=10h (MIC1 Sel)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3) Returns 0Fh (Side-Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 23:16 | Connection List Entry (N+2) Returns 0Eh (Cen/Lfe DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 15:8 | Connection List Entry (N+1) Returns 0Dh (Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 0Ch (Front DAC Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=11h (MIC2 Sel)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3) Returns 0Fh (Side-Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 23:16 | Connection List Entry (N+2) Returns 0Eh (Cen/Lfe DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 15:8 | Connection List Entry (N+1) Returns 0Dh (Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 0Ch (Front DAC Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=12h (LINE1 Sel)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3) Returns 0Fh (Side-Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 23:16 | Connection List Entry (N+2) Returns 0Eh (Cen/Lfe DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 15:8 | Connection List Entry (N+1) Returns 0Dh (Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 0Ch (Front DAC Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=13h (LINE2 Sel)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3) Returns 0Fh (Side-Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 23:16 | Connection List Entry (N+2) Returns 0Eh (Cen/Lfe DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 15:8 | Connection List Entry (N+1) Returns 0Dh (Surr DAC Sum Widget) for N=0~3 Returns 00h for N>3 |
| 7:0 | Connection List Entry (N) Returns 0Ch (Front DAC Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=14h (Pin Widget: FRONT-OUT)

| Bit | Description |
|------------|---|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 0Ch (NID=0Ch, Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=15h (Pin Widget: SURR-OUT)

| Bit | Description |
|------------|---|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 0Dh (NID=0Dh, Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=16h (Pin Widget: CEN/LFE-OUT)

| Bit | Description |
|------------|---|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 0Eh (NID=0Eh, Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=17h (Pin Widget: SIDESURR-OUT)

| Bit | Description |
|------------|---|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 0Fh (NID=0Fh, Sum Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=18h (Pin Widget: MIC1)

| Bit | Description |
|------------|--|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 10h (NID=10h, Select Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=19h (Pin Widget: MIC2)

| Bit | Description |
|------------|--|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 11h (NID=11h, Select Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=1Ah (Pin Widget: LINE1)

| Bit | Description |
|------------|--|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 12h (NID=12h, Select Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for NID=1Bh (Pin Widget: LINE2)

| Bit | Description |
|------|--|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1) Returns 000000h |
| 7:0 | Connection List Entry (N) Returns 13h (NID=13h, Select Widget) for N=0~3 Returns 00h for N>3 |

Codec Response for Other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 38. Verb – Get Processing State (Verb ID=F03h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=F03h | 0's |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit response |

Codec Response for All NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.6. Verb – Set Processing State (Verb ID=703h)

Table 39. Verb – Set Processing State (Verb ID=703h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|------------------------|
| CAd=X | Node ID=Xh | Verb ID=703h | Processing State [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for all nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 40. Verb – Get Coefficient Index (Verb ID=Dh)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|----------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=Dh | 0's | Bit [15:0] are Coefficient Index |

Codec Response for NID=20h (Realtek Defined Hidden Registers)

| Bit | Description |
|-------|-----------------------|
| 31:16 | Reserved. Read as 0's |
| 15:0 | Coefficient Index |

Codec Response for Other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 41. Verb – Set Coefficient Index (Verb ID=5h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=5h | Coefficient Index [15:0] | 0's for all nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 42. Verb – Get Processing Coefficient (Verb ID=Ch)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|-------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=Ch | 0's | Processing Coefficient [15:0] |

Codec Response for NID=20h (Realtek Defined Hidden Registers)

| Bit | Description |
|-------|------------------------|
| 31:16 | Reserved. Read as 0's |
| 15:0 | Processing Coefficient |

Codec Response for Other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 43. Verb – Set Processing Coefficient (Verb ID=4h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=4h | Coefficient [15:0] | 0's for all nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 44. Verb – Get Amplifier Gain (Verb ID=Bh)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|------------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=Bh | 'Get' payload [15:0] | Bit[7:0] are responsible for 'Get' |

'Get' Payload in Command Bit[15:0]

| Bit | Description |
|------|---|
| 15 | Get Input/Output 0: Input amplifier gain is requested 1: Output amplifier gain is requested |
| 14 | Reserved. Read as 0 |
| 13 | Get Left/Right 0: Right amplifier gain is requested 1: Left amplifier gain is requested |
| 12:4 | Reserved. Read as 0's |
| 3:0 | Index[3:0] for Input Source Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored. |

Codec Response for NID=07h (MIC ADC), 08h(LINE ADC) and 09h (MIX ADC)

| Bit | Description |
|------|--|
| 31:8 | 0's |
| 7 | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute) |
| 6:0 | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~35) specifying the volume from 0B~+35dB in 1dB steps Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute) |

Codec Response for NID=0Bh (MIXER Sum Widget)

| Bit | Description |
|------|---|
| 31:8 | 0's |
| 7 | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute 1: Mute (Default for all Index). Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute) |
| 6:0 | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~65) specifying the volume from -35dB~+30dB in 1dB steps Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute) |

Codec Response for NID=0Ch~0Fh (Sum Widget: Front, Surr, Cen/Lfe, SIDESURR Sum)

| Bit | Description |
|------|--|
| 31:8 | 0's |
| 7 | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute) |
| 6:0 | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0]. 7-bit step value (0~64) specifying the volume from -64dB~0dB in 1dB steps |

Codec Response for NID=14h~1Bh (Pin Complex: Front/Surr/CenLfe/SIDESURR/MIC1/MIC2/LINE1/LINE2)

| Bit | Description |
|------|--|
| 31:8 | 0's |
| 7 | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute, 0: Unmute, 1: Mute (NID=14h~1Bh,Default=1) |
| 6:0 | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0's Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain) |

Codec Response to Other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 45. Verb – Set Amplifier Gain (Verb ID=3h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=3h | ‘Set’ payload [7:0] | 0’s for all nodes |

‘Set’ Payload in Command Bit[15:0]

| Bit | Description |
|------|---|
| 15 | Set Output Amp 1 indicates output amplifier gain will be set |
| 14 | Set Input Amp 1 indicates input amplifier gain will be set |
| 13 | Set Left Amp 1 indicates left amplifier gain will be set |
| 12 | Set Right Amp 1 indicates right amplifier gain will be set |
| 11:8 | Index Offset (for input amplifiers on Sum widgets and Selector Widgets) 5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the ‘Set Input Amp’ bit is not set |
| 7 | Mute 0: Unmute 1: Mute ($-\infty$ gain) |
| 6:0 | Gain[6:0] A 7-bit step value specifying the amplifier gain |

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 46. Verb – Get Converter Format (Verb ID=Ah)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|--------------------|---------------------------|--------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=Ah | 0's | Bit[15:0] are converter format |

Codec Response for NID=02h~06h (Output Converters: Front, Surr, Cen/Lfe, Side-Surr DAC, and S/PDIF-OUT).

Codec Response for NID=07h~0Ah (Input Converters: MIC, LINE, UIO1, UIO2, MIX DAC, and S/PDIF-IN)

| Bit | Description |
|-------|---|
| 31:16 | Reserved. Read as 0 |
| 15 | Stream Type (TYPE) 0: PCM 1: Non-PCM |
| 14 | Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz |
| 13:11 | Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved |
| 10:8 | Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 Not supported. Always read as 000b |
| 7 | Reserved. Read as 0 |
| 6:4 | Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved |
| 3:0 | Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 47. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=Xh | Verb ID=2h | Set format [15:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for all nodes |

'Set' Payload in Command Bit[15:0]

| Bit | Description |
|-------|--|
| 31:16 | Reserved. Read as 0 |
| 15 | Stream Type (TYPE) 0: PCM 1: Non-PCM |
| 14 | Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz |
| 13:11 | Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved |
| 10:8 | Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 |
| 7 | Reserved. Read as 0 |
| 6:4 | Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved |
| 3:0 | Number of Channels 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels |

8.15. Verb – Get Power State (Verb ID=F05h)

Table 48. Verb – Get Power State (Verb ID=F05h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=Ah | 0's |

Codec Response Format

| Response [31:0] |
|-------------------|
| Power State [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:6 | Reserved. Read as 0's. |
| 5:4 | PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set. |
| 3:2 | Reserved. Read as 0's. |
| 1:0 | PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node. |

Codec Response for NID=02h, 03h, 04h, and 05h (Front, Surr, Cen/Lfe and Side-Surr DACs).

Codec Response for NID=07h, 08h, and 09h (MIC, LINE and MIX ADCs)

| Bit | Description |
|------|---|
| 31:6 | Reserved. Read as 0's |
| 5:4 | PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. The actual power state of the referenced node is also controlled by Audio Function (NID=01h), the PS-Set setting of the referenced node is used to provide fine-grained power control |
| 3:2 | Reserved. Read as 0's |
| 1:0 | PS-Set. Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls current power setting of referenced node |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.16. Verb – Set Power State (Verb ID=705h)

Table 49. Verb – Set Power State (Verb ID=705h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=705h | Power State [7:0] | 0's for all nodes |

'Power State' in Command Bit[7:0]

| Bit | Description |
|-----|--|
| 7:6 | Reserved. Read as 0's |
| 5:4 | PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node |
| 3:2 | Reserved. Read as 0's |
| 1:0 | PS-Set. Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 |

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 50. Verb – Get Converter Stream, Channel (Verb ID=F06h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F06h | 0's | Stream & Channel [7:0] |

Codec Response for NID=02h~06h (Output Converters: Front, Surr, Cen/Lfe, SIDESURR DAC, and S/PDIF-OUT)

Codec Response for NID=07h~0Ah (Input Converters: MIC ADC, LINE ADC, MIX DAC, and S/PDIF-IN)

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's |
| 7:4 | Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc. |
| 3:0 | Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 51. Verb – Set Converter Stream, Channel (Verb ID=706h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=706h | Stream & Channel [7:0] | 0's for all nodes |

'Stream and Channel' in Command Bit[7:0]

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's |
| 7:4 | Set Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc. |
| 1:0 | Set Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel |

Note: This verb assigns stream and channel for output converters (NID=02h~06h) and input converters (NID=07h~0Ah). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 52. Verb – Get Pin Widget Control (Verb ID=F07h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F07h | 0's | Pin Control [7:0] |

Codec Response for NID=14h~1Bh

(Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit | Description |
|------|---|
| 31:1 | Reserved. Read as 0's |
| 7 | H-Phn Enable (Headphone Amplifier Enable, EN_AMP for a I/O unit) 0: Disabled 1: Enabled |
| 6 | Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled |
| 5 | In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled |
| 4: | Reserved |

Codec Response for NID=14h~1Bh

(Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit | Description |
|-----|--|
| 2:0 | VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 53. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=707h | Pin Control [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for all nodes |

'Pin Control' in command [7:0]: (Pin: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit | Description |
|------|--|
| 31:1 | Reserved. Read as 0's |
| 7 | H-Phn Enable 0: Disabled 1: Enabled |
| 6 | Out Enable 0: Disabled 1: Enabled |
| 5 | In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled |
| 4: | Reserved |

'Pin Control' in command [7:0]: (Pin: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit | Description |
|-----|--|
| 2:0 | VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved |

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real time event.

Table 54. Verb – Get Unsolicited Response Control (Verb ID=F08h)

| Get Command Format | | | | Codec Response Format | |
|--------------------|-------------|---------------|-------------------|-----------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAd=X | Node ID=Xh | Verb ID= F08h | 0's | 32-bit Response | |

Codec Response for NID=0Ah (S/PDIF-IN), 14h~1Bh (Pin Complex), NID=01h for GPIO

| Bit | Description |
|------|--|
| 31:8 | Reserved. Read as 0's |
| 7 | Unsolicited Response 0: Disabled 1: Enabled |
| 6:4 | Reserved. Read as 0's |
| 3:0 | Assigned Tag for Unsolicited Response The tag [3:0] is assigned by software to determine which widget generates unsolicited responses |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

Table 55. Verb – Set Unsolicited Response Control (Verb ID=708h)

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=708h | EnableUnsol [7:0] | 0's for all nodes |

'EnableUnsol' in Command Bit [7:0]

| Bit | Description |
|------|--|
| 31:8 | Reserved. Read as 0's |
| 7 | Unsolicited Response 0: Disable 1: Enable |
| 6:4 | Reserved. Read as 0's |
| 3:0 | Tag for Unsolicited Response. Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses. |

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 56. Verb – Get Pin Sense (Verb ID=F09h)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|---------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= F09h | 0's | 32-bit Response |

Codec Response for NID=14h~1Bh (Pin Complex)

| Bit | Description |
|------|---|
| 31 | Presence Detect Status 0: No device is attached to the pin 1: Device is attached to the pin |
| 30:0 | Measured Impedance 0x7FFFFFFF or 0xFFFFFFFF: Valid sense is not available or busy |

Codec Response for other NID

| Bit | Description |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 57. Verb – Execute Pin Sense (Verb ID=709h)

| Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= 709h | Right Channel[0] | 0's for all nodes |

'Payload' in Command Bit[7:0]

| Bit | Description |
|-----|---|
| 7:1 | Reserved. Read as 0's |
| 0 | Right (Ring) Channel Select 0: Sense Left channel (Tip) 1: Sense Right channel (Ring) |

8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 58. Verb – Get Configuration Default (Verb ID=F1Ch)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= F1Ch | 0's | 32-bit Response |

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Eh, and 1Fh

| Bit | Description |
|------|--|
| 31:0 | 32-bit configuration information for each pin widget |

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

**Table 59. Verb – Set Configuration Default Bytes 0, 1, 2, 3
(Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)**

| Set Command Format | | | | Codec Response Format | |
|--------------------|--------------------|-----------------------------------|--------------------------|------------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAd=X | Node ID=Xh | Verb ID=71Ch, 71Dh, 71Eh, 71Fh | Label [7:0] | 0's for all nodes | |

Note: Supported by Pin Widget NID=14h~1Bh, 1Eh and 1Fh. Other widgets will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 60. Verb – Get BEEP Generator (Verb ID= F0Ah)

| Get Command Format | | | | Codec Response Format | |
|--------------------|--------------------|-------------------|--------------------------|------------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAd=X | Node ID=Xh | Verb ID= F1Bh | 0's | Divider [7:0] | |

'Response' for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved. |
| 7:0 | Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is 48kHz/(255*4)=47Hz The highest tone is 48kHz/(1*4)=12kHz A value of 00h in F[7:0] disables internal BEEP generator and allows external PCBEEP input |

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 61. Verb – Set BEEP Generator (Verb ID= 70Ah)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=71Bh | Divider [7:0] | 0's for all nodes |

'Divider' in Set Command

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7:0 | Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$ The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$ A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.29. Verb – Get GPIO Data (Verb ID= F15h)

Table 62. Verb – Get GPIO Data (Verb ID= F15h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F15h | 0's | 32-bit Response |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Data. Not supported |
| 1:0 | GPIO[1:0] Data The value written (output) or sensed (input) on the corresponding pin if it is enabled |

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.30. Verb – Set GPIO Data (Verb ID= 715h)

Table 63. Verb – Set GPIO Data (Verb ID= 715h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=715h | Data [7:0] | 0's for all nodes |

'Data' in Set command for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] output Data. Not supported |
| 1:0 | GPIO[1:0] Output Data The value written determines the value driven on a pin that is configured as an output pin |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 64. Verb – Get GPIO Enable Mask (Verb ID= F16h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F16h | 0's | EnableMask [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved |
| 7:2 | Reserved |
| 1:0 | GPIO[1:0] Enable mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 65. Verb – Set GPIO Enable Mask (Verb ID=716h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=716h | Enable Mask [7:0] | 0's for all nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Enable Mask. Not supported |
| 1:0 | GPIO[1:0] Enable Mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 66. Verb – Get GPIO Direction (Verb ID=F17h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F17h | 0's | Direction [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Direction Control. Not supported |
| 1:0 | GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 67. Verb – Set GPIO Direction (Verb ID=717h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=717h | Direction [7:0] | 0's for all nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Direction Control. Not supported |
| 1:0 | GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.35. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 68. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F19h | 0's | UnsolEnable [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Unsolicited Enable Mask. Not supported |
| 1:0 | GPIO[1:0] Unsolicited Enable mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.36. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 69. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=719h | UnsolEnable [7:0] | 0's for all nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved |
| 7:2 | GPIO[7:2] Unsolicited Enable Mask. Not supported |
| 1:0 | GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's |

8.37. Verb – Function Reset (Verb ID=7FFh)

Table 70. Verb – Function Reset (Verb ID=7FFh)

| Command Format (NID=01H) | | | | Codec Response Format |
|--------------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=01h | Verb ID=7FFh | 0's | 0's |

Codec Response

| Bit | Description |
|------|-----------------------|
| 31:0 | Reserved. Read as 0's |

Note: The Function Reset command causes all widgets to return to their power-on default state.

8.38. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

Table 71. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|-----------------------|-------------------|---------------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F0Dh/ F0Eh | 0's | Bit[31:16]=0's, Bit[15:0] are SIC bit |

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0]).

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-------|---|
| 31:16 | Read as 0's |
| 15 | Reserved. Read as 0's |
| 14:8 | CC[6:0] (Category Code) |
| 7 | LEVEL (Generation Level) |
| 6 | PRO (Professional or Consumer format) 0: Consumer format 1: Professional format |
| 5 | /AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright) 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | VCFG for Validity Control (control V bit and data in Sub-Frame) |
| 1 | V for Validity Control (control V bit and data in Sub-Frame) |
| 0 | Digital Enable. DigEn 0: OFF 1: ON |

NID=0Ah (S/PDIF-IN) Response to 'Get verb (F0Dh)'

NID=0Ah (S/PDIF-IN) Response to 'Get verb (F0Eh)'

| Bit | Description (a part of S/PDIF-IN Channel Status) |
|-------|---|
| 31:16 | Reserved. Read as 0's |
| 15 | Reserved. Read as 0's |
| 14:8 | CC[6:0] (Category Code) |
| 7 | LEVEL (Generation Level) |
| 6 | PRO (Professional or Consumer format) 0: Consumer format 1: Professional format |

NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Dh)’

NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Eh)’

| Bit | Description (a part of S/PDIF-IN Channel Status) |
|-----|---|
| 5 | /AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright) 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | Reserved |
| 1 | In‘V’alid. V bit in sub-frame of S/PDIF-IN 0: Data X and Y are valid, or S/PDIF-IN is not locked 1: At least one of data X and Y is invalid |
| 0 | Digital Enable. DigEn 0: OFF 1: ON |

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0’s |

8.39. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 72. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Xh, Set Control 1)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=70Dh | SIC [7:0] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0’s |

Set Command Format (Verb ID=70Yh, Set Control 2)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=70Eh | SIC [15:8] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0’s |

‘Payload’ in Set Control 1 for NID=06h (S/PDIF-OUT)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|---|
| 7 | LEVEL (Generation Level) |
| 6 | PRO (Professional or Consumer format) 0: Consumer format 1: Professional format |
| 5 | /AUDIO (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright) 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | VCFG for Validity Control (control V bit and data in Sub-Frame) |
| 1 | V for Validity Control (control V bit and data in Sub-Frame) |
| 0 | Digital Enable. DigEn 0: OFF 1: ON |

‘Payload’ in Set Control 2 for NID=06h (S/PDIF-OUT)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|---|
| 7 | Reserved. Read as 0’s |
| 6:0 | CC[6:0] (Category Code) |

‘Payload’ in Set Control 1 for NID=0Ah (S/PDIF-IN)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|---|
| 7:1 | Reserved |
| 0 | Digital Enable. DigEn 0: OFF 1: ON |

‘Payload’ in Set Control 2 for NID=0Ah (S/PDIF-IN)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|---|
| 7:0 | Reserved. Read as 0’s |

Note: Other widgets will ignore this verb.

8.40. Get/Set Volume Knob Widget (NID=21h) (Verb ID= F0Fh/70Fh)

Table 73. Get/Set Volume Knob Widget (NID=21h) (Verb ID= F0Fh/70Fh)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F0Fh | 0's | Bit[31:8]=0's, Bit[7:0] is volume |

Codec Response for NID=21h (Volume Knob Widget)

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7 | Direct 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume |
| 6:0 | Volume in steps |

Set Command Format (Verb ID=70Yh, Set Control 2)

| Set Command Format (Verb ID=70Yh, Set Control 2) | | | | Codec Response Format |
|--|-------------|--------------|----------------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=70Fh | Bit[7] is 'Direct' control | 0's |

'Payload' in Set Command for NID=21h (Volume Knob Widget)

| Bit | Description |
|------|--|
| 31:8 | Reserved |
| 7 | Direct 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume |
| 6:0 | Reserved |

Note: Other nodes will ignore this verb.

8.41. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/D22h/F23h)

Table 74. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd = X | Node ID=01h | Verb ID=F20h | 0s | 32-bit Response |

Codec Response for NID=01h

| Bit | Description |
|-------|------------------------------|
| 31:16 | Subsystem ID (Default=0880h) |
| 15:8 | Reserved. Read as 0s |
| 7:0 | Assembly ID. Read as 0 |

Note: Not supported by the ALC880, ALC880D, ALC880-LF, and ALC880D-LF.

8.42. Verb – Set Subsystem ID [31:0] (Verb ID=723h, 722h, 721h, 720h)

**Table 75. Verb – Set Subsystem ID [31:0]
(Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])**

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------------------------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd = X | Node ID=01h | Verb ID=723h, 722h, 721h, 720h | Label [7:0] | 0s for all nodes |

Note1: Supported by Audio Function Group NID=01h, other widgets will ignore this verb.

Note2: The BIOS can use these verbs to set the customized subsystem ID for Audio Function Group (NID=01h).

Note3: Not supported by the ALC880, ALC880D, ALC880-LF, and ALC880D-LF.

Codec Response for all NID

| Bit | Description |
|------|-------------|
| 31:0 | 0s |

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 76. Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--------------------------------------|--------|------------------------|---------|---------|-------|
| Power Supplies: | | | | | |
| Digital | DVDD | 3.0 | 3.3 | 3.6 | V |
| Analog | AVDD | 3.0 | 5.0 | 5.5 | V |
| Ambient Operating Temperature | Ta | 0 | - | +70 | °C |
| Storage Temperature | Ts | | | +125 | °C |
| ESD (Electrostatic Discharge) | | | | | |
| | | Susceptibility Voltage | | | |
| All Pins | | 4500V | | | |

9.1.2. Threshold Voltage

DVDD= 3.3V±5%, T_{ambient}=25°C, with 50pF external load.

Table 77. Threshold Voltage

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|-----------------|----------------------|---------|---------------------|-------|
| Input Voltage Range | V _{in} | -0.30 | - | DVDD +0.30 | V |
| Low Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI) | V _{IL} | - | - | 0.30*DVDD (1.00) | V |
| High Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI) | V _{IH} | 0.65* DVDD (2.00) | - | - | V |
| Low Level Input Voltage (S/PDIF-IN/OUT, GPIOs) | V _{IL} | - | - | 0.44*DVDD (1.45) | V |
| High Level Input Voltage (S/PDIF-IN/OUT, GPIOs) | V _{IH} | 0.56* DVDD (1.85) | - | - | V |
| High Level Output Voltage | V _{OH} | 0.9*DVDD | | - | V |
| Low Level Output Voltage | V _{OL} | - | - | 0.1*DVDD | V |
| Input Leakage Current | - | -10 | - | 10 | μA |
| Output Leakage Current (Hi-Z) | - | -10 | - | 10 | μA |
| Output Buffer Drive Current | - | - | 5 | - | mA |
| Internal Pull Up Resistance | - | - | 50k | 100k | Ω |

9.1.3. Digital Filter Characteristics

Table 78. Digital Filter Characteristics

| Filter | Symbol | Minimum | Typical | Maximum | Units |
|--------------------|-----------------------------|---------|---------|---------|-------|
| ADC Lowpass Filter | Passband | 0 | - | 19.2 | kHz |
| | Stopband | 28.8 | | | kHz |
| | Stopband Rejection | | -76.0 | | dB |
| | Passband Frequency Response | | ±0.20 | | dB |
| DAC Lowpass Filter | Passband | 0 | - | 19.2 | kHz |
| | Stopband | 28.8 | | | kHz |
| | Stopband Rejection | | -78.5 | | dB |
| | Passband Frequency Response | | ±0.20 | | dB |

9.1.4. S/PDIF Input/Output Characteristics

DVDD= 3.3V, T_{ambient}=25°C, with 75Ω external load.

Table 79. S/PDIF Input/Output Characteristics

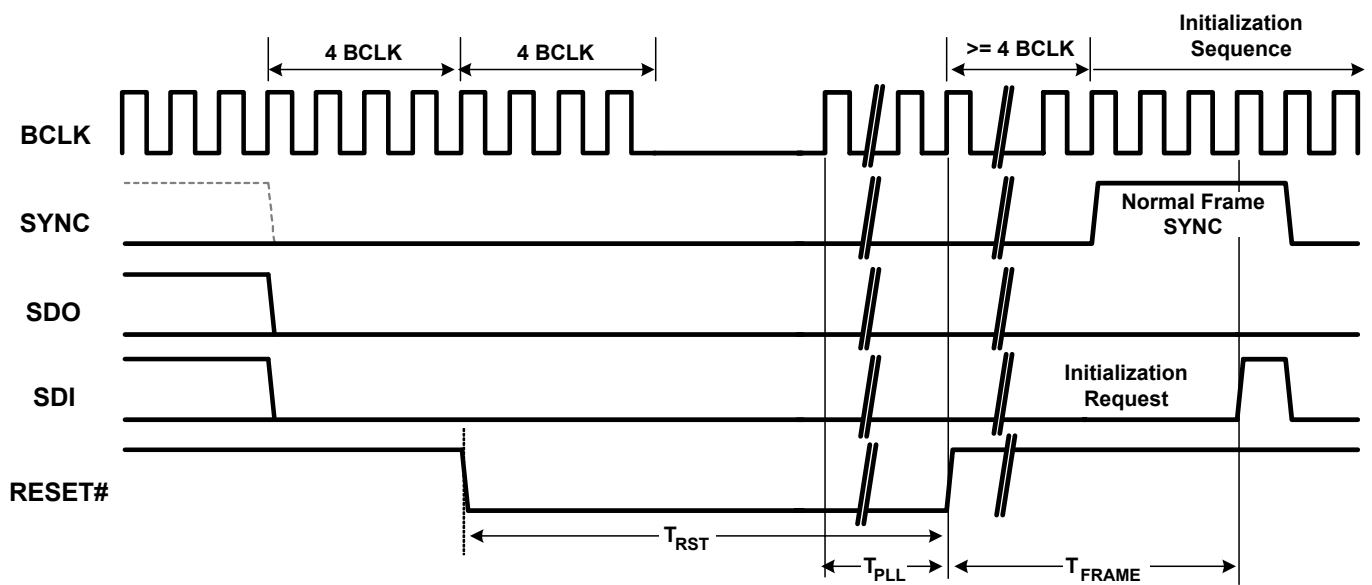
| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|------------------------------|-----------------|---------|---------|---------|-------|
| S/PDIF-OUT High Level Output | V _{OH} | 3.0 | 3.3 | - | V |
| S/PDIF-OUT Low Level Output | V _{OL} | - | 0 | 0.3 | V |
| S/PDIF-IN High Level Input | V _{IH} | 1.85 | - | - | V |
| S/PDIF-IN Low Level Input | V _{IL} | - | - | 1.45 | V |
| S/PDIF-IN Bias Level | V _t | - | 1.65 | - | V |

9.2. AC Characteristic

9.2.1. Link Reset and Initialization Timing

Table 80. Link Reset and Initialization Timing

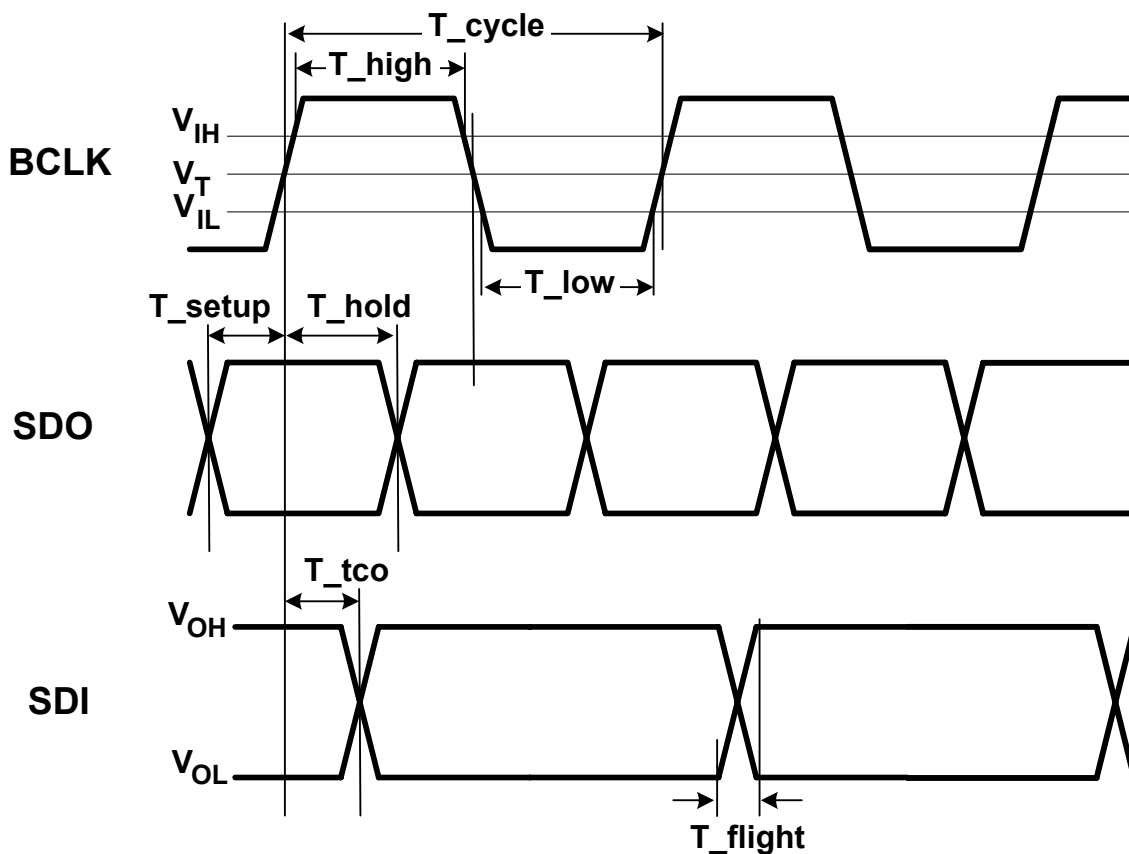
| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|-------------|---------|---------|---------|------------|
| RESET# Active Low Pulse Width | T_{RST} | 1.0 | - | - | μs |
| RESET# Inactive to BCLK Startup delay for PLL ready time | T_{PLL} | 20 | - | - | μs |
| SDI Initialization Request | T_{FRAME} | - | - | 1 | Frame Time |


Figure 15. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 81. Link Timing Parameters at the Codec

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|---------------------|----------------|---------|----------------|-----------|
| BCLK Frequency | | - | 24.0 | - | MHz |
| BCLK Period | T_{cycle} | - | 41.67 | - | ns |
| BCLK Jitter | T_{jitter} | - | - | 2.0 | ns |
| BCLK High Pulse Width | T_{high} | 18.75 (45%) | - | 22.91 (55%) | ns (%) |
| BCLK Low Pulse Width | T_{low} | 18.75 (45%) | - | 22.91 (55%) | ns (%) |
| SDO Setup Time at Both Rising and Falling Edge of BCLK | T_{setup} | 2.1 | - | - | ns |
| SDO Hold Time at Both Rising and Falling Edge of BCLK | T_{hold} | 2.1 | - | - | ns |
| SDI Valid Time After Rising Edge of BCLK (1: 50pF external load) | T_{tco} | - | 7.5 | 8.0 | ns |
| SDI Flight Time | T_{flight} | - | 2.0 | - | ns |


Figure 16. Link Signal Timing

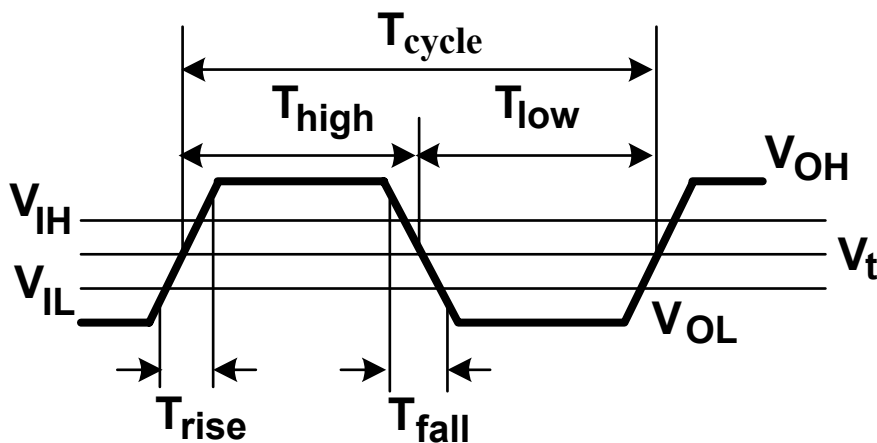
9.2.3. S/PDIF Output and Input Timing

Table 82. S/PDIF Output and Input Timing

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---------------------|------------|------------|------------|--------|
| S/PDIF-OUT Frequency ^{*1} | - | - | 6.144 | - | MHz |
| S/PDIF-OUT Period ^{*1} | T_{cycle} | - | 162.8 | - | ns |
| S/PDIF-OUT Jitter | T_{jitter} | - | - | 4 | ns |
| S/PDIF-OUT High Level Width ^{*1} | T_{High} | 78.1 (48%) | 81.4 (50%) | 84.6 (52%) | ns (%) |
| S/PDIF-OUT Low Level Width ^{*1} | T_{Low} | 78.1 (48%) | 81.4 (50%) | 84.6 (52%) | ns (%) |
| S/PDIF-OUT Rising Time | T_{rise} | - | 2.0 | - | ns |
| S/PDIF-OUT Falling Time | T_{fall} | - | 2.0 | - | ns |
| S/PDIF-IN Period ^{*2} | T_{cycle} | - | 162.8 | - | ns |
| S/PDIF-IN Jitter | T_{jitter} | - | - | 10 | ns |
| S/PDIF-IN High Level Width ^{*2} | T_{High} | 73.2 (45%) | 81.4 (50%) | 89.5 (55%) | ns (%) |
| S/PDIF-IN Low Level Width ^{*2} | T_{Low} | 73.2 (45%) | 81.4 (50%) | 89.5 (55%) | ns (%) |

^{*1}: Bit parameters for 48kHz sample rate of S/PDIF-OUT

^{*2}: Bit parameters for 48kHz sample rate of S/PDIF-IN


Figure 17. Input and Output Timing

9.2.4. Test Mode

Codec test mode and Automatic Test Equipment (ATE) mode are not supported.

9.3. Analog Performance

- Standard Test Conditions
- $T_{\text{ambient}}=25\text{ }^{\circ}\text{C}$, DVDD= 3.3V $\pm 5\%$, AVDD=5.0V $\pm 5\%$
 - 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
 - 10K Ω /50pF load; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation

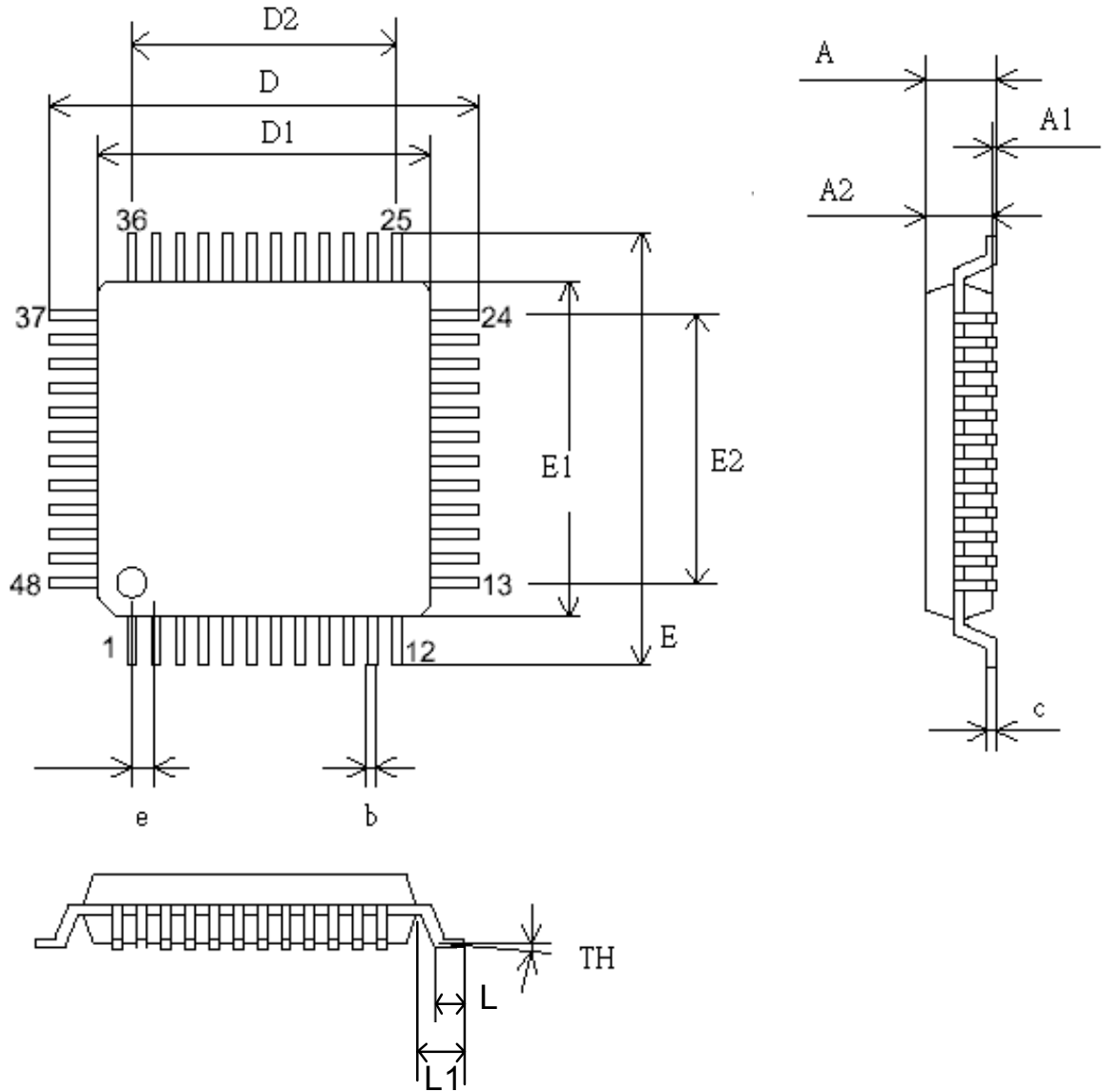
Table 83. Analog Performance

| Parameter | Min | Typ | Max | Units |
|---|------|-------|---------|---------------|
| Full Scale Input Voltage | | | | |
| All Inputs (gain=0dB) | - | 1.5 | - | Vrms |
| All ADC | - | 1.1 | - | Vrms |
| Full Scale Output Voltage | | | | |
| All DAC | - | 1.1 | 1.4 | Vrms |
| S/N (A Weighted) | | | | |
| Analog Inputs to Outputs | - | 95 | 100 | dB FSA |
| All ADC | - | 88 | - | dB FSA |
| All DAC | - | 95 | - | dB FSA |
| THD+N | | | | |
| Analog Inputs to Outputs | - | -90 | - | dB FS |
| ADC | - | -80 | - | dB FS |
| All DAC | - | -86 | - | dB FS |
| Frequency Response | | | | |
| Mixers | 10 | - | 22,000 | Hz |
| ADC, DAC | 16 | - | 19,200 | Hz |
| Power Supply Rejection | - | -40 | - | dB |
| Total Out-of-Band Noise (28.8kHz~100kHz) | - | -60 | - | dB |
| Amplifier Gain Step | - | 1 | - | dB |
| Crosstalk Between Input Channels | - | -80 | - | dB |
| Input Impedance (gain=0dB) | | 64 | | K Ω |
| Output Impedance | | | | |
| Amplified Output | | 1 | | Ω |
| Non-amplified Output | | 100 | | Ω |
| Digital Power Supply Current (normal operation) | | | | |
| DVDD=3.3V | - | 35 | - | mA |
| Digital Power Supply Current (power down mode) | | | | |
| DVDD=3.3V | - | - | 600 | μA |
| Analog Power Supply Current (normal operation) | | | | |
| AVDD=5.0V/3.3V | - | 68/52 | - | mA |
| Analog Power Supply Current (power down mode) | | | | |
| AVDD=5.0V/3.3V | - | - | 600/400 | μA |
| VREFOUTx Output Voltage | 2.25 | 2.50 | 3.75 | V |
| VREFOUTx Output Current | | 5 | | mA |

10. Application Circuits

Designers are suggested to contact Realtek to get the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits should be confirmed by Realtek. Realtek may update the latest application circuits onto our web site (www.realtek.com.tw) without modifying this data sheet.

11. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

11.1. Mechanical Dimensions Notes

| SYMBOL | MILLIMETER | | | INCH | | |
|--------|------------|------|------|------------|--------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 7.00 BSC | | | 0.276 BSC | | |
| D2 | 5.50 | | | 0.217 | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 7.00BSC | | | 0.276 BSC | | |
| E2 | 5.50 | | | 0.217 | | |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC | | | 0.0196 BSC | | |
| TH | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.0236 | 0.030 |
| L1 | | 1.00 | | | 0.0393 | |

| | | |
|---|----------|---------|
| TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm | | |
| LEADFRAME MATERIAL | | |
| APPROVE | DOC. NO. | |
| | VERSION | 02 |
| CHECK | DWG NO. | PKG-065 |
| | DATE | |
| REALTEK SEMICONDUCTOR CORP. | | |

12. Ordering Information

Table 84. Ordering Information

| Part Number | Package | Status |
|---------------|--|--------|
| ALC880 | Standard product. LQFP-48 | |
| ALC880D | ALC880 + Dolby Digital Live (software feature) | |
| ALC880-LF | ALC880 with Lead (Pb)-Free LQFP-48 package | |
| ALC880D-LF | ALC880D with Lead (Pb)-Free LQFP-48 package | |
| ALC880-VH | Standard product + HDA 1.0 compliant LQFP-48 package | |
| ALC880D-VH | ALC880-VH + Dolby Digital Live (software feature) | |
| ALC880-VH-LF | ALC880-VH with Lead (Pb)-Free LQFP-48 package | |
| ALC880D-VH-LF | ALC880D-VH with Lead (Pb)-Free LQFP-48 package | |

Note 1: See page 5 for Green package and version identification.

Note 2: Above parts are tested under AVDD =5.0V. If customers have lower AVDD request, please contact Realtek sales representatives or agents.

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