ALC888S-VC

(PN: ALC888S-VC-GR, ALC888SDD-VC-GR)

7.1+2 CHANNEL HIGH DEFINITION AUDIO CODEC WITH TWO INDEPENDENT S/PDIF-OUT

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC888S-VC (ALC888S Version C) High Definition Audio Codec ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/04/07	First release

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1. General Description

The ALC888S-VC and ALC888SDD-VC are high-performance 7.1+2 Channel High Definition Audio Codecs with two independent S/PDIF outputs. They feature ten DAC channels that simultaneously support 7.1 sound playback, plus independent stereo sound output (multiple streaming) through the front panel stereo outputs, and integrate two stereo ADCs that can support a stereo microphone, and feature Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) for voice applications.

The ALC888S-VC supports 16/20/24-bit S/DPIF input and output functions with sampling rate of up to 192kHz, offering easy connection of PCs to high quality consumer electronic products such as digital decoders and Minidisk devices. In addition to the standard (primary) S/PDIF output function, ALC888S features another independent (secondary) S/PDIF-OUT output and converters that transport digital audio output to a High Definition Media Interface (HDMI) transmitter (becoming more common in high-end PCs).

All analog IO are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched

The ALC888S-VC series support host audio controller from the Intel ICH series chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like environment sound emulation, multiple-band software equalizer and dynamic range control, optional Dolby® Digital Live, DTS® CONNECT™, and Dolby® Home Theater programs, the ALC888S provides an excellent home entertainment package and game experience for PC users.

The ALC888S-VC is an upgraded version of the ALC888S version B that meets the current WLP3.10 (Windows Logo Program) and future WLP requirements that become effective from 01 June 2008 (See section 2.3 Enhanced Features, page 4). The ALC888S-VC also conforms to Intel's Audio Codec low power state white paper and is ECR compliant.

2. Features

2.1. Hardware Features

- Meets premium audio requirements for Microsoft WLP 3.10
- Meets stricter performance requirements for future WLP effective from 01 June 2008
- High-performance DACs with 97dB SNR (A-Weighting), ADCs with 90dB SNR (A-Weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format recording simultaneously
- All DACs supports 16/20/24-bit, 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 16/20/24-btt, 44.1k/48k/96k/192kHz sample rate
- Two independent S/PDIF-OUT converters support 16/20/24-bit, 44.1k/48k/88.2k/96k/192kHz sample rate. One converter for normal S/PDIF output, the other outputs an independent digital stream to the HDMI transmitter
- One S/PDIF-IN converter supports 44.1k/48k/96k/192k Hz sample rate
- High-quality analog differential CD input
- Supports external PCBEEP input, built-in digital BEEP generator, and pass through function in D3 mode
- Software selectable 2.5V/3.75V/4.7V VREFOUT
- Two jack detection pins each designed to detect up to 4 jacks
- Extra jack detection pin for CD input when it is used as an optional line level input, S/PDIF input and output
- Supports legacy analog mixer architecture
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for each re-tasking jack
- Two GPIOs for customized applications
- Supports Anti-pop mode when analog power AVDD is on and digital power is off

- Support stereo digital microphone interface to improve voice quality
- Integrates high pass filter to cancel DC offset generated from digital microphone
- 48-pin LQFP 'Green' package
- Support low voltage IO for HDA Link (1.5V~3.3V)
- Intel low power ECR compliant, supports power status control for each analog converter and pin widgets, supports jack detection and wake up event in D3 mode

2.2. Software Features

- Meets Microsoft WLP 3.10 and future WLP audio requirements
- WaveRT based audio function driver for Windows Vista
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- Emulation of 26 sound environments to enhance gaming experience
- Multi bands of software equalizer and tool are provided
- Voice Cancellation and Key Shifting effect
- Dynamic range control (expander, compressor and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Provides 10-foot GUI for Windows Media Center
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Dolby® PCEE program™ (optional software feature)
- DTS® CONNECT™ (optional software feature)

- SRS® TrueSurround HD (optional software feature)
- Fortemedia® SAM™ technology for voice processing (Beam Forming and Acoustic Echo Cancellation) (optional software feature)
- Creative® Host Audio program (optional software feature)
- Voice recognition and Realtek proprietary API (SkyTel) is supported (optional software feature)

2.3. Enhanced Features

- Meet performance requirements in future WLP version (Effective from 01 June 2008)
- ADC supports 24-bit PCM format and 192kHz sample rate recording
- Supports secondary S/PDIF-OUT converter to output digital audio to external HDMI transmitter
- PCBEEP pass through function is supported when Codec is in D3 power down mode
- 3rd jack detection pin for CD input, S/PDIF output, and S/PDIF input connector
- Integrated high-pass filter to cancel DC offset generated from a digital microphone
- Intel low power ECR compliant, supports power status control for each analog converter and pin widget, supports jack detection and wake-up event in D3 mode

3. System Applications

- Desktop multimedia PCs
- Notebook PCs
- Information appliances (IA) e.g., set-top box

4. Block Diagram

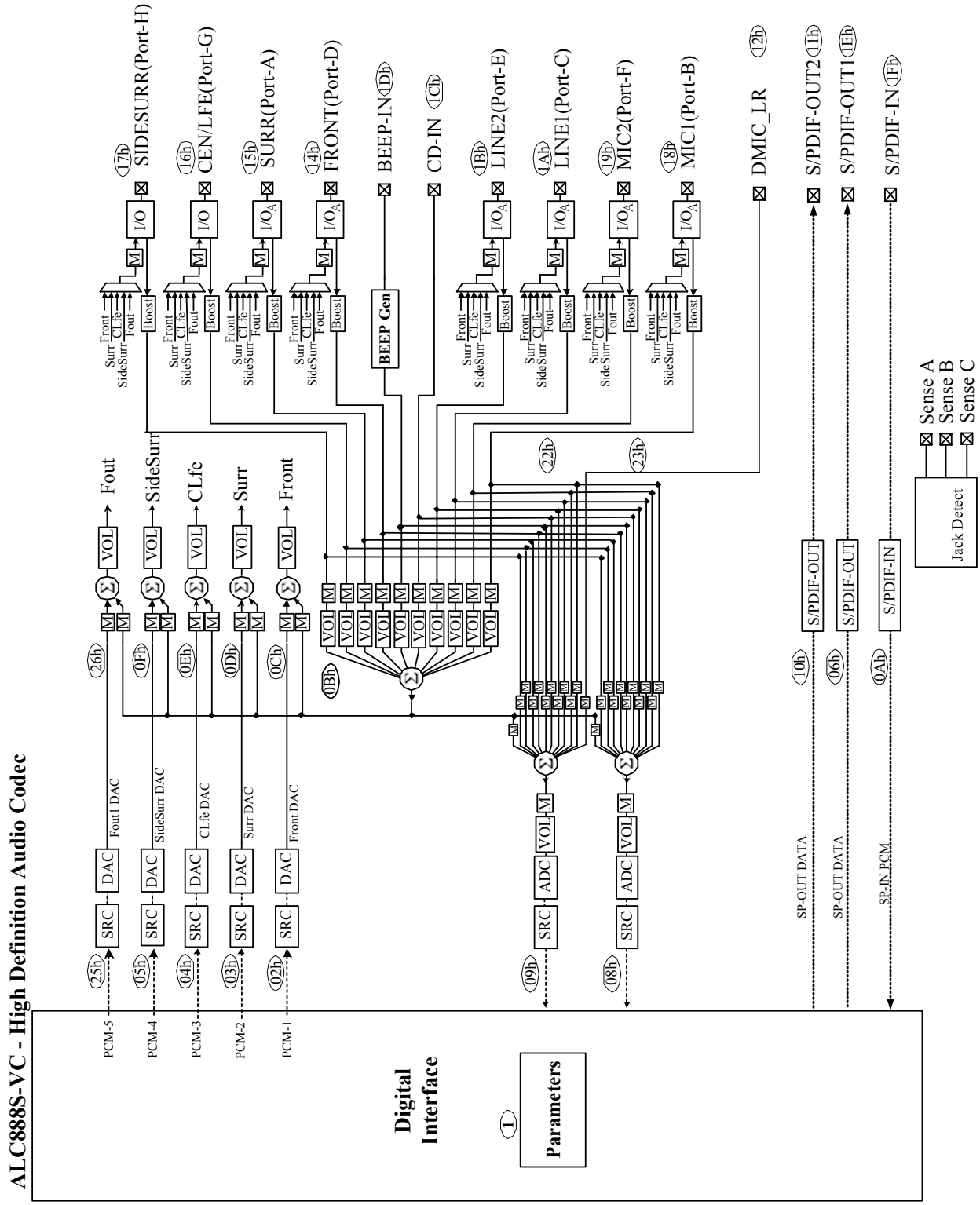


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin Complex widgets NID=14h~1Bh are re-tasking IO.

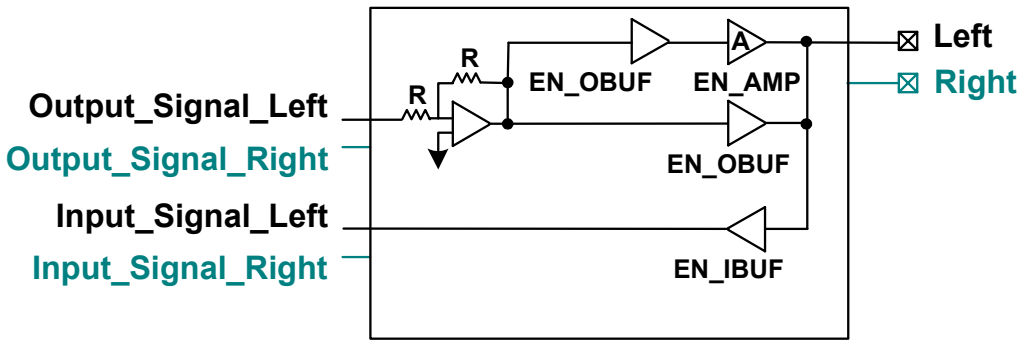


Figure 2. Analog Input/Output Unit

5. Pin Assignments

5.1. ALC888S-VC

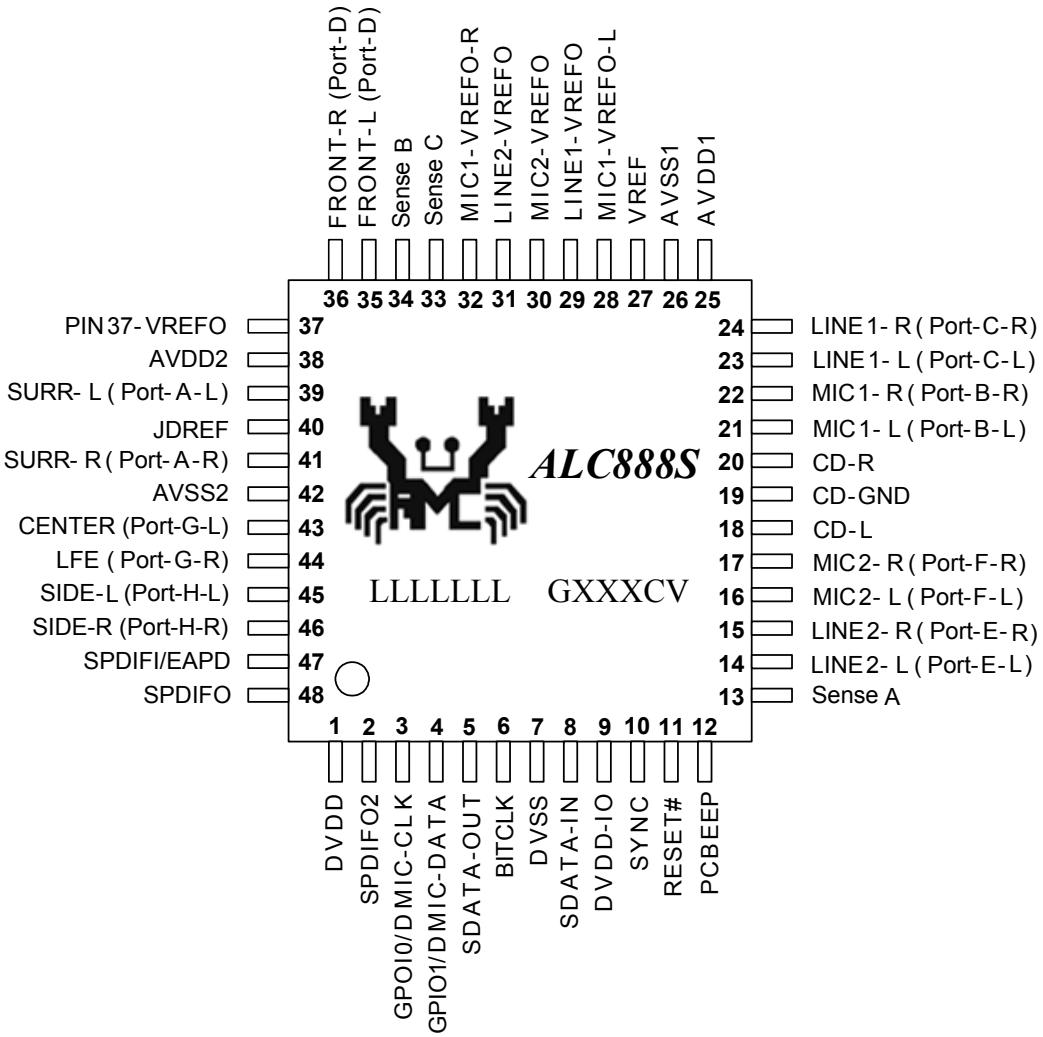


Figure 3. ALC888S-VC (Version C) Pin Assignments

*Pin differences between the ALC888S-VC version and version B are listed in section 6.5, page 11.

5.2. Green Package and Version Identification

Green package is indicated by a 'G' as shown in Figure 3. The version number is shown in the location marked 'CV'. For example, 'CV=C0' indicates silicon version 'C' and stepping version '0', which is the first stepping of the ALC888S-VC.

5.3. ALC888S (Version B)

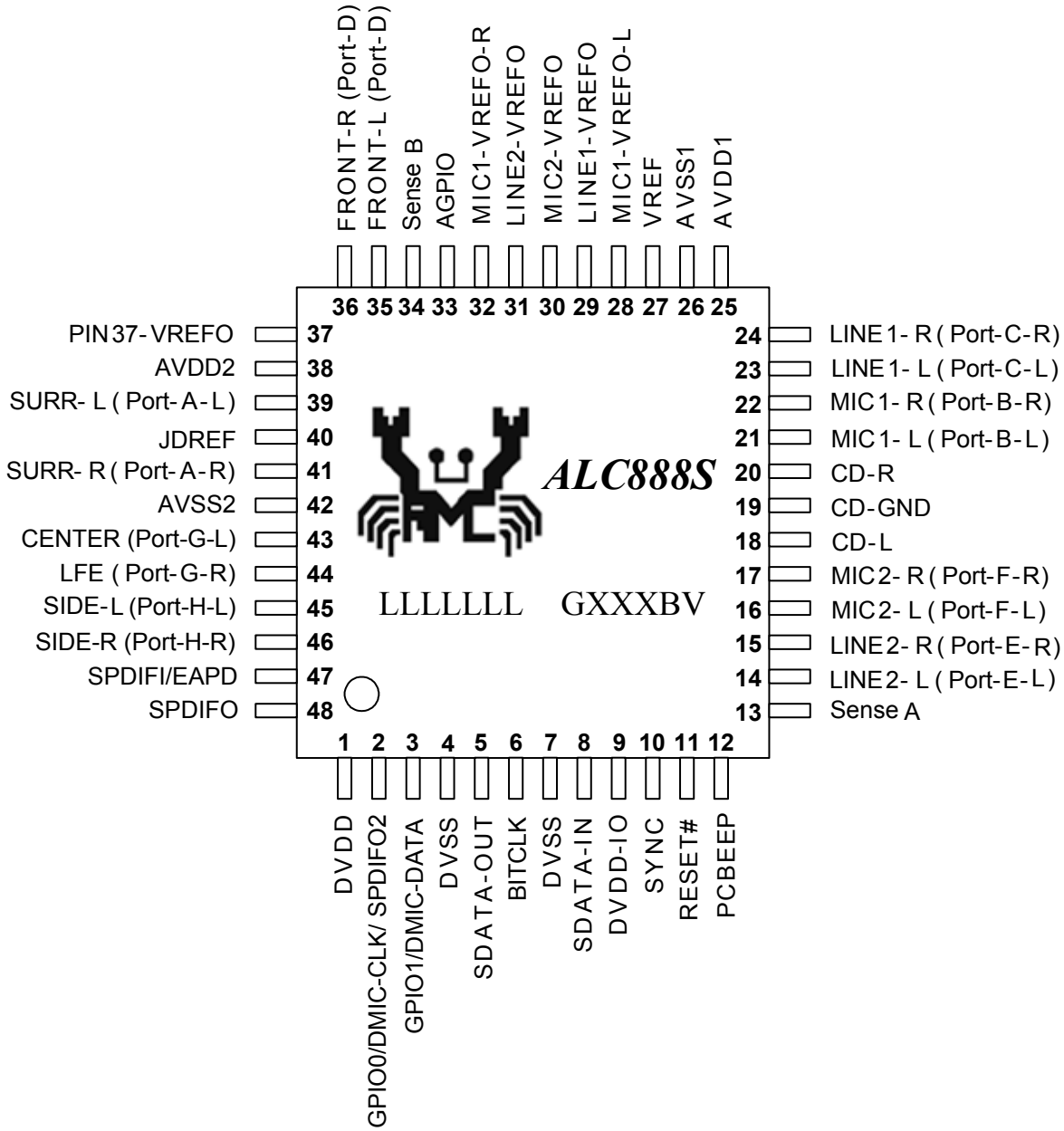


Figure 4. ALC888S (Version B) Pin Assignment

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
RESET#	I	11	H/W Reset	V_t=0.5*DVDD
SYNC	I	10	Sample Sync (48kHz)	V_t=0.5*DVDD
BITCLK	I	6	24MHz Bit Clock Input	V_t=0.5*DVDD
SDATA-OUT	I	5	Serial TDM Data Input	V_t=0.5*DVDDIO
SDATA-IN	O	8	Serial TDM Data Output	V_t=0.5*DVDDIO, V_{OH}=DVDDIO, V_{OL}=DVSS
SPDIFI / EAPD	I/O	47	S/PDIF Input / Signal to Power Down External Amplifier	V_{IL}=1.45V, V_{IH}=1.85V / V_{OH}=DVDD, V_{OL}=DVSS
SPDIFO	O	48	First S/PDIF Output	Output has 12mA@75Ω driving capability V_{OH}=DVDD, V_{OL}=DVSS
SPDIFO2	O	2	Secondary S/PDIF Output for Digital Audio Output to HDMI	Output has 12mA@75Ω driving capability V_{OH}=DVDD, V_{OL}=DVSS
GPIO0 / DMIC-CLK	IO	3	General Purpose Input/Output 0 Clock Output to Digital MIC	Input: Vt=(2/3)*DVDD Output: V_{OH}=DVDD, V_{OL}=DVSS
GPIO1 / DMIC-DATA	IO	4	General Purpose Input/Output 1 Serial Data from Digital MIC	Input: Vt=(2/3)*DVDD Output: V_{OH}=DVDD, V_{OL}=DVSS
				Total: 10 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LINE2-L	IO	14	2nd Line Input Left Channel	Analog input/output, default is input (JACK-E)
LINE2-R	IO	15	2nd Line Input Right Channel	Analog input/output, default is input (JACK –E)
MIC2-L	IO	16	2nd Stereo Microphone Input Left Channel	Analog input/output, default is input (JACK –F)
MIC2-R	IO	17	2nd Stereo Microphone Input Right Channel	Analog input/output, default is input (JACK –F)
CD-L	I	18	CD Input Left Channel	Analog input, 1.6Vrms of full scale input
CD-GND	I	19	CD Input Reference Ground	Analog input, 1.6Vrms of full scale input
CD-R	I	20	CD Input Right Channel	Analog input, 1.6Vrms of full scale input
MIC1-L	IO	21	1st Stereo Microphone Input Left Channel	Analog input/output, default is input (JACK –B)
MIC1-R	IO	22	1st Stereo Microphone Input Right Channel	Analog input/output, default is input (JACK –B)
LINE1-L	IO	23	1st Line Input Left Channel	Analog input/output, default is input (JACK –C)
LINE1-R	IO	24	1st Line Input Right Channel	Analog input/output, default is input (JACK –C)
PCBEEP	I	12	External PCBEEP Input	Analog input, 1.6Vrms of full scale input

Name	Type	Pin	Description	Characteristic Definition
FRONT-L	IO	35	Front Output Left Channel	Analog output (JACK –D)
FRONT-R	IO	36	Front Output Right Channel	Analog output (JACK –D)
SURR–L	IO	39	Surround Out Left Channel	Analog output (JACK –A)
SURR–R	IO	41	Surround Out Right Channel	Analog output (JACK –A)
CENTER	O	43	Center Output	Analog output (JACK –G)
LFE	O	44	Low Frequency Output	Analog output (JACK –G)
SIDE–L	O	45	Side Output Left Channel	Analog output (JACK –H)
SIDE–R	O	46	Side Output Right Channel	Analog output (JACK –H)
Sense A	I	13	Jack Detect Pin l	Jack resistor network input 1 for port A/B/C/D {39.2k, 20k, 10k, 5.1k} with 1% accuracy
Sense B	I	34	Jack Detect Pin 2	Jack resistor network input 2 for port E/F/G/H {39.2k, 20k, 10k, 5.1k} with 1% accuracy
Sense C	I	33	Jack Detect Pin 3	Jack resistor network input 3 for CD, 1st S/PDIF Out, 2nd S/PDIF Out, S/PDIF-IN {39.2k, 20k, 10k, 5.1k} with 1% accuracy
				Total: 23 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
VREF	-	27	2.5V Reference Voltage	10µf capacitor to analog ground
MIC1-VREFO-L	O	28	Bias Voltage for MIC1 Jack	2.5V/3.75V reference voltage
LINE1-VREFO	O	29	Bias Voltage for LINE1 Jack	2.5V/3.75V reference voltage
MIC2-VREFO	O	30	Bias Voltage for MIC2 Jack	2.5V/3.75V reference voltage
LINE2-VREFO	O	31	Bias Voltage for LINE2 Jack	2.5V/3.75V reference voltage
MIC1-VREFO-R	O	32	Bias Voltage for MIC1 Jack	2.5V/3.75V reference voltage
PIN37-VREFO	O	37	Bias Voltage for Software Select Jack	2.5V/3.75V reference voltage
JDREF	-	40	Reference Resistor for Jack Detection	20K, 1% external resistor to analog ground
				Total: 8 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
AVDD1	I	25	Analog VDD	Analog power for mixer and amplifier
AVSS1	I	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	I	38	Analog VDD	Analog power for DACs and ADCs
AVSS2	I	42	Analog GND	Analog ground for DACs and ADCs
DVDD	I	1	Digital VDD	Digital power for core
DVDD-IO	I	9	Digital VDD	Digital IO power for HDA bus
DVSS	I	7	Digital GND	Digital ground for HDA bus
				Total: 7 Pins

6.5. Pin Differences: ALC888S-VC vs. ALC888S (Version B)

Table 5. Pin Difference: ALC888S-VC vs. ALC888S (Version B)

Pin Number	ALC888S-VC	ALC888S (Version B)	Description for ALC888S-VC
Pin 2	SPDIFO2	GPIO0/DMIC-CLK/ SPDIFO2	Pin 2 is assigned as secondary S/PDIF-OUT, not shared with GPIO and digital microphone interface*[1]
Pin 3	GPIO0/DMIC-CLK	GPIO1/DMIC-DATA	GPIO0/DMIC-CLK is shifted to pin 3*[2]
Pin 4	GPIO1/DMIC-DATA	DVSS	GPIO1/DMIC-DATA is shifted to pin 4*[3]
Pin 33	Sense C	AGPIO	Pin 33 is designed to support 3rd jack detect

**1: The secondary S/PDIF output is default disabled and floated.*
**2: Pin 3 is default configured as a GPI input. The clock output of the digital microphone is functional when the BIOS program digital MIC port is enabled.*
**3: Pin 4 is default defined as a GPI input. Data input to the digital microphone is functional when the BIOS program digital MIC port is enabled. If the digital MIC function is not used, the ALC888S-VC is pin compatible with the ALC888S B version, and can be mounted directly on a B version PCB layout.*

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 5 shows the basic concept of the HDA link protocol.

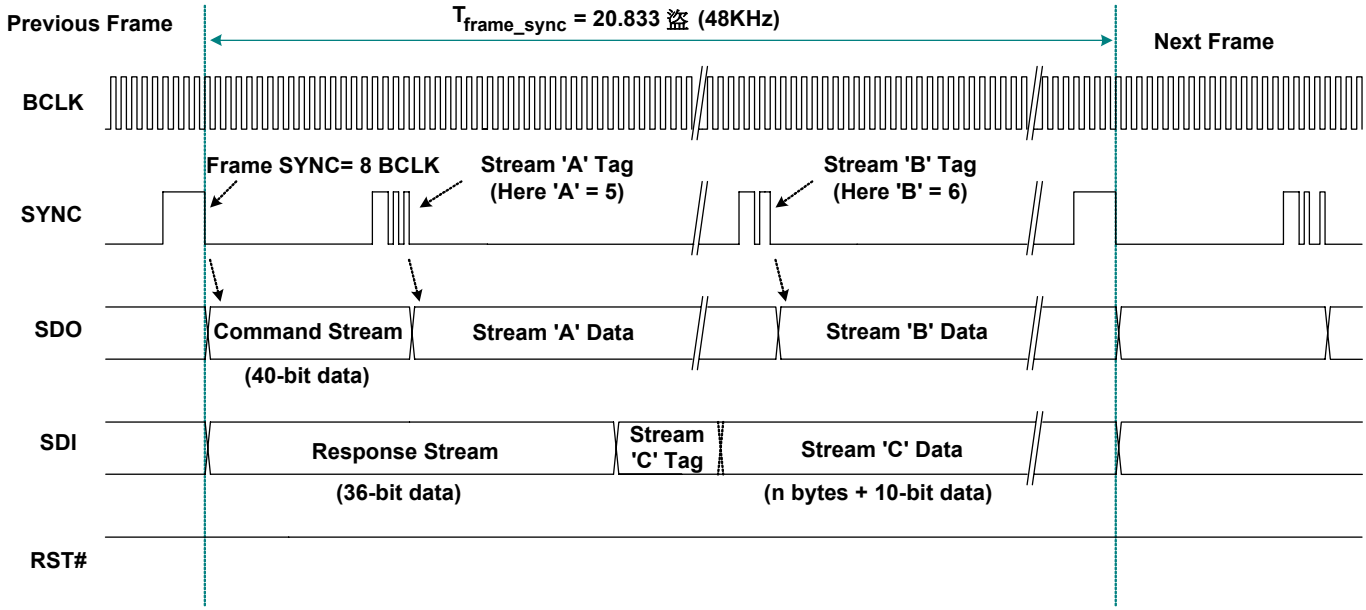


Figure 5. HDA Link Protocol

7.1.1. Signal Definitions

Table 6. Link Signal Definitions

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connecting to all codecs.
SYNC	48kHz of signal is used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial data input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.

Table 7. HDA Signal Definitions

Signal Name	Source	Type for Controller	Description
BCLK	Controller	Output	Global 24.0MHz bit clock
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal
SDO	Controller	Output	Serial data output from controller
SDI	Codec/Controller	Input/Output	Serial data input from codec. Weakly pulled down by the controller
RST#	Controller	Output	Global active low reset signal

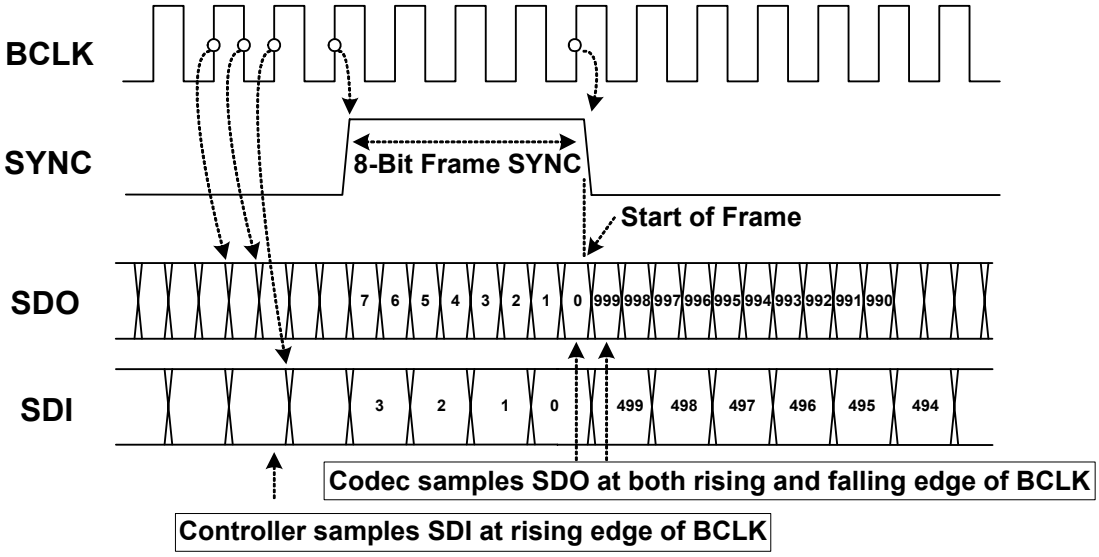


Figure 6. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 7 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 15 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 7 can be implemented concurrently in an HDA system. The ALC888S-VC is designed to receive a single SDO stream.

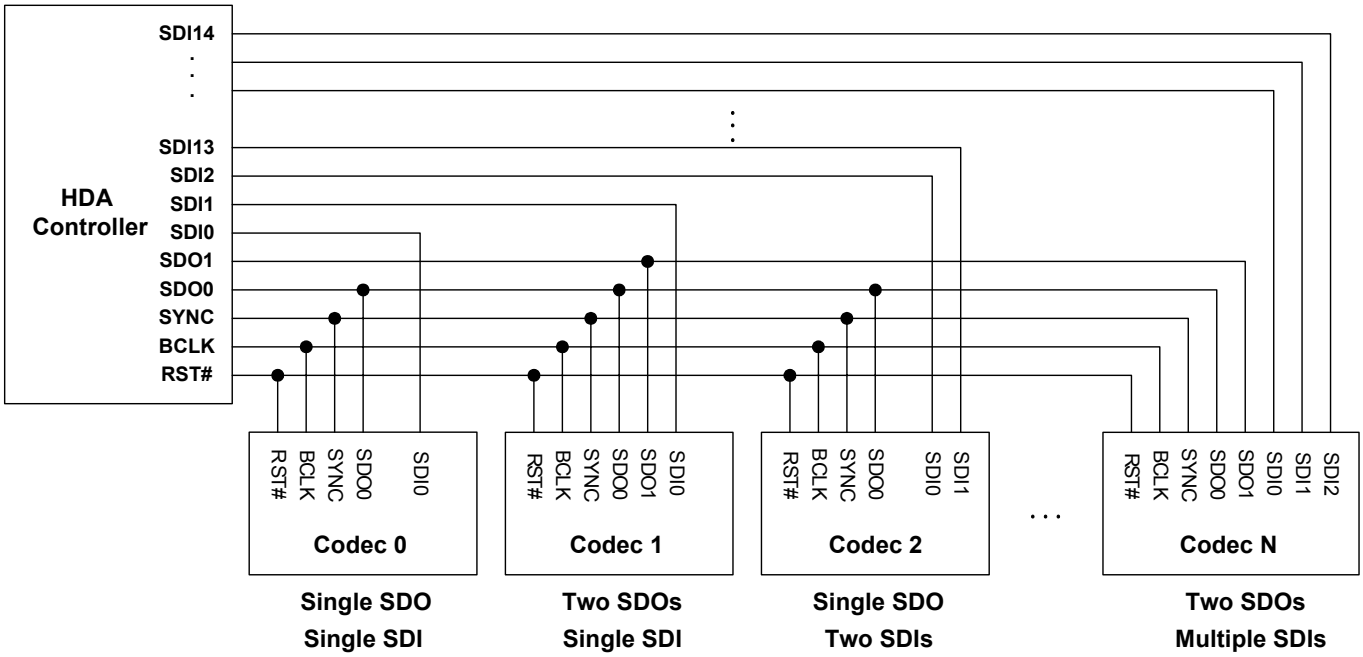


Figure 7. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be two blocks in the same stream to carry 96kHz samples (Figure 8).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 9).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

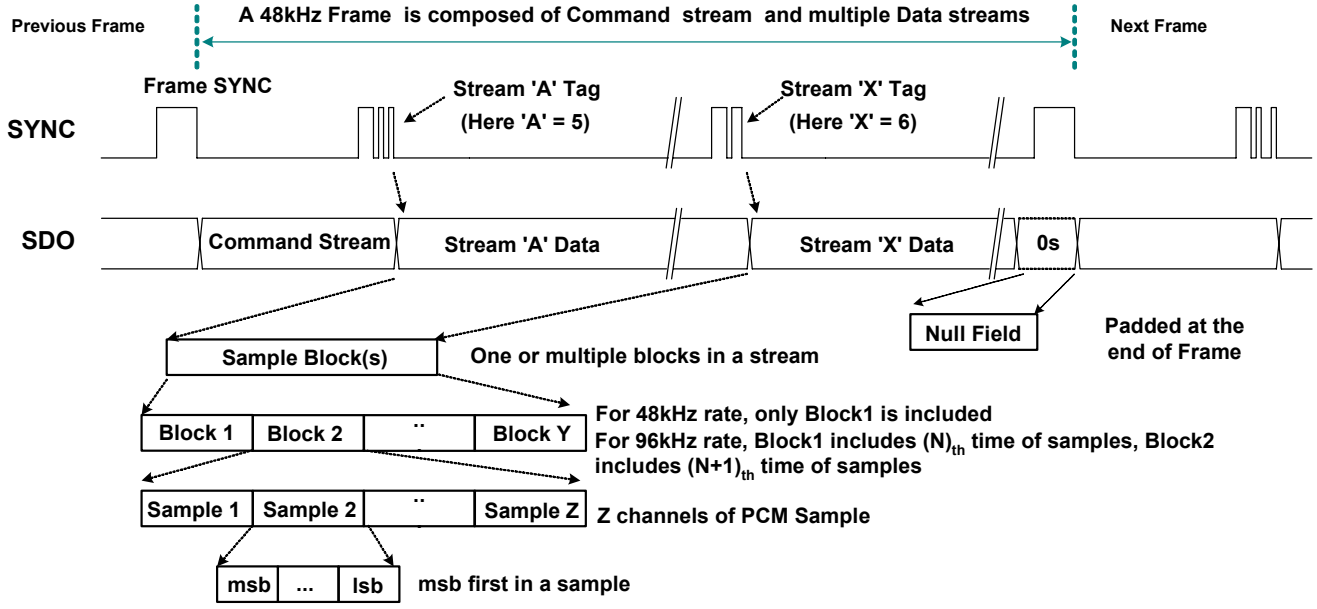


Figure 8. SDO Outbound Frame

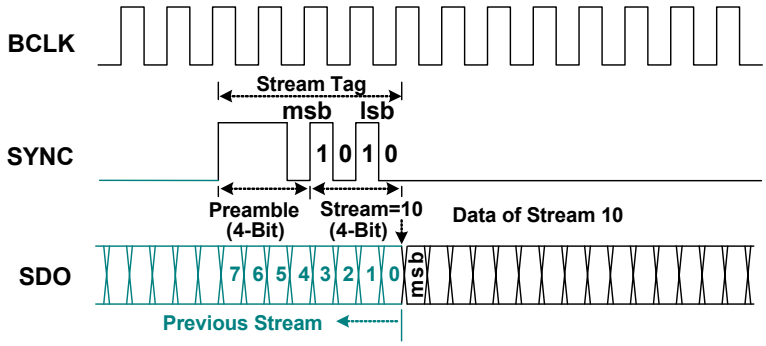


Figure 9. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines that the target codec supports multiple SDO capability, it enables the 'Stripe Control' bit in the controller's Output Stream Control Register to initiate a specific stream (Stream 'A' in Figure 10) to be transmitted on multiple SDOs. In this case, the MSB of the stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To ensure that all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

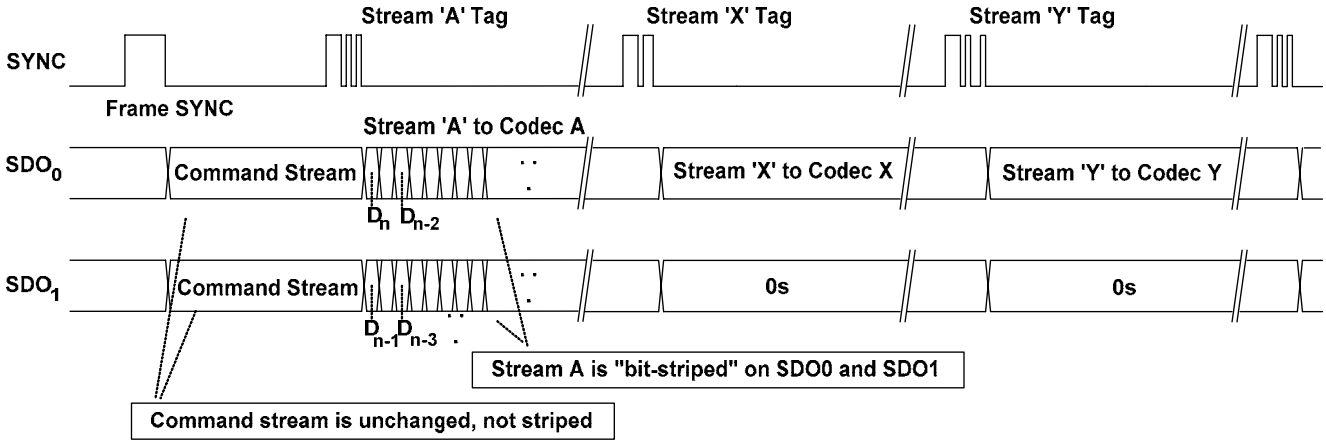


Figure 10. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), the SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 11).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 12).

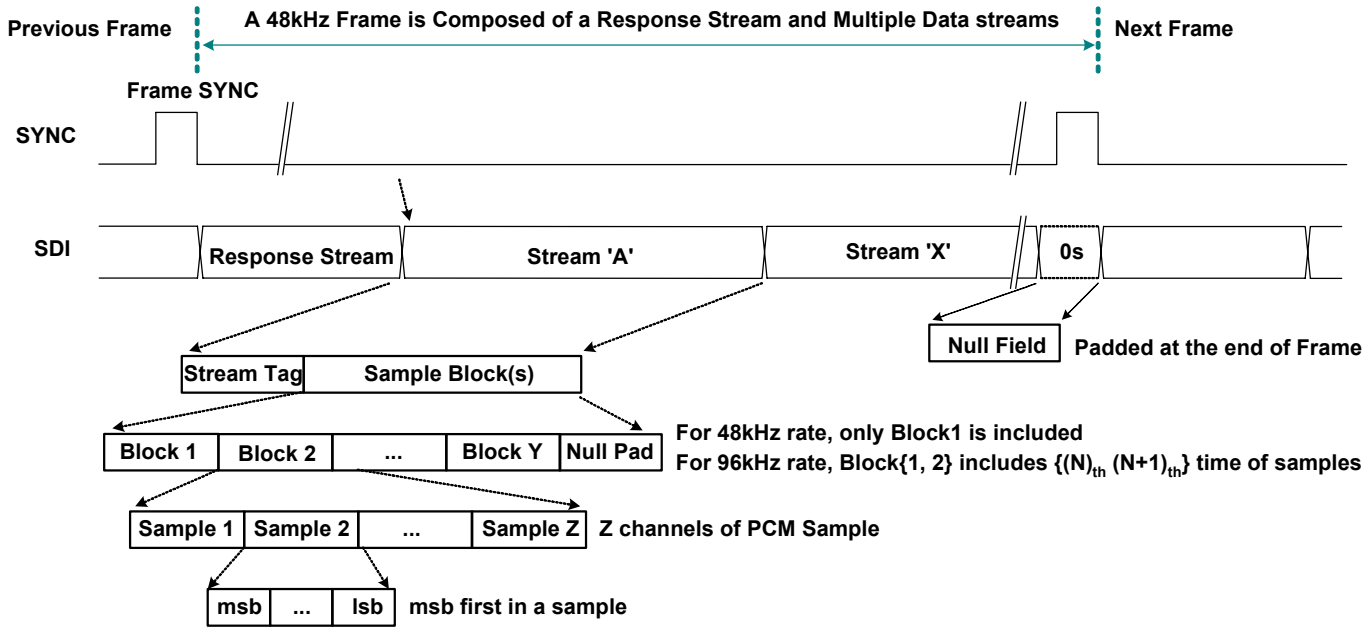


Figure 11. SDI Inbound Stream

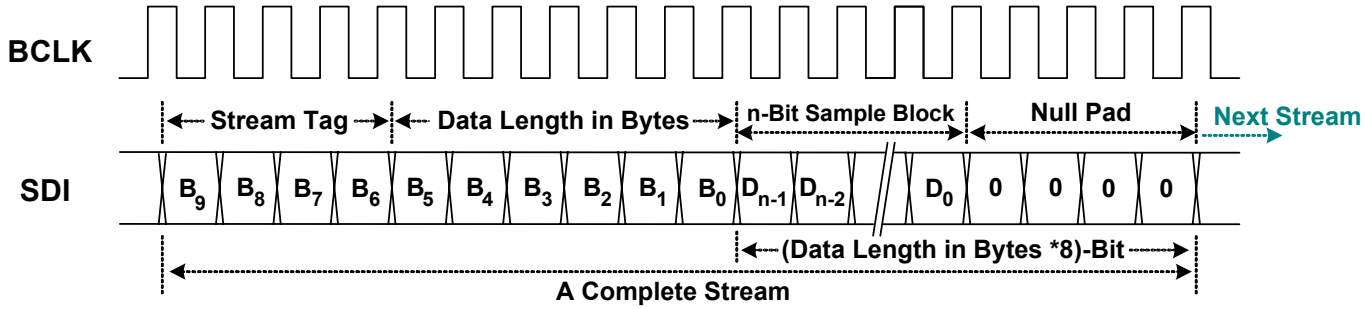


Figure 12. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data into separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

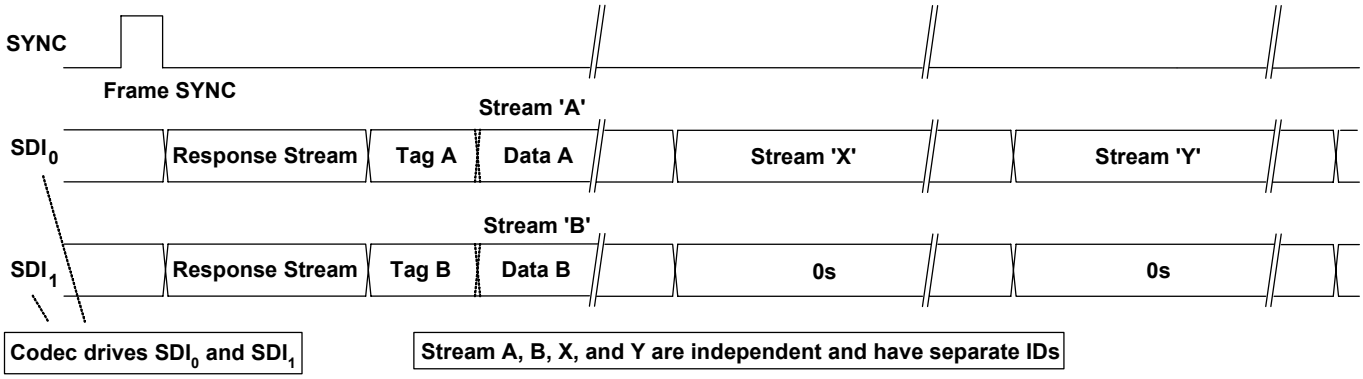


Figure 13. Codec Transmits Data Over Multiple SDIs

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 8, page 19, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 9, page 19, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence ‘12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)’ interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence *and* interleave n empty frames.

Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 10, page 20).

Table 8. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 9. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y^2NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y^2 (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y^4 (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame.
Y: One sample block in a frame.
Y^x: X sample blocks in a frame

Table 10. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-11^2- (repeat)
174.4kHz	12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-11^4- (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{ - } =NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYN

{11}=YNYNYNYNYNYNYNYNYNYNYN

{ - }=NN

44.1kHz 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz 12^2- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

174.4kHz 12^4- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset

2. Codec Reset

3. Codec changes its power state (for example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)

2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller

3. Software initiates power management sequences. Figure 14, page 22, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset

❷ When the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame

❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low

❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state

❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)

❼ Software is responsible for de-asserting RST# after a minimum of 100µs BCLK running time (the 100µsec provides time for the codec PLL to stabilize)

❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC

❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

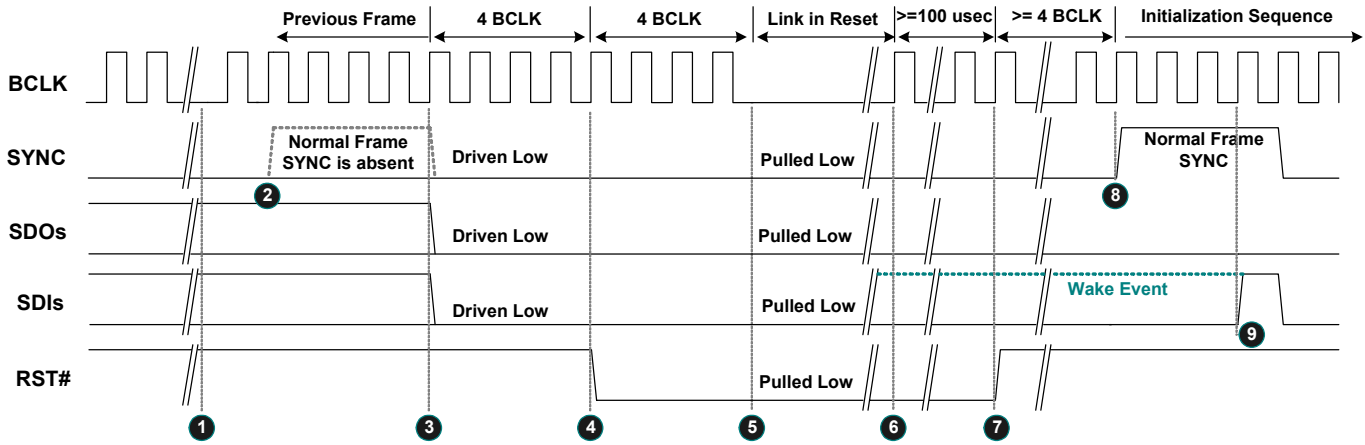


Figure 14. Link Reset Timing

7.3.2. Codec Reset

A 'Codec Reset' is initiated via the codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence will not be requested. In the extended power state, a function reset cannot initialize the register setting in power state D3. The Host SW needs to send a 'double function reset' to reset all settings.

7.3.3. Double Function Reset

Double Function Reset is executed by sending two Function Group resets back to back. This Function Group 'Double' reset shall do a full initialization and reset all settings to their power on defaults. This Double Reset is defined as two Function Group Reset verbs received without any other intervening valid verbs. The reset verbs are not required to be received in sequential frames, but there must not be any other verbs received in frames between the consecutive Function Group Reset verbs. It is allowed that there are several null commands received in frames between Function Group Reset verbs.

7.3.4. Codec Initialization Sequence

❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller

❷ The codec will stop driving the SDI during this turnaround period

❸❹❺❻ The controller drives SDI to assign a CAD to the codec

❼ The controller releases the SDI after the CAD has been assigned

❽ Normal operation state

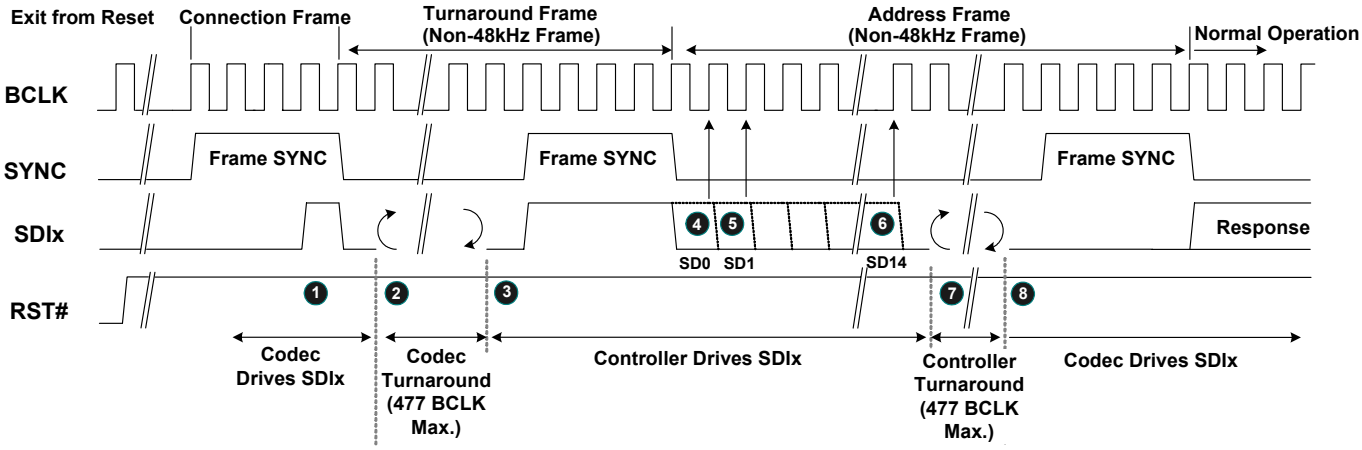


Figure 15. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 11 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 12 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 11. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 12. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 13. Supported Commands

Supported Verb	Get Verb	Set Verb	Root Node	Audio Function Group	Modem Function Group*1	HDMI Function Group*1	Vendor Define Group*1	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget*1	Volume Knob	Beep Generator	Vendor Define Widget
Get parameter	F00	-	Y	Y	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
Connection Select	F01	701	-	-	-	-	-	-	Y	Y	-	Y	-	-	-	-
Get Connection List Entry	F02	-	-	-	-	-	-	-	Y	Y	Y	Y	-	-	-	-
Processing State	F03	703	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Coefficient Index	D--	5--	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
Processing Coefficient	C--	4--	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
Amplifier Gain/Mute	B--	3--	-	-	-	-	-	-	Y	Y	Y	-	-	-	-	-
Stream Format	A--	2--	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Digital Converter 1	F0D	70D	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Digital Converter 2	F0D	70E	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Power State	F05	705	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Channel / Stream ID	F06	706	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
SDI Select	F04	704	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Pin Widget Control	F07	707	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Unsolicited Enable	F08	708	-	-	-	-	-	-	-	Y	-	-	-	Y	-	-
Pin Sense	F09	709	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
EAPD / BTL Enable	F0C	70C	-	-	-	-	-	-	-	-	-	-	-	-	-	-
All GPIO Control	F10-F1A	710-71A	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Beep Generator Control	F0A	70A	-	-	-	-	-	-	-	-	-	-	-	-	Y	-
Volume Knob Control	F0F	70F	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 0	F20	720	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 1	F20	721	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 2	F20	722	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 3	F20	723	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Config Default, Byte 0	F1C	71C	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 1	F1C	71D	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 2	F1C	71E	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 3	F1C	71F	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
RESET	-	7FF	-	Y	-	-	-	-	-	-	-	-	-	-	-	-

**1: The ALC888S does not support Modem/HDMI/Vendor groups and Power State widgets.*

Table 14. Supported Parameters

Supported Parameter	Parameter ID	Root Node	Audio Function Group	Modem Function Group*1	HDMI Function Group*1	Vendor Define Group*1	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget*1	Volume Knob	Beep Generator	Vendor Define Widget
Vendor ID	00	Y	-	-	-	-	-	-	-	-	-	-	-	-	-
Revision ID	02	Y	-	-	-	-	-	-	-	-	-	-	-	-	-
Subordinate Node Count	04	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
Function Group Type	05	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Audio Function Group Capabilities	08	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Audio Widget Capabilities	09	-	-	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
Sample Size, Rate	0A	-	Y	-	-	-	Y	Y	-	-	-	-	-	-	-
Stream Formats	0B	-	Y	-	-	-	Y	Y	-	-	-	-	-	-	-
Pin Capabilities	0C	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Input Amp Capabilities	0D	-	-	-	-	-	-	Y	-	Y	Y	-	-	-	-
Output Amp Capabilities	12	-	-	-	-	-	-	-	Y	Y	-	-	-	-	-
Connection List Length	0E	-	-	-	-	-	-	Y	Y	Y	Y	-	-	-	-
Supported Power States	0F	-	Y	-	-	-	Y	Y	Y	Y	Y	-	-	-	Y
Processing Capabilities	10	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
GPI/O Count	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volume Knob Capabilities	13	-	-	-	-	-	-	-	-	-	-	-	-	-	-

**1: The ALC888S does not support Modem/HDMI/Vendor groups and Power State widgets.*

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 15. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 16. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

The ALC888S-VC does not support Wake-Up events when in low power mode. All power management state changes in widgets are driven by software. Table 17 shows the System Power State Definitions.

In the ALC888S-VC, all the widgets, including output/input converters, support power control. Software may have various power states depending on system configuration.

Table 18 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-grained power control.

Table 17. System Power State Definitions

Power States	Definitions
D0	All power on. Individual DACs and ADCs can be powered up or down as required.
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up.
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference is off (D1 + analog reference off).
D3 (Hot)	Power still supplied. The codec stops the internal clock. State is maintained.
D3 (Cold)	All Power removed. State lost.

Table 18. Power Controls in NID 01h

Item	Description	D0	D1	D2	D3	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	Front DAC	Normal	PD	PD	PD	PD
	Surr DAC)	Normal	PD	PD	PD	PD
	Cen/Lfe DAC	Normal	PD	PD	PD	PD
	Side DAC	Normal	PD	PD	PD	PD
	Fout DAC	Normal	PD	PD	PD	PD
	LINE ADC	Normal	PD	PD	PD	PD
	MIX ADC	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down

Table 19. Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. S/PDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied
Front DAC powered down	Analog block and digital filter are powered down
Surr DAC powered down	Analog block and digital filter are powered down
CEN/LFE DAC powered down	Analog block and digital filter are powered down
SIDESURR DAC powered down	Analog block and digital filter are powered down
Fout DAC powered down	Analog block and digital filter are powered down
LINE ADC powered down	Analog block and digital filter are powered down. Data on SDATA-IN is quiet
MIX ADC powered down	Analog block and digital filter are powered down. Data on SDATA-IN is quiet
Headphone Driver powered down	All headphone drivers are powered down
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off

7.5.1. ALC888S-VC Additional Power Features

The ALC888S-VC is designed to meet Intel's low-power-state white paper and is ECR HDA-015B compliant. It meets the five attributes discussed in the white paper:

1. D3 state power < 30mW.

2. Exit latency (D3 to D0 transfer) < 10ms.

3. Audio pop/click suppression during D3 and D0 transition < -65dBV.

4. Supports Jack detection in D3 state.

5. D3 functions with or without the BITCLK

The ALC888S-VC minimizes D3 state idle mode power consumption and increases overall battery life in mobile systems.

In D3 mode, only a power on reset or a 'double function reset' resets all ALC888S-VC settings, cutting software configuration time spent entering/leaving D3 state, and reducing latency time for D3 to D0 transitions.

The ALC888S-VC supports Wake-Up events in D3 mode, including jack detection and GPIO status changes. If the HDA-Link was alive (with BCLK), the ALC888S-VC Wake-Up response is as normal. If no BITCLK is present, the ALC888S-VC drives the SDI high in order to wake up the system

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC888S-VC. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget. Some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, to get detailed information about supported parameters.

Table 20. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 21. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format

Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID)
15:0	Device ID=0888h

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 22. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC888S-VC is fully compliant
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC888S-VC is fully compliant
15:8	Revision ID. The vendor's revision number. 00h is for ALC888, 01h is for ALC888S, 02h is for ALC888S-VC, etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID

Note: The Root Node (NID=00h in the ALC888S-VC) supports this parameter.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node. For function group nodes, it provides the total number of widgets associated with this function node.

Table 23. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:16	Starting Node Number. The starting node number in the sequential widgets
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 24. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's.
8	UnSol Capable. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 25. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's.
16	Beep Generator. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group.
15:12	Reserved. Read as 0's.
11:8	Input Delay.
7:4	Reserved. Read as 0's.
3:0	Output Delay.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 26. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's
23:20	Widget Type 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets
15:11	Reserved. Read as 0's
10	Power Control 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0
4	Format Override
3	AmpParOvr, AMP Param Override
2	OutAmpPre. Out AMP Present
1	InAmpPre. In AMP Present
0	Stereo 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameters here provide default information about formats. Individual converters have their own parameters to provide supported formats if their 'Format Override' bit is set.

Table 27. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's
20	B32. 32-bit audio format support 0: Not supported 1: Supported
19	B24. 24-bit audio format support 0: Not supported 1: Supported
18	B20. 20-bit audio format support 0: Not supported 1: Supported
17	B16. 16-bit audio format support 0: Not supported 1: Supported
16	B8. 24-bit audio format support 0: Not supported 1: Supported
15:12	Reserved. Read as 0's
11	R12. 384kHz (=8*48kHz) rate support 0: Not supported 1: Supported
10	R11. 192kHz (=4*48kHz) rate support 0: Not supported 1: Supported
9	R10. 176.4kHz (=4*44.1kHz) rate support 0: Not supported 1: Supported
8	R9. 96kHz (=2*48kHz) rate support 0: Not supported 1: Supported
7	R8. 88.2kHz (=2*44.1kHz) rate support 0: Not supported 1: Supported
6	R7. 48kHz rate support 0: Not supported 1: Supported
5	R6. 44.1kHz rate support 0: Not supported 1: Supported
4	R5. 32kHz (=2/3*48kHz) rate support 0: Not supported 1: Supported
3	R4. 22.05kHz (=1/2*44.1kHz) rate support 0: Not supported 1: Supported
2	R3. 16kHz (=1/3*48kHz) rate support 0: Not supported 1: Supported
1	R2. 11.025kHz (=1/4*44.1kHz) rate support 0: Not supported 1: Supported
0	R1. 8kHz (=1/6*48kHz) rate support 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the 'Format Override' bit is set.

Table 28. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's
2	AC3 0: Not supported 1: Supported
1	Float32 0: Not supported 1: Supported
0	PCM 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 29. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's
15:8	VREF Control Capability. '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD.

7:6	5	4	3	2	1	0
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z

Bit	Description
7	L-R Swap. Indicates the capability of swapping the left and rights
6	Balanced I/O Pin. '1' indicates this pin complex has balanced pins.
5	Input Capable. '1' indicates this pin complex supports input.
4	Output Capable. '1' indicates this pin complex supports output.
3	Headphone Drive Capable. '1' indicates this pin complex has an amplifier to drive a headphone.
2	Presence Detect Capable. '1' indicates this pin complex can detect whether there is anything plugged in.
1	Trigger Required. '1' indicates whether a software trigger is required for an impedance measurement.
0	Impedance Sense Capable. '1' indicates this pin complex can perform analog sense on the attached device to determine its type

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 30. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. '0' means the gain is fixed
7	Reserved. Read as 0
6:0	Offset Indicates which step is 0dB

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 31. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable
30:23	Reserved. Read as 0
22:16	Step Size Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB
15	Reserved. Read as 0
14:8	Number of Steps Indicates the number of steps in the gain range. '0' means the gain is fixed
7	Reserved. Read as 0
6:0	Offset. Indicates which step is 0dB

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 32. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0
7	Short Form 0: Short Form 1: Long Form
6:0	Connect List Length Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget)

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 33. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's
3	D3Sup 1: Power state D3 is supported
2	D2Sup 1: Power state D2 is supported
1	D1Sup 1: Power state D1 is supported
0	D0Sup 1: Power state D0 is supported

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 34. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's
15:8	NumCoeff. Number of Coefficient
7:1	Reserved. Read as 0's
0	Benign 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 35. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0 The ALC888S-VC does not support GPIO wake up function
30	GPIUnsol=1 The ALC888S-VC supports GPIO unsolicited response
29:24	Reserved. Read as 0's
23:16	NumGPIs=00h No GPI pin is supported
15:8	NumGPOs=00h No GPO pin is supported
7:0	NumGPIOs=02h Three GPIO pins are supported

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 36. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

Bit	Description
31:8	Reserved. Read as 0's
7	Delta 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps The number of steps in the range of the Volume Control Knob

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 37. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F01h	0's

Codec Response Format

Response [31:0]
Bit[7:0] are Connection Index

Codec Response for Analog Port-A/B/C/D/E/F/G/H

Bit	Description
31:8	0's
7:0	Connection Index Currently Set (Default value is 00h) 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Dh 02h: Sum Widget NID=0Eh 03h: Sum Widget NID=0Fh 04h: Sum Widget NID=26h Other: Reserved

Codec Response for first Digital Pin S/PDIF-OUT 1Eh

Bit	Description
31:8	0's
7:0	Connection Index Currently Set (Default value is 00h) 00h: Digital Converter (S/PDIF-OUT) NID=06h Other: Reserved

Codec Response for second Digital Pin S/PDIF-OUT 11h

Bit	Description
31:8	0's
7:0	Connection Index Currently Set (Default value is 00h) 00h: Digital Converter (S/PDIF-OUT) NID=10h Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 38. Verb – Set Connection Select (Verb ID=701h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 39. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F02h	Offset Index - N[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=08h (LINE ADC)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 23h (Sum Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=09h (MIX ADC)

Bit	Description
15:8	Connection List Entry (N+3), (N+2) and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 22h (Sum Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Ah (S/PDIF-IN Converter)

Bit	Description
31:8	Connection List Entry (N+3), (N+2) and (N+1) Returns 000000h
7:0	Connection List Entry (N) Returns 1Fh (S/PDIF-IN Pin Widget) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Bh (Mixer)

Bit	Description
31:24	Connection List Entry (N+3) Returns 1Bh (Pin Complex – LINE2) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Complex – LINE1) for N=0~3 Returns 14h (Pin Complex – FRONT) for N=4~7 Returns 00h for N>7
15:8	Connection List Entry (N+1) Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7 Returns 17h (Pin Complex – SIDESURR) for N=8~11 Returns 00h for N>11
7:0	Connection List Entry (N) Returns 18h (Pin Complex – MIC1) for N=0~3 Returns 1Ch (Pin Complex – CD) for N=4~7 Returns 16h (Pin Complex – CEN/LFE) for N=8~11 Returns 00h for N>11

Codec Response for NID=0Ch (Front Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 02h (Front DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Dh (Surround Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 03h (Surround DAC) for N=0~3 Returns 00h for N>3.

Codec Response for NID=0Eh (Cen/Lfe Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 04h (Cen/Lfe DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=0Fh (Side-Surr Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 05h (Front DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=26h (Fout Sum)

Bit	Description
31:24	Connection List Entry (N) Returns 00h
23:16	Connection List Entry (N+2) Returns 00h
15:8	Connection List Entry (N+1) Returns 0Bh (Mixer) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 25h (Fout1 DAC) for N=0~3 Returns 00h for N>3

Codec Response for NID=14h~1Bh (Port-A to port-H)

Bit	Description
31:24	Connection List Entry (N+3) Returns 0Fh (Sum Widget NID=0Fh) for N=0~3 Returns 00h for n>3
23:16	Connection List Entry (N+2) Returns 0Eh (Sum Widget NID=0Eh) for N=0~3 Returns 00h for N>3
15:8	Connection List Entry (N+1) Returns 0Dh (Sum Widget NID=0Dh) for N=0~3 Returns 00h for N>3
7:0	Connection List Entry (N) Returns 0Ch (Sum Widget NID=0Ch) for N=0~3 Returns 26h (Sum Widget NID=26h) for N=4~7 Returns 00h for N>7

Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)

Bit	Description
31:16	Connection List Entry (N+3) and (N+2) Returns 0000h
15:8	Connection List Entry (N+1) Returns 00h
7:0	Connection List Entry (N) Returns 06h (S/PDIF-OUT converter) for N=0~3 Returns 00h for N>3

Codec Response for NID= 22h/23h/ (Sum Widget before MIX/LINE ADCs)

Bit	Description
31:24	Connection List Entry (N+3) Returns 1Bh (Pin Complex – LINE2) for N=0~3 Returns 15h (Pin Complex-SURR) for N=4~7 Returns 00h for N>7
23:16	Connection List Entry (N+2) Returns 1Ah (Pin Complex – LINE1) for N=0~3 Returns 14h (Pin Complex – FRONT) for N=4~7 Returns 0Bh (Sum Widget) for N=8~11 Returns 00h for N>11
15:8	Connection List Entry (N+1) Returns 19h (Pin Complex – MIC2) for N=0~3 Returns 1Dh (Pin Complex – PCBEEP) for N=4~7 Returns 17h (Pin Complex – SIDESURR) for N=8~11 Returns 00h for N>11
7:0	Connection List Entry (N) Returns 18h (Pin Complex – MIC1) for N=0~3 Returns 1Ch (Pin Complex – CD) for N=4~7 Returns 16h (Pin Complex – CEN/LFE) for N=8~11 Returns 00h for N>11

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 40. Verb – Get Processing State (Verb ID=F03h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F03h	0's

Codec Response Format

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.6. Verb – Set Processing State (Verb ID=703h)

Table 41. Verb – Set Processing State (Verb ID=703h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 42. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Dh	0's

Codec Response Format

Response [31:0]
Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Defined Registers)

Bit	Description
31:16	Reserved. Read as 0's
15:0	Coefficient Index

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 43. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 44. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Defined Registers)

Bit	Description
31:16	Reserved. Read as 0's
15:0	Processing Coefficient

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 45. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 46. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Bh	'Get' payload [15:0]

Codec Response Format

Response [31:0]
Bit[7:0] are responsible for 'Get'

'Get' Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0's
3:0	Index[3:0] for Input Source Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored

Codec Response for 08h (LINE ADC) and 09h (MIX ADC)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0. (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –16.5B~+30dB in 1.5dB steps. Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute)

Codec Response for NID=0Bh (MIXER Sum Widget)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index) Bit-15 is 1 in 'Get Amplifier Gain': Read as 0. (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –34.5dB~+12dB in 1.5dB steps. Bit-15 is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute)

Codec Response for NID=0Ch~0Fh (Sum Widget: Front, Surr, CenLfe, SideSurr)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute 1: Mute Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. (No Input Amplifier Gain) Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –46.5dB~0dB in 1.5dB steps.

Codec Response for NID=14h~1Bh (Pin Complex: Front, Surr, CenLfe, SideSurr, MIC1, MIC2, LINE1, LINE2)

Bit	Description
31:8	0's
7	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0 Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute 1:Mute (NID=14h~1Bh,Default=1)
6:0	Bit-15 is 0 in 'Get Amplifier Gain': Read as 0's Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)

Codec Response to Other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 47. Verb – Set Amplifier Gain (Verb ID=3h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp. '1' indicates output amplifier gain will be set
14	Set Input Amp. '1' indicates input amplifier gain will be set
13	Set Left Amp. '1' indicates left amplifier gain will be set
12	Set Right Amp. '1' indicates right amplifier gain will be set
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets) 5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the 'Set Input Amp' bit is not set
7	Mute 0: Unmute 1: Mute (-∞gain)
6:0	Gain[6:0]. A 7-bit step value specifying the amplifier gain.

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 48. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Bit[15:0] are converter format

Codec Response for NID=02h~06h, 10h, 25h (Output Converters: Front, Surr, Cen/Lfe, SideSurr, 1st S/PDIF-OUT, 2nd S/PDIF-OUT, Fout DAC).

Codec Response for NID=08h~0Ah (Input Converters: LINE, MIX DAC, and S/PDIF-IN)

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC888S-VC does not support Divisor. Always read as 000b
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: reserved
3:0	Number of Channels 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 49. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
CAd=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0
15	Stream Type (TYPE) 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE) 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT) 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV) 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0
6:4	Bits per Sample (BITS) 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h)

Table 50. Verb – Get Power State (Verb ID=F05h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's
5:4	PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set
3:2	Reserved. Read as 0's
1:0	PS-Set, Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.16. Verb – Set Power State (Verb ID=705h)

Table 51. Verb – Set Power State (Verb ID=705h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's
5:4	PS-Act. Actual Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's
1:0	PS-Set. Set Power State [1:0] 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F06h	0's

Codec Response Format

Response [31:0]
Stream & Channel [7:0]

Codec Response for NID=02h~06h, 10h, 25h (Output Converters: Front, Surr, Cen/Lfe, SideSurr, 1st S/PDIF-OUT, 2nd S/PDIF-OUT, Fout DAC)

Codec Response for NID=08h~0Ah (Input Converters: LINE ADC, MIX DAC, and S/PDIF-IN)

Bit	Description
31:8	Reserved. Read as 0's
7:4	Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 52. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's
7:4	Set Stream[3:0] The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0] The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel

Note: This verb assigns stream and channel for output converters (NID=02h~06h 10h, 25h) and input converters (NID=08h~0Ah). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 53. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 11h, 1Fh
(Pin Complex: Front, Surr, CenLfe, SideSurr, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, 1st S/PDIF-OUT, 2nd S/PDIF-OUT and S/PDIF-IN)

Bit	Description
31:1	Reserved. Read as 0's
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for a I/O unit) 0: Disabled 1: Enabled
6	Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit) 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled
4:	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 54. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0] for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 11h, 1Fh: (Pin Complex: Front, Surr, CenLfe, SideSurr, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, 1st S/PDIF-OUT, 2nd S/PDIF-OUT and S/PDIF-IN)

Bit	Description
31:1	Reserved. Read as 0's
7	H-Phn Enable 0: Disabled 1: Enabled
6	Out Enable 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for a I/O unit) 0: Disabled 1: Enabled
4:	Reserved
2:0	VrefEn (Vrefout Enable Control) 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD) 101b: 100% of AVDD 110b~111b: Reserved

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

Table 55. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= F08h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (GPIO), 14h~1Bh (Port A to H)

Bit	Description
31:8	Reserved. Read as 0's
7	Unsolicited Response is Enabled 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's
3:0	Assigned Tag for Unsolicited Response The tag[3:0] is assigned by software to determine which widget generates unsolicited responses

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enables a widget to generate an unsolicited response.

Table 56. Verb – Set Unsolicited Response Control (Verb ID=708h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'EnableUnsol' in Command Bit[7:0] for NID=01h (GPIO), 14h~1Bh (Port A to H)

Bit	Description
31:8	Reserved. Read as 0's
7	Enable Unsolicited Response 0: Disable 1: Enable
6:4	Reserved. Read as 0's
3:0	Tag for Unsolicited Response Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 57. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= F09h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID = 14h~1Bh, 1Eh, 1Fh

Bit	Description
31	Presence Detect Status 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance The ALC888S does not support hardware impedance detection. This field is read as 0's.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h)

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 58. Verb – Execute Pin Sense (Verb ID=709h)

Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= 709h	Right Channel[0]

Codec Response Format

Response [31:0]
0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's
0	Right (Ring) Channel Select 0: Sense Left channel (Tip) 1: Sense Right channel (Ring) The ALC888S does not support hardware impedance sensing and will ignore this control.

8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Reads the 32-bit sticky register for each Pin Widget configured by software.

Table 59. Verb – Get Configuration Default (Verb ID=F1Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= F1Ch	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Eh, 11h and 1Fh

Bit	Description
31:0	32-bit configuration information for each pin widget

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

Table 60. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Note: Supported by Pin Widget NID=14h~1Bh, 1Eh, 11h, and 1Fh. Other widgets will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 61. Verb – Get BEEP Generator (Verb ID= F0Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID= F1Bh	0's

Codec Response Format

Response [31:0]
Divider [7:0]

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is 48kHz/(255*4)=47Hz The highest tone is 48kHz/(1*4)=12kHz A value of 00h in F[7:0] disables internal BEEP generator and allows external PCBEEP input

Codec Response for Other NID

Bit	Description
31:0	0's

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 62. Verb – Set BEEP Generator (Verb ID= 70Ah)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=71Bh	Divider [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved
7:0	Frequency Divider, F[7:0] The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0] The lowest tone is 48kHz/(255*4)=47Hz The highest tone is 48kHz/(1*4)=12kHz A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.29. Verb – Get GPIO Data (Verb ID=F15h)

Table 63. Verb – Get GPIO Data (Verb ID= F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Data. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Data The value written (output) or sensed (input) on the corresponding pin if it is enabled

Codec Response for Other NID

Bit	Description
31:0	0's

8.30. Verb – Set GPIO Data (Verb ID=715h)

Table 64. Verb – Set GPIO Data (Verb ID= 715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Output Data. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Output Data The value written determines the value driven on a pin that is configured as an output pin

Codec Response for All NID

Bit	Description
31:0	0's

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 65. Verb – Get GPIO Enable Mask (Verb ID= F16h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F16h	0's

Codec Response Format

Response [31:0]
EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	Reserved
1:0	GPIO[1:0] Enable Mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 66. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=716h	Enable Mask [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Enable Mask. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Enable Mask 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 67. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F17h	0's

Codec Response Format

Response [31:0]
Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Direction Control. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 68. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=717h	Direction [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Direction Control. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.35. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 69. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F19h	0's

Codec Response Format

Response [31:0]
UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's

8.36. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 70. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=719h	UnsolEnable [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC888S-VC
1:0	GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.
Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb-'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's

8.37. Verb – Function Reset (Verb ID=7FFh)

Table 71. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01H)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=01h	Verb ID=7FFh	0's

Codec Response Format

Response [31:0]
0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's

Note: The Function Reset command causes all widgets in the ALC888S-VC to return to their power on default state.

8.38. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

Table 72. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=F0Dh/F0Eh	0's

Codec Response Format

Response [31:0]
Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=06h and 10h (1st and 2nd S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0])
NID=06h and 10h (1st and 2nd S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's
15	Reserved. Read as 0's
14:8	CC[6:0] (Category Code)
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer Format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Dh)
NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Eh)

Bit	Description (part of S/PDIF-IN Channel Status)
31:16	Reserved. Read as 0’s
15	Reserved. Read as 0’s
14:8	CC[6:0] (Category Code)
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer Format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	Reserved
1	In‘V’alid. V Bit in Sub-Frame of S/PDIF-IN 0: Data X and Y are valid, or S/PDIF-IN is not locked 1: At least one of data X and Y is invalid
0	Digital Enable. DigEn 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0’s

8.39. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 73. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Xh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Yh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=06h and 10h (1st and 2nd S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level)
6	PRO (Professional or Consumer Format) 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type) 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright) 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis) 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame)
1	V for Validity Control (control V bit and data in Sub-Frame)
0	Digital Enable. DigEn 0: OFF 1: ON

'Payload' in Set Control 2 for NID=06h and 10h (1st and 2nd S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's
6:0	CC[6:0] (Category Code)

'Payload' in Set Control 1 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:1	Reserved
0	Digital Enable. DigEn 0: OFF 1: ON

'Payload' in Set Control 2 for NID=0Ah (S/PDIF-IN)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7:0	Reserved. Read as 0's

Note: Other widgets will ignore this verb.

8.40. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/D22h/F23h)

32-bit Read/Write register for Audio Function Group (NID=01h)

Table 74. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=01h	Verb ID=F20h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h

Bit	Description
31:16	Subsystem ID[23:8]. (Default=10ECh)
15:8	Subsystem ID[7:0]. (Default=08h).
7:0	Assembly ID[7:0]. (Default=88h).

8.41. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Table 75. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=01h	Verb ID=723h, 722h, 721h, 720h	Label [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for all NID

Bit	Description
31:0	0's

8.42. Get/Set EAPD Enable (VID=70Ch/F0Ch)

Table 76. Verb – Get/Set EAPD [31:0]

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=Xh	Verb ID=F0Ch	0s

Codec Response Format

Response [31:0]
Bit[1] is EAPD Control

CODEC response in Get Command for NID=14h (LINE-OUT Pin Widget), 15h (HP-OUT Pin Widget)

Bit	Description
31:3	Reserved
2	L-R Swap The ALC888S-VC does not support swapping left and right channel, it is read as 0.
1	EAPD Enable 0: EAPD pin state is not controlled by power state of corresponding pin widget. 1: EAPD pin state is controlled by power state of corresponding pin widget.
0	BTL Enable The ALC888S-VC does not support BTL output, it is read as 0.

CODEC Response in Get Command for other NID

Bit	Description
31:0	0's.

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=Xh	Verb ID=70Ch	Bit[1] is EAPD Control

Codec Response Format

Response [31:0]
0s

CODEC Response in Set Command for all nodes

Bit	Description
31:0	0's.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 77. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply					
Digital Power for Core	DVDD	3.0	3.3	3.6	V
Digital Power for HDA Link	DVDD-IO*	1.5	3.3	3.6	V
Analog	AVDD**	3.3	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-	-	+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
All Pins	Pass 3500V				

**: The digital link power DVDD-IO must be lower than the digital core power DVDD.*
***: The standard testing condition before shipping is AVDD = 5.0V unless specified. Customer designing with a different AVDD should contact Realtek technical support representatives for special testing support.*

9.1.2. Threshold Voltage

DVDD= 3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 78. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage (HDA link)	V_{IL}	-	-	0.30*DVDDIO	V
High Level Input Voltage (HDA link)	V_{IH}	0.65*DVDDIO	-	-	V
Low Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V_{IL}	-	-	0.44*DVDD (1.45)	V
High Level Input Voltage (S/PDIF-IN/OUT, GPIOs)	V_{IH}	0.56*DVDD (1.85)	-	-	V
High Level Output Voltage	V_{OH}	0.9*DVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

9.1.3. Digital Filter Characteristics

Table 79. Digital Filter Characteristics

Filter	Description	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	0.45*Fs	kHz
	Stopband	0.60*Fs	-	-	kHz
	Stopband Rejection	-	-76.0	-	dB
	Passband Frequency Response	-	±0.02	-	dB
DAC Lowpass Filter	Passband	0	-	0.45*Fs	kHz
	Stopband	0.60*Fs	-	-	kHz
	Stopband Rejection	-	-78.5	-	dB
	Passband Frequency Response	-	±0.020	-	dB

Note: Fs=Sample rate.

9.1.4. S/PDIF Input/Output Characteristics

DVDD= 3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 80. S/PDIF Input/Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V
S/PDIF-IN High Level Input	V_{IH}	1.85	-	-	V
S/PDIF-IN Low Level Input	V_{IL}	-	-	1.45	V
S/PDIF-IN Bias Level	Vt	-	1.65	-	V

9.2. AC Characteristic

9.2.1. Link Reset and Initialization Timing

Table 81. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	µs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	20	-	-	µs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time

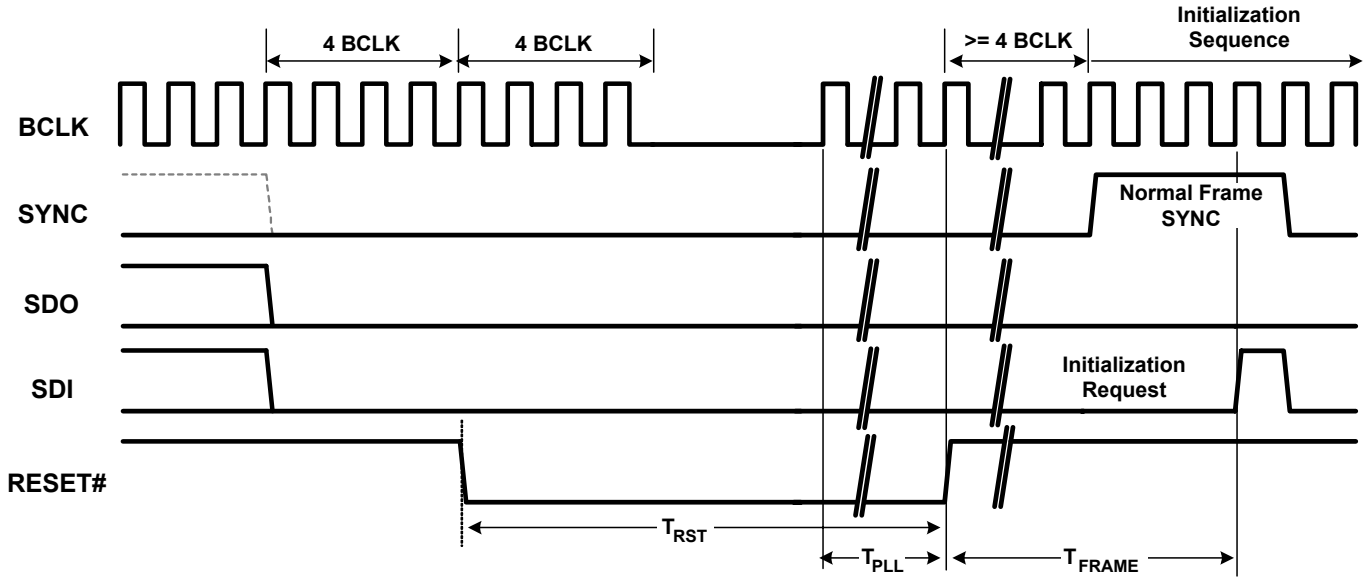


Figure 16. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 82. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency	-	-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	T_{low}	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF external load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns

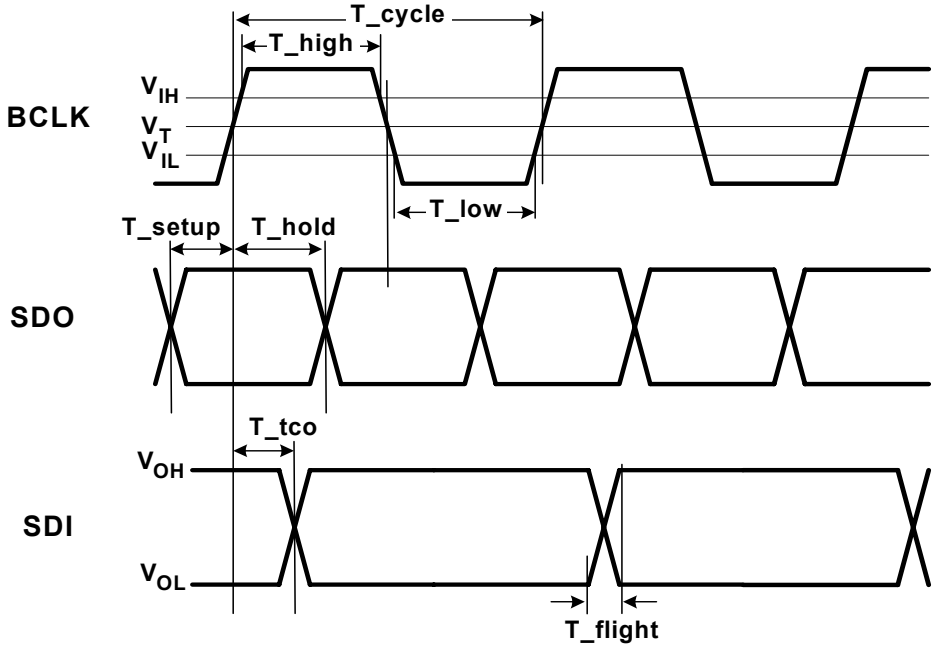


Figure 17. Link Signals Timing

9.2.3. S/PDIF Output and Input Timing

Table 83. S/PDIF Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency	-	-	3.072	-	MHz
S/PDIF-OUT Period *1	T_{cycle}	-	325.6	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns
S/PDIF-IN Period *2	T_{cycle}	-	325.6	-	ns
S/PDIF-IN Jitter	T_{jitter}	-	-	10	ns
S/PDIF-IN High Level Width	T_{High}	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)
S/PDIF-IN Low Level Width	T_{Low}	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)

**1: Bit parameters for 48kHz sample rate of S/PDIF-OUT*
**2: Bit parameters for 48kHz sample rate of S/PDIF-IN*

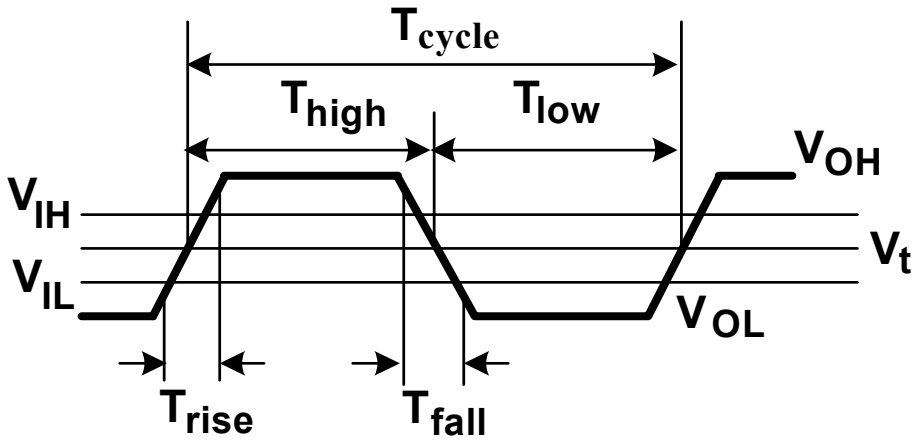


Figure 18. Output and Input Timing

9.2.4. Test Mode

The ALC888S-VC does not support codec test mode or Automatic Test Equipment (ATE) mode.

9.3. Analog Performance

Standard Test Conditions

- Tambient=25 oC, DVDD=3.3V ±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz

Table 84. Analog Performance

Parameter	Min	Typical	Max	Units
Full Scale Input Voltage				
All Inputs (gain=0dB)	-	1.6	-	Vrms
ADC	-	1.1	-	Vrms
Full Scale Output Voltage				
DAC	-	1.4	-	Vrms
Headphone Amplifier Output@32Ω Load	-	1.0	-	Vrms
S/N (A Weighted)				
ADC	-	90	-	dB FSA
DAC	-	96	-	dB FSA
Headphone Amplifier Output@32Ω Load	-	95	-	dB FSA
THD+N				
ADC	-	-84	-	dB FS
DAC	-	-90	-	dB FS
Headphone Amplifier Output@32Ω Load	-	-80	-	dB FS
Frequency Response				
ADC	10	-	0.45*Fs	Hz
DAC	0	-	0.45*Fs	Hz
Power Supply Rejection	-	-50	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (gain=0dB)	-	47	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-amplified Output	-	100	-	Ω
Digital Power Supply Current (normal operation)				
DVDD=3.3V	-	TBD	-	mA
Digital Power Supply Current (power down mode)				
DVDD=3.3V	-	TBD	-	mA
Analog Power Supply Current (normal operation)				
AVDD=5.0V	-	TBD	-	mA
Analog Power Supply Current (power down mode)				
AVDD=5.0V	-	TBD	-	mA
VREFOUTx Output Voltage	2.25	2.50	3.75	V
VREFOUTx Output Current	-	5	-	mA

Note: Fs=Sample Rate.

10. Application Circuits

If a digital microphone and GPIO are not used, the ALC888S-VC is pin compatible with the ALC888 series. To get the best compatibility in hardware design and software driver, any modification should be confirmed by Realtek. Realtek may update the latest application circuits onto our web site (www.realtek.com.tw) without modifying this datasheet.

10.1. Filter Connection

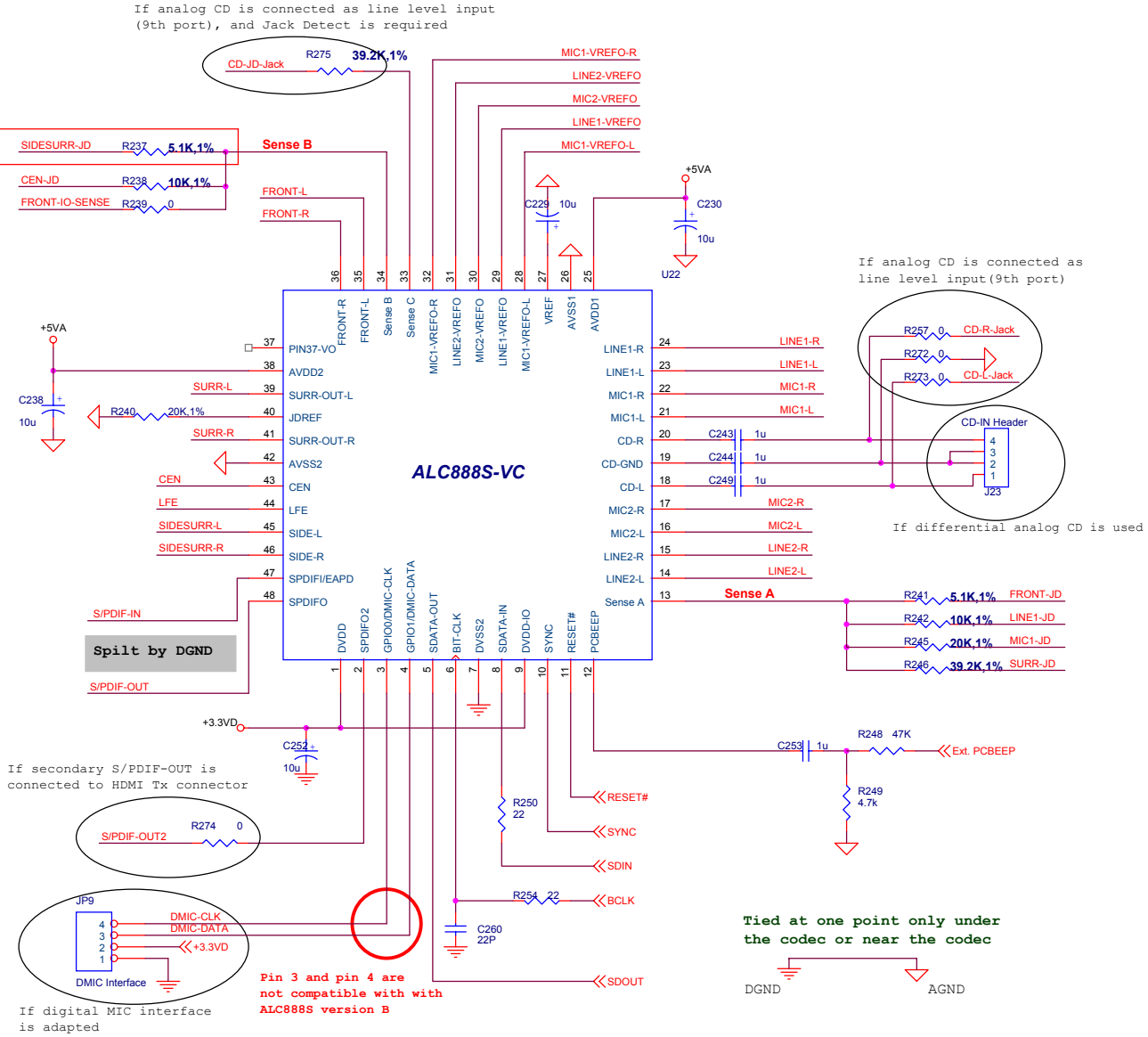


Figure 19. Filter Connection

10.2. Onboard Front Panel Header Connection

Option 1 in Figure 20 comes from by Intel's front panel IO connectivity design guide. A drawback of this option is that the ports connected to the front panel must use the same jack detection pin. According to the HD Audio standard specification, ports A/B/C/D use 'Sense A' as the jack detect pin; ports E/F/G/H use 'Sense B' as the jack detect pin. This is not a good option when the system integrators want to use port-A (pin 39/41) and port-F (pin 16/17) to be the front panel ports, as 'Sense A' and 'Sense B' cannot be tied together.

Option 2 in Figure 20 shows an alternative front panel header design that is also compatible with standard front panel I/O cable. The option 2 header design lets the two ports use an individual sense pin, and is compatible with current HD Audio front panel cable.

For the best compatibility with long front panel cable may not follow Intel's Front Panel I/O Connectivity standard, the option 2 header design has good ground loop is strongly recommended. The main drawback of option 2 is not suitable for AC'97 front cable

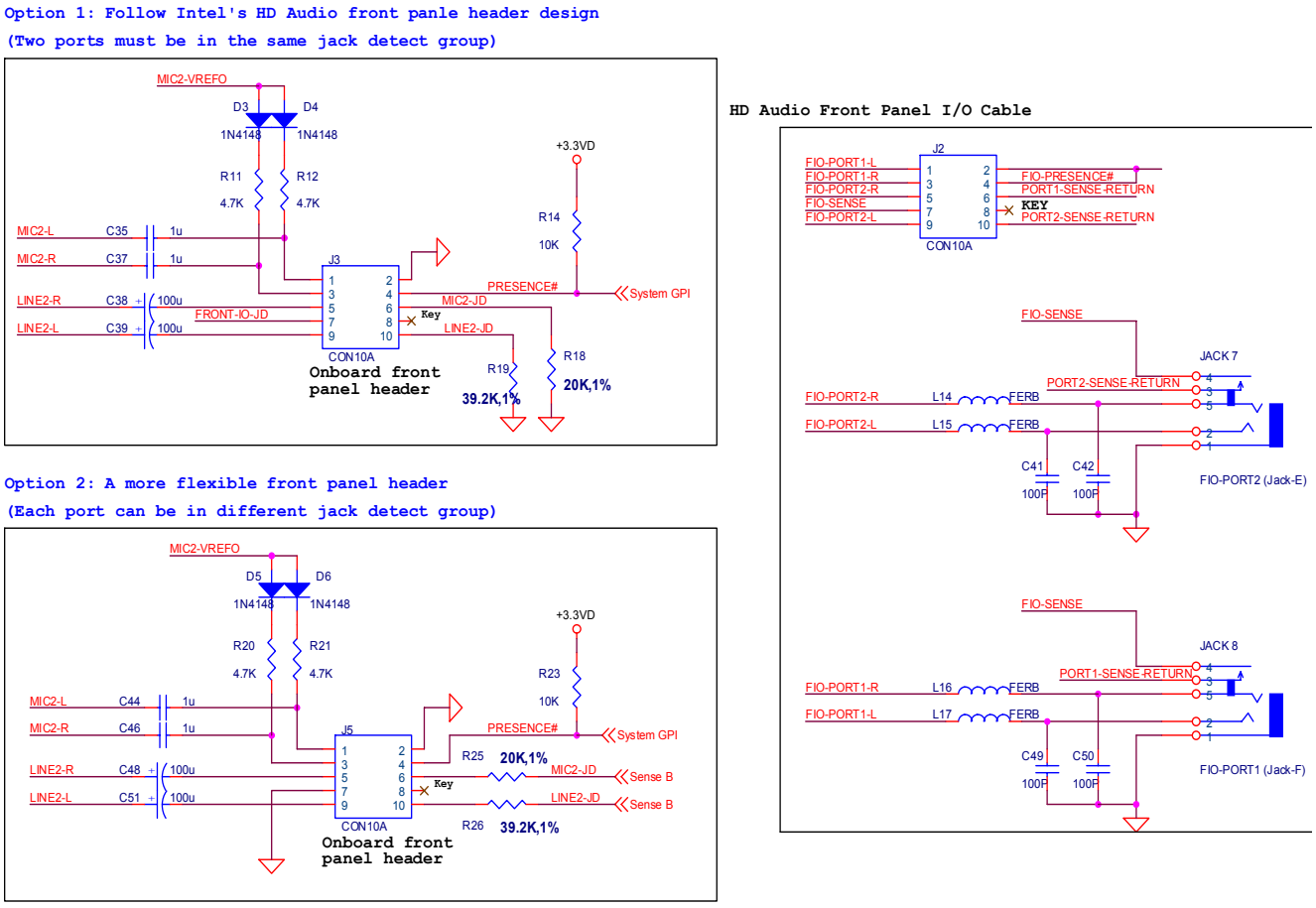


Figure 20. Front Panel Header Connection

10.3. Jack Connection on Rear Panel

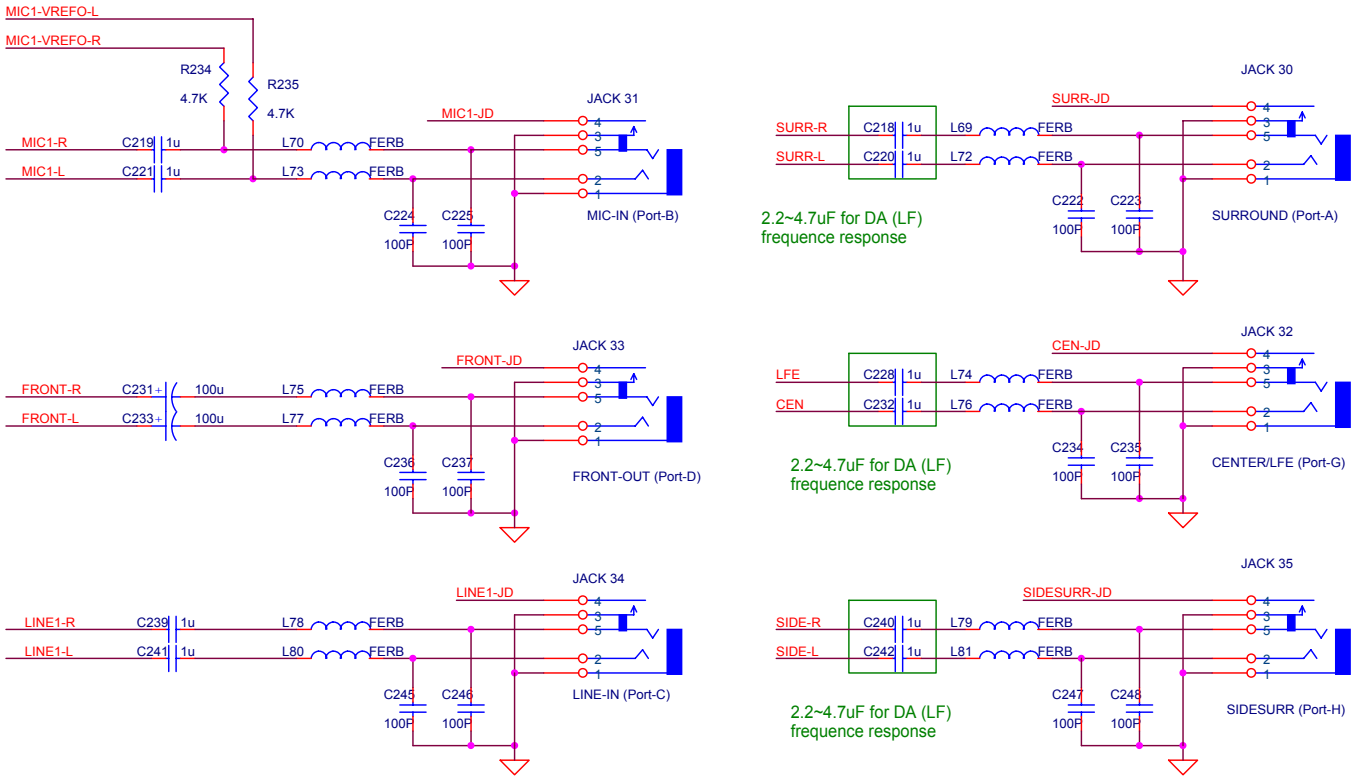


Figure 21. Jack Connection on Rear Panel

10.4. S/PDIF Input/Output Connection

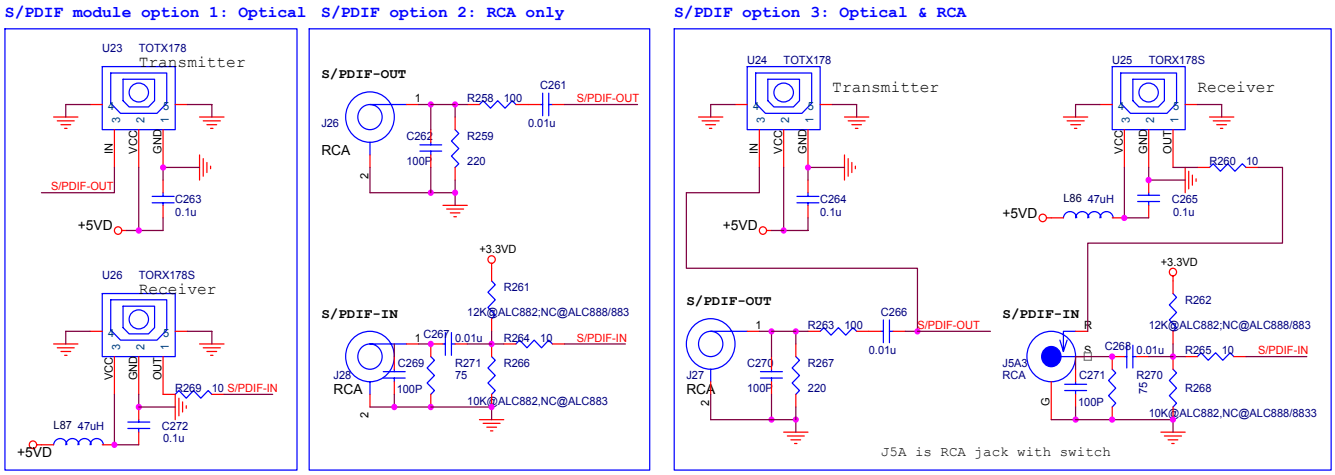


Figure 22. S/PDIF Input/Output Connection

10.5. Secondary S/PDIF-OUT Connected to HDMI Tx Connector

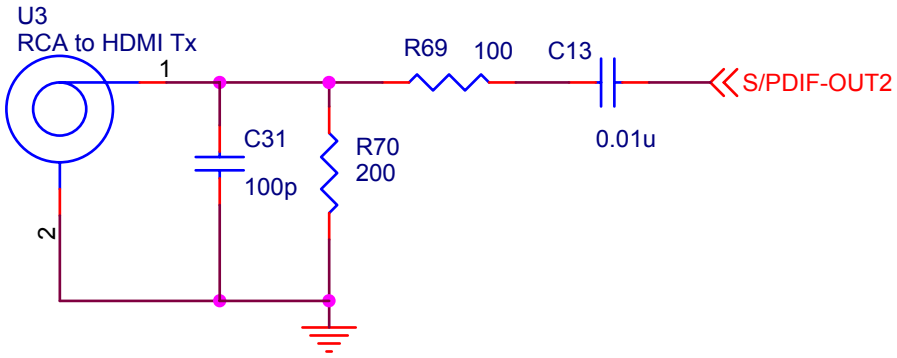


Figure 23. Secondary S/PDIF-OUT Connected to HDMI Tx Connector

10.6. Differential Analog CD Used as Line Level Input

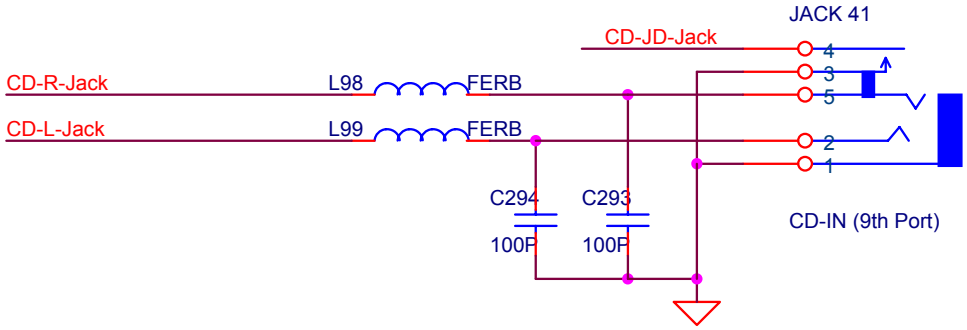
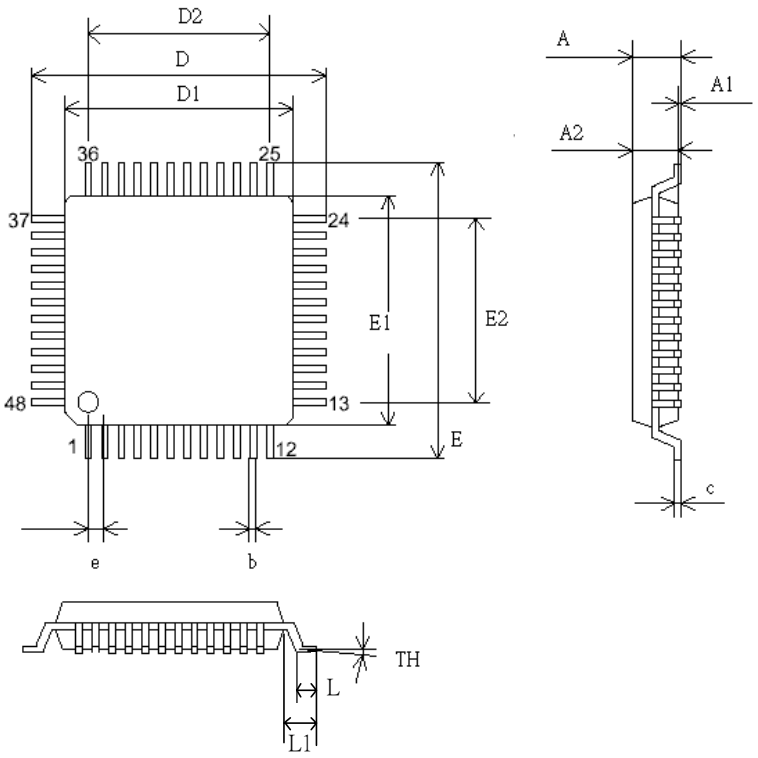


Figure 24. Differential Analog CD Used as Line Level Input

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1	-	1.00	-	-	0.0393	-

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

12. Ordering Information

Table 85. Ordering Information

Part Number	Description	Status
ALC888S-VC-GR	ALC888 Version C, LQFP-48 with 'Green' Package	Sample
ALC888SDD-VC-GR	ALC888S-VC + Dolby® Digital Live + DTS® CONNECT™ (Software Feature)	Sample

Note 1: See page 7 for 'Green' package and version identification.
Note 2: Above parts are tested under AVDD=5.0V. Customers requesting lower AVDD support should contact Realtek sales representatives or agents.

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