Appendix. Options

512KB Memory Expansion

Description

The 512KB memory expansion card provides 512KB of additional memory on the system board. When added to the system board, the card provides a total of 640KB of conventional memory below the 1MB address space and 384KB of extended memory above 1MB address space.

The card contains four 256K x 4 dynamic memory chips organized as 256K x 16 words. Memory speed is 120 nanoseconds. Card size is 2.4 inches x 1.55 inches (61.0 mm x 39.4 mm).

Connector

The card has 40 gold edge tabs, 20 on the front and 20 on the back for connection to the system board memory expansion connector.

Front Pin	Signal Name	Back Pin	Signal Name
1	MD0	40	MA0
2	MD1	39	MA1
3	MD2	38	MA2
4	MD3	37	MA3
5	Ground	36	MA4
6	MD4	35	Ground
7	MD5	34	MA5
8	MD6	33	MA6
9	MD7	32	MA7
10	Ground	31	MA8
11	MD8	30	Reserved
12	MD9	29	Ground
13	MD10	28	-CASL
14	MD11	27	-CASH
15	Ground	26	-WE
16	MD12	25	Reserved
17	MD13	24	-RAS1
18	MD14	23	Reserved
19	MD15	22	Ground
20	Ground	21	+5 V

Figure A-1. 512KB Memory Expansion Signal Names

Signal Name	Definition
-CASH	Column Address Strobe (High Byte)
-CASL	Column Address Strobe (Low Byte)
MA0-MA8	Multiplexed Address Inputs
MD0-MD15	Data In and Data Out
-RAS1	Row Address Strobe
-WE	Write Enable

Audio Card & Joystick

Function Description

The Audio card has several functions:

- Joystick Interface
- 8 Bit Digital-to-Analog Converter (DAC)
- 8 Bit Analog-to-Digital Converter (ADC)
- Sound Generator
- Serial Musical Instrument Digital Interface (MIDI).

All functions share a common interrupt (Level 7). Two Application Specific Integrated Circuits (ASIC) are used to provide some address decoding and interface to several functions.

Joystick

The Joystick interface is compatible with that used in the original IBM PC Game Control Adapter. This adapter allows two joysticks with buttons to be used as a game interface.

The position of each joystick axis is measured by triggering a pulse generator. Four pulse generators are triggered by writing to IO port 201H. After triggering a pulse, software determines the length of the pulse by reading port 201H.

In addition to pulse generators, there are four digital inputs. These are used to read the buttons on the joysticks. When the buttons are pressed, the digital inputs read as 0.

By setting a bit in the control register of the ASICs (Bit 6 of port 202H), the joystick is in the auto trigger mode. This mode automatically re-triggers the pulse generators when all pulse inputs have gone to their inactive (low) state. The value of the pulse width is timed in hardware and yields a value of 0 to 255. The axis of each joystick is simultaneously timed. The axes are latched and read at any time in ports 204H, 205H, 206H, and 207H. This hardware timing of the pulses occurs only in the automatic mode of the joystick. If for any reason the pulse is longer than 255 microseconds, the returned value will be 0FFH (255). The conversion result is latched and read until a new pulse width conversion is completed.

Digital-to-Analog Converter (DAC)

The digital-to-analog converter has a 2K byte, first-in-first-out (FIFO) register. A byte is shifted from the FIFO to the DAC when the FIFO timer reloads. Data is written to the FIFO via port 200H. When the FIFO timer reloads, a byte of data is read from the FIFO and latched onto the Data Out (DO) bus. A flag indicates almost empty status for the FIFO. This flag is programmable from 0 to 1K by writing to port 204H. The 8-bit value is multiplied by 4 and added to the read address of the FIFO controller. If this matches the write address of the FIFO controller, an almost empty flag is set to 1. This flag is only valid when this condition exists. If another read or write occurs, the flag is cleared. This flag generates an internal interrupt or, if enabled, is used to generate an external off-chip interrupt. Two additional flags indicate FIFO full and FIFO empty. If the FIFO is full, any additional attempted writing of data results in lost data. Both full and empty bits may be read via the status register (202H).

Data from the FIFO is sent to an external DAC and generates audio. This output is filtered and AC coupled to other system signals before being sent to the display power amplifier.

Analog-to-Digital Converter (ADC)

The analog-to-digital converter is used to digitize analog voltages. The A/D converter converts a voltage to a digital value provided the input voltage is between ± 380 millivolts and is changing at less than 7.42 millivolts per microsecond (mV/µS). Any input greater than ± 380 millivolts is clipped. Any signal changing faster than 7.42 mV/µS is rate limited to 7.42 mV/µS. The ADC is formed using a DAC, comparator, and up/down counter clocked at 2.5 MHz. This results in a digital low pass filter with a cut-off at 4.88 KHz. Higher frequency signals pass if they are of lower amplitude.

The value of the up/down counter is latched on reload of the FIFO timer. This allows the conversion rate to be set by writing to the FIFO reload register. This latched value is read at port 200H.

FIFO Timer

The FIFO Timer is clocked at 1 MHz and is used to control the rate of data for both audio in and out. The value of the timer is written to port 203H and is read via port 203H. If the timer counts up from 0 and is reset to 0, then the count value is equal to the reload value. A pulse is generated on overflow and is used to latch data into the ADC latch and to read data out of the FIFO. The time between reloads is one cycle longer than the value written to the reload register. A reload value of 0 stops the FIFO timer and holds it in the 0 state. The maximum time is 256 microsecond. The reload register is not affected by a reset. It must be initialized at POR.

Interrupt Generator

An interrupt can be generated to allow interrupt-driven operation of the audio subsystem. This interrupt is disabled after reset.

Joystick interrupts are enabled by setting bit 3 of the control register to 1. When enabled, an interrupt is generated after each conversion of the joysticks. If enabled, the interrupt can be watched via bit 5 of the status register (202H). The interrupt can be reset by setting bit 3 back to 0. This interrupt generates an external interrupt only if the external interrupt enable bit is set (bit 0 of control 202H).

An interrupt from the almost empty flag is available if bit 1 of the control register is set. This interrupt status is read in bit 1 of the status register.

An interrupt is generated at all times from the FIFO overflow bit to indicate ADC data is ready. Its status is available on bit 4 of the status register. Any read of ADC data (200H) will reset this interrupt.

The external interrupt enable bit is used to allow an external interrupt to be generated from any three internal interrupt sources. If the external interrupt is enabled, software must read the status register to determine the cause of the interrupt.

Sound Generator

The sound generator can generate three voices plus noise. This part is write only. Port 205H is used to write to the sound generator.

Serial MIDI

The Musical Instrument Digital Interface (MIDI) is used to transmit and receive MIDI information. The MIDI uses a serial current loop to send and receive binary data. The data stream is 8 bits, no parity, one stop and one start bit. This 10-bit stream is processed at 31.25K baud. This rate results in a bit time of 32 microsecond per bit and 320 microsecond per byte. This interface is hardware compatible with the *MIDI 1.0 Specification.*

Connector Descriptions

Audio Card Connector

The audio card has a single 2-by-17-pin connector for attachment to the system board.

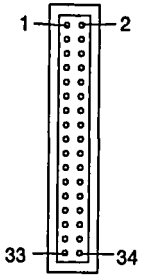


Figure A-2 on page A-9 shows the voltages and signals assigned to the audio card connector.

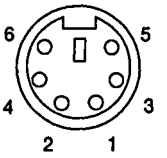
Figure A-2. Audio Card to System Board Voltage and Signal Assignments

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	O	IRQ 7	2	NA	Ground
3	NA	Ground	4	I	CLK
5	I	SA9	6	I	SA7
7	NA	Ground	8	I	SA8
9	I	-IOR	10	I	SA6
11	I	-IOW	12	I	SA5
13	I	SA4	14	I	AEN
15	I	SA3	16	NA	Ground
17	I	SA2	18	I	SA1
19	I	SA0	20	I	+12 Volts
21	I/O	SD0	22	I	-12 Volts
23	I/O	SD2	24	I/O	SD1
25	I/O	SD3	26	I	+5 Volts
27	I/O	SD4	28	O	MODOUT
29	I/O	SD5	30	I	RESET DRV
31	I/O	SD6	32	I/O	SD7
33	O	AUDOUT	34	I	MODIN

Microphone Connector (3/32 Inch [2.5mm] Phone Plug)

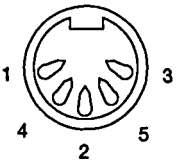
Center contact - Microphone
Outside contact - Ground

MIDI Connector (6 Pin Mini-DIN Plug)



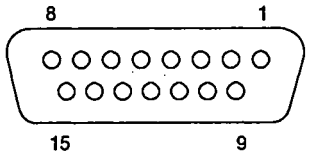
Pin	Signal Name/Function
1	MIDI THRU/OUT +
2	MIDI THRU/OUT –
3	MIDI OUT –
4	MIDI IN +
5	MIDI OUT +
6	MIDI IN –

MIDI IN, OUT, THRU/OUT Connectors (5 Pin DIN Plug)



Pin	Signal Name/Function
1	No Connect
2	Shield
3	No Connect
4	MIDI +
5	MIDI –

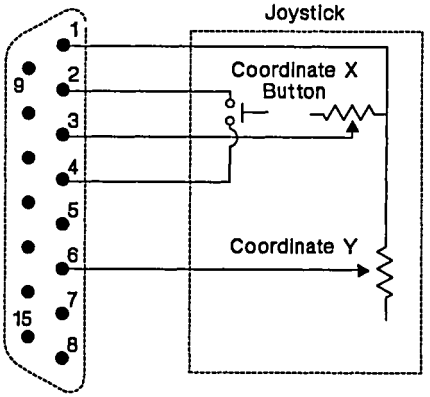
Joystick Connector (15 Pin Female D-Shell)



Pin	Signal Name/Function
1	+ 5 Volts
2	Button 4 (Stick A Button 1)
3	Position 0 (Stick A Coordinate X)
4	Ground
5	Ground
6	Position 1 (Stick A Coordinate Y)
7	Button 5 (Stick A Button 2)
8	+ 5 Volts
9	+ 5 Volts
10	Button 6 (Stick B Button 1)
11	Position 2 (Stick B Coordinate X)
12	Ground
13	Position 3 (Stick B Coordinate Y)
14	Button 7 (Stick B Button 2)
15	+ 5 Volts

Joystick Schematic Diagram

15-PIN MALE D-SHELL CONNECTOR



Note: Potentiometer for Coordinates X and Y has a range of 0 to 145 k-ohms. Button is normally open; closed when pressed.

I/O Address Assignments

I/O Address (hex)	Read Function
200	Read Analog to Digital Converter Data
201	Read Joystick and buttons
202	Read Control Register
203	Read FIFO Timer reload value
204	Joystick (X Axis Stick A) P0
205	Joystick (Y Axis Stick A) P1
206	Joystick (X Axis Stick B) P2
207	Joystick (Y Axis Stick B) P3
330	Read to MIDI TXD Register
331	Read to MIDI IER Register
332	Read to MIDI IIR Register
335	Read to MIDI LSR Register
	Write Function
200	Write to Digital to Analog Converter
201	Starts Joystick conversions
202	Write to Control Register
203	Write FIFO Timer reload value
204	Write almost empty value
205	Write to Sound Generator
330	Write to MIDI TXD Register
331	Write to MIDI IER Register
332	Write to MIDI IIR Register
335	Write to MIDI LSR Register

Software Registers

I/O Address 200H

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Read	Write
D7 – 7 MSB	ADC Input	DAC Output
D6 – 6	ADC Input	DAC Output
D5 – 5	ADC Input	DAC Output
D4 – 4	ADC Input	DAC Output
D3 – 3	ADC Input	DAC Output
D2 – 2	ADC Input	DAC Output
D1 – 1	ADC Input	DAC Output
D0 – 0 LSB	ADC Input	DAC Output

A read of port 200H reads the data latch for the input ADC. This data was latched on the previous overflow of the FIFO timer. This read also clears the ADC Data Ready bit.

A write to port 200H writes data to the FIFO for the output DAC. If the FIFO is full, this data is lost. If the FIFO is empty, the data is output to the DAC on the next overflow of the FIFO timer.

I/O Address 201H

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Read	Write
D7 – 7 MSB	Button 7 (B2)	See Note
D6 – 6	Button 6 (B1)	See Note
D5 – 5	Button 5 (A2)	See Note
D4 – 4	Button 4 (A1)	See Note
D3 – 3	Stick 3 (BY)	See Note
D2 – 2	Stick 2 (BX)	See Note
D1 – 1	Stick 1 (AY)	See Note
D0 – 0 LSB	Stick 0 (AX)	See Note

Note: A write to port 201 causes all stick inputs to go high for a value specified by the equation TIME = 24.2 microsecond + 0.011(r) microsecond. (Manual mode only.) Button inputs are not affected.

Port 201 emulates the existing IBM PC Game Control Adapter. A write to this port causes the pulse generators to be triggered.

Button pins are TTL level non-inverting inputs.

When in the auto joystick mode, the pulse generators are continuously triggered.

I/O Address 202H

MSB LSB

RIO	JM	JIE	ADR	FF	FE	IR	AIE

Bit	Read	Write
RIO – 7 MSB	RIN1 Bit	ROUT Bit
JM – 6	RIN0 Bit	0 – Manual Joystick 1 – Auto Mode
JIE – 5	Joystick Int	0 – Joystick Int Disabled 1 – Enabled
ADR – 4	ADC Data Rdy	Reserved
FF – 3	FIFO Full	Reserved
FE – 2	FIFO Empty	0 – Modem Audio Disabled 1 – Enabled
IR – 1	Almost Empty Int	0 – AE Int Disabled 1 – Enabled
AIE – 0 LSB	Ext Int Enable	0 – Ext Int Disabled 1 – Enabled

Note: Default value for this port is 00H after a RESET.

Bit 7, the RIN0, RIN1, and ROUT bits, are reserved.

Bit 6 is used to select the manual or auto trigger mode. A read will read the value of the RIN0 Bit.

Bit 5 is used to enable interrupts from the joystick.

Bit 4 is read only and is used to indicate that ADC data has been latched due to FIFO timer overflow. A read of the data from port 200H resets this bit.

Bit 3 is read only and is used to indicate that the FIFO is full. Any additional write to port 200H results in lost data.

Bit 2 is used to indicate that the FIFO is empty. A write to this bit controls the modem audio enable bit.

Bit 1 is used to allow interrupts from the almost empty flag. The interrupt flag is cleared by writing a 0 then a 1 to this bit.

Bit 0 is the External interrupt control bit. A 1 enables interrupt generation from any of the three internal interrupt sources.

I/O Address 203H

MSB LSB

T7	T6	T5	T4	T3	T2	T1	T0

Bit	Read	Write
T7 – 7 MSB	FIFO Timer	Timer Reload Value
T6 – 6	FIFO Timer	Timer Reload Value
T5 – 5	FIFO Timer	Timer Reload Value
T4 – 4	FIFO Timer	Timer Reload Value
T3 – 3	FIFO Timer	Timer Reload Value
T2 – 2	FIFO Timer	Timer Reload Value
T1 – 1	FIFO Timer	Timer Reload Value
T0 – 0 LSB	FIFO Timer	Timer Reload Value

Note: Timer clocked at a 1-microsecond rate.

This port controls the timer reload value for the FIFO timer. This timer is used for both ADC and DAC timing.

I/O Address 204H

MSB LSB

P7	P6	P5	P4	P3	P2	P1	P0

Bit	Read	Write
P7 – 7 MSB	Stick 0 Position	Almost empty Bit 9
P6 – 6	Stick 0 Position	Almost empty Bit 8
P5 – 5	Stick 0 Position	Almost empty Bit 7
P4 – 4	Stick 0 Position	Almost empty Bit 6
P3 – 3	Stick 0 Position	Almost empty Bit 5
P2 – 2	Stick 0 Position	Almost empty Bit 4
P1 – 1	Stick 0 Position	Almost empty Bit 3
P0 – 0 LSB	Stick 0 Position	Almost empty Bit 2

This port is used to read the X position of Stick A. A write to this port controls the value of the almost empty register. A value of 0 generates an almost empty when there are 0 bytes left, a 1 generates an almost empty when 4 bytes are left, and so on.

I/O Address 205H (Write)

MSB LSB

0	0	F9	F8	F7	F6	F5	F4

This is the form for the second byte of all voice generators. After sending the byte to select the register and low 4 bits of the voice, the second byte is sent to adjust the high 6 bits of the 10 voice register.

MSB LSB

1	0	0	0	F3	F2	F1	F0

This is the first byte of data to select Voice Register 1 of the Sound Generator. This selects Voice 1 and sets the low 4 bits of the Voice 1 frequency. The frequency is determined by 125 KHz/F, where F is 0 to 1023.

MSB LSB

1	0	0	1	A3	A2	A1	A0

```
A3  A2  A1  A0

 0   0   0   1 -  2 dB Attenuation
 0   0   1   0 -  4 dB Attenuation
 0   1   0   0 -  8 dB Attenuation
 1   0   0   0 - 16 dB Attenuation
 1   1   1   1 - OFF - No Output
```

This controls the attenuation of Voice 1.

MSB LSB

1	0	1	0	F3	F2	F1	F0

This is the first byte of data to select Voice Register 2 of the Sound Generator. This selects Voice 2 and sets the low 4 bits of the Voice 2 frequency. The frequency is determined by 125 KHz/F, where F is 0 to 1023. The second byte determines the other 6 bits of the voice register.

MSB LSB

1	0	1	1	A3	A2	A1	A0

A3 A2 A1 A0

0 0 0 1 - 2 dB Attenuation
0 0 1 0 - 4 dB Attenuation
0 1 0 0 - 8 dB Attenuation
1 0 0 0 - 16 dB Attenuation
1 1 1 1 - OFF - No Output

This controls the attenuation of Voice 2.

MSB LSB

1	1	0	0	F3	F2	F1	F0

This is the first byte of data to select Voice Register 3 of the Sound Generator. This selects Voice 3 and sets the low 4 bits of the Voice 3 frequency. The frequency is determined by 125 KHz/F, where F is 0 to 1023. The second byte determines the other 6 bits of the voice register.

MSB LSB

1	1	0	1	A3	A2	A1	A0

A3 A2 A1 A0

0 0 0 1 - 2 dB Attenuation
0 0 1 0 - 4 dB Attenuation
0 1 0 0 - 8 dB Attenuation
1 0 0 0 - 16 dB Attenuation
1 1 1 1 - OFF - No Output

This controls the attenuation of Voice 3.

MSB LSB

1	1	1	0	0	FB	N0	N1

FB Noise Type

0 - Periodic Noise
1 - White Noise

N0	N1	Shift Rate
0	0	N/1024
0	1	N/2048
1	0	N/4096
1	1	Voice Generator 3 Output

This selects the shift rate and feedback for the Noise Generator.

MSB LSB

1	1	1	1	A3	A2	A1	A0

A3	A2	A1	A0	
0	0	0	1	- 2 dB Attenuation
0	0	1	0	- 4 dB Attenuation
0	1	0	0	- 8 dB Attenuation
1	0	0	0	- 16 dB Attenuation
1	1	1	1	- OFF - No Output

This controls the attenuation of the Noise Generator.

I/O Address 205H (Read)

MSB LSB

P7	P6	P5	P4	P3	P2	P1	P0

Bit	Read
P7 – 7 MSB	Stick 1 Position
P6 – 6	Stick 1 Position
P5 – 5	Stick 1 Position
P4 – 4	Stick 1 Position
P3 – 3	Stick 1 Position
P2 – 2	Stick 1 Position
P1 – 1	Stick 1 Position
P0 – 0 LSB	Stick 1 Position

This port is used to read the Y position of Stick A.

I/O Address 206H

MSB LSB

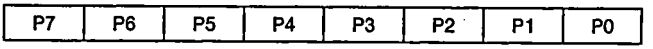
P7	P6	P5	P4	P3	P2	P1	P0

Bit	Read	Write
P7 – 7 MSB	Stick 2 Position	Reserved
P6 – 6	Stick 2 Position	Reserved
P5 – 5	Stick 2 Position	Reserved
P4 – 4	Stick 2 Position	Reserved
P3 – 3	Stick 2 Position	Reserved
P2 – 2	Stick 2 Position	Reserved
P1 – 1	Stick 2 Position	Reserved
P0 – 0 LSB	Stick 2 Position	Reserved

This port is used to read the X position of Stick B.

I/O Address 207H

MSB LSB

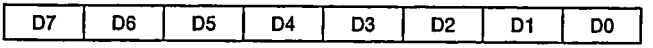


Bit	Read	Write
P7 – 7 MSB	Stick 3 Position	Reserved
P6 – 6	Stick 3 Position	Reserved
P5 – 5	Stick 3 Position	Reserved
P4 – 4	Stick 3 Position	Reserved
P3 – 3	Stick 3 Position	Reserved
P2 – 2	Stick 3 Position	Reserved
P1 – 1	Stick 3 Position	Reserved
P0 – 0 LSB	Stick 3 Position	Reserved

This port is used to read the Y position of Stick B.

I/O Address 330H

MSB LSB



Bit	Read	Write
D7 – 7 MSB	Rx Data Bit 7	Tx Data Bit 7
D6 – 6	Rx Data Bit 6	Tx Data Bit 6
D5 – 5	Rx Data Bit 5	Tx Data Bit 5
D4 – 4	Rx Data Bit 4	Tx Data Bit 4
D3 – 3	Rx Data Bit 3	Tx Data Bit 3
D2 – 2	Rx Data Bit 2	Tx Data Bit 2
D1 – 1	Rx Data Bit 1	Tx Data Bit 1
D0 – 0 LSB	Rx Data Bit 0	Tx Data Bit 0

This port is used to read and write MIDI data.

I/O Address 331H

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Read/Write
D7 – 7 MSB	Reserved
D6 – 6	Reserved
D5 – 5	Reserved
D4 – 4	0 – MIDI Out 1 – MIDI Thru
D3 – 3	Reserved
D2 – 2	Reserved
D1 – 1	Tx Data Interrupt
D0 – 0 LSB	Rx Data Interrupt

This port is used to control the interrupt enables for the MIDI. Interrupts will be routed to IRQ 7.

I/O Address 332H

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Read Only
D7 – 7 MSB	Reserved
D6 – 6	Reserved
D5 – 5	Reserved
D4 – 4	Reserved
D3 – 3	Reserved
D2 – 2	Reserved
D1 – 1	Reserved
D0 – 0 LSB	Interrupt Pending

This port is used to determine interrupt status.

I/O Address 335H

MSB LSB

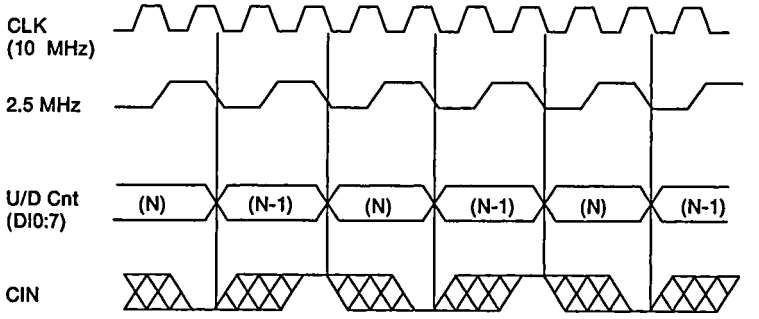
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Read Only
D7 – 7 MSB	Reserved
D6 – 6	Reserved
D5 – 5	TxD Empty
D4 – 4	Reserved
D3 – 3	Framing Error
D2 – 2	Reserved
D1 – 1	Overrun Error
D0 – 0 LSB	Rx Data Available

This port is used to determine the condition of the transmit and receive data buffers.

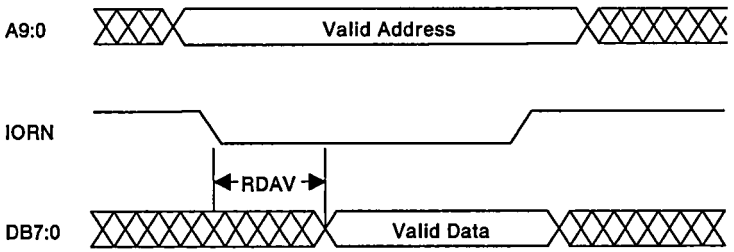
Signal Timings

Input ADC Timing (Steady State)



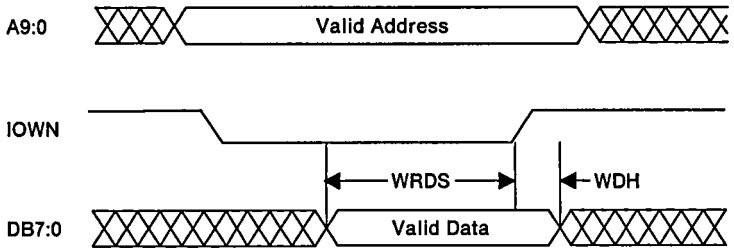
Note: CIN sampled prior to the up/down counter changes.

Bus Read Timing



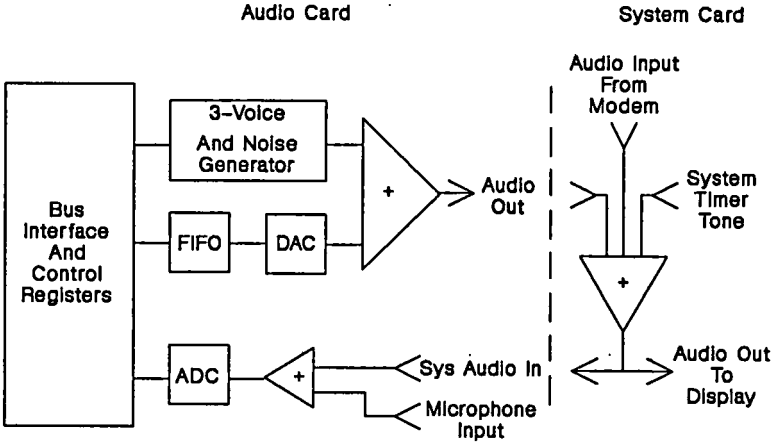
Timing		Min	Max (ns)
RDAV	RD active to valid read data		80

Bus Write Timing

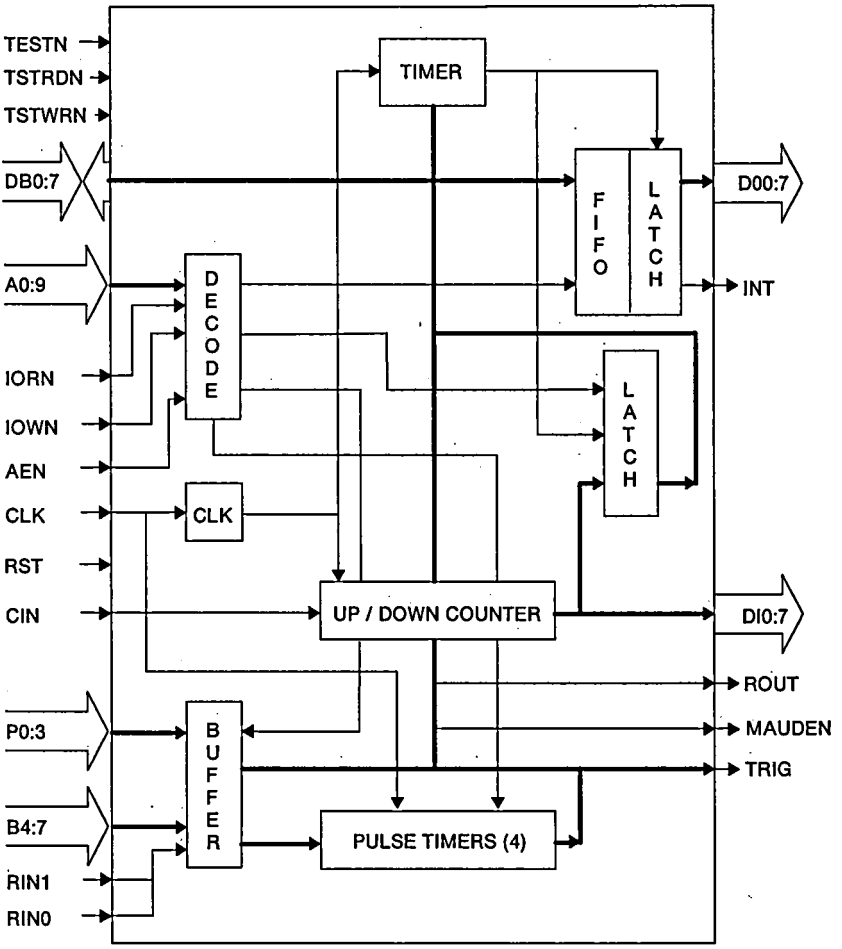


Timing		Min (ns)	Max (ns)
WRDS	Data setup prior to WR active	100	
WDH	Data hold after Write		15

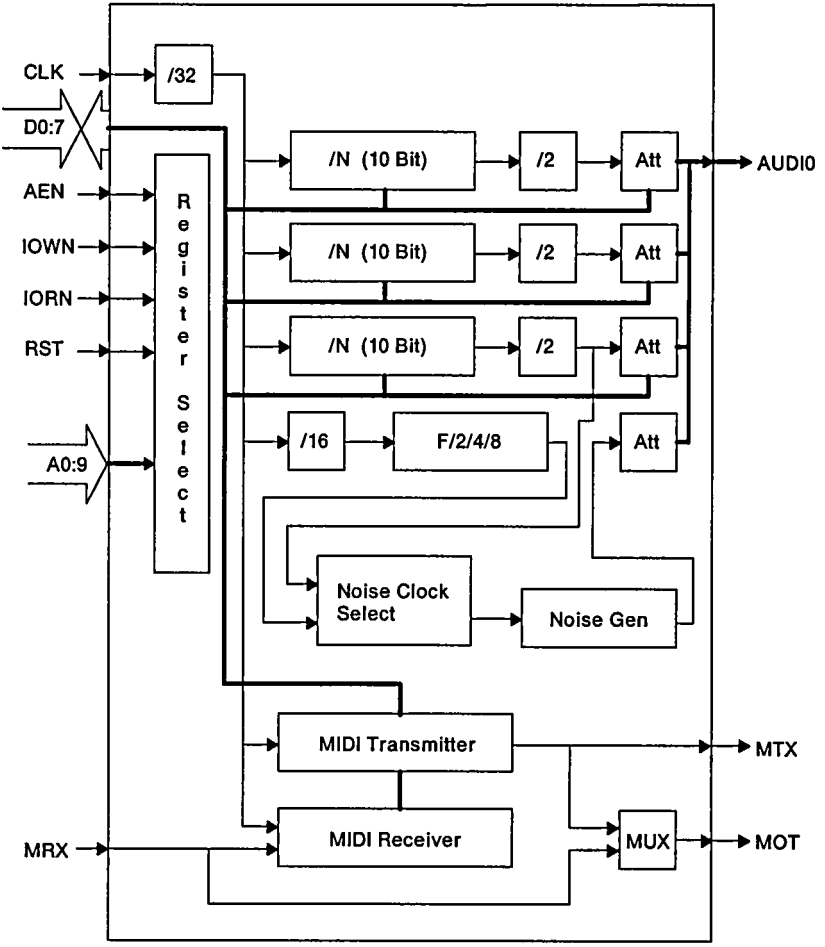
Audio Subsystem



Audio Module Block Diagram



Sound Generator Module Block Diagram



5.25-Inch External Diskette Drive Unit

The 5.25-inch External Diskette Drive Unit attaches to the bottom of the IBM PS/1 computer system unit. The 5.25-inch external diskette drive unit contains a logic card, a 5.25-inch diskette drive and the necessary cables to electrically connect the unit to the system unit.

The logic card buffers the interface signals coming from and going to the system unit. The buffer card has a flat cable attached which connects to either a 360KB Double Sided Diskette Drive or a 1.2MB High Capacity Diskette Drive, depending on the option purchased.

A thirty-four conductor flat ribbon cable connects the buffer card to the system unit. A separate four conductor cable provides the 5.25-inch external diskette drive with +5 and +12 volt power from the system unit.

Once installed, the 5.25-inch external diskette drive becomes the system drive B, which is non-bootable.

Buffer Card Functional Diagram

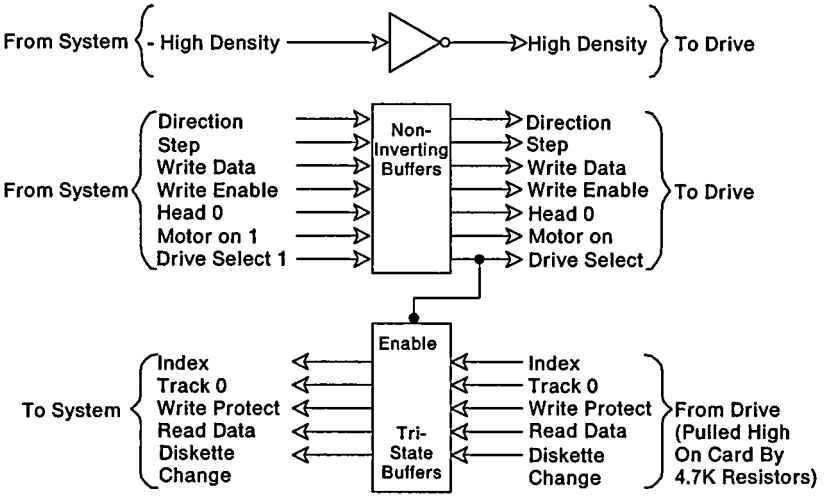


Figure A-3. Buffer Card Functional Diagram

Description

The buffer card provides high-current open-collector buffers for signals passing from the system unit to the diskette drive, inverting the high density select signal. The card also provides pull-up resistors and tri-state buffers for signals received from the drive.

A 2-by-17 pin header (J1) connects the buffer card to the system unit. A 2-by-17 card-edge connector (J2) attaches to the diskette drive.

Note: High density select has no effect when a 360KB diskette drive is present. Also, with a 360KB diskette drive, -diskette change is always high (inactive).

Specifications

The following are specifications for the 5.25-inch external diskette drive unit:

Size

- Width: 274 millimeters (10.8 inches)
- Depth: 320 millimeters (12.6 inches)
- Height: 64 millimeters (2.5 inches).

Weight

- 3.4 kilograms (7.5 pounds).

Buffer Card Connector Pin-Outs

J1			
Pin	**Signal**	**Pin**	**Signal**
1	Drive 2 installed (Gnd)	2	-High Density Select
3	+5 V	4	Reserved (N/C)
5	Ground	6	Reserved (N/C)
7	Ground	8	-Index
9	Reserved (N/C)	10	-Motor on 1
11	Ground	12	-Drive Select 0
13	Ground	14	-Drive Select 1
15	Ground	16	-Motor on 0
17	Ground	18	-Direction
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Ground	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	Head 0
33	Ground	34	-Diskette Change

J2			
Pin	**Signal**	**Pin**	**Signal**
1	Ground	2	-High Density Select
3	Ground	4	Reserved (N/C)
5	Ground	6	Reserved (N/C)
7	Ground	8	-Index
9	Ground	10	Reserved (N/C)
11	Ground	12	-Drive Select
13	Ground	14	Reserved (N/C)
15	Ground	16	-Motor on
17	Ground	18	-Direction
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Ground	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	Head 0
33	Ground	34	-Diskette Change

5.25-Inch Double-Sided Diskette Drive

Description

The IBM PS/1 computer 5.25-inch Double-Sided Diskette Drive is a direct-access device that can store 360KB of data on a dual-sided 5.25-inch diskette. All data format and access control is in the system. The following figure describes the type of diskette required by this drive.

Figure A-4. Diskette Requirements

Characteristic	Requirement
Certification	Double-sided 48 TPI (tracks per inch) 40 tracks per surface Soft Sector
Recording Density	5,876 bits per inch
Media Coercivity	300 to 350 Oersteds
Jacket	Standard 5.25-inch

Interfaces

The diskette drive has two types of interfaces: control and dc power. The following figure shows the signals and pin assignments for the control interfaces.

Figure A-5. Control Interface (P1/J1)

Signal	I/O	Signal Pin	Ground Pin
Reserved	-	2	1
Reserved	-	4	3
-Drive Select 3	I	6	5
-Index	O	8	7
-Drive Select 0	I	10	9
-Drive Select 1	I	12	11
-Drive Select 2	I	14	13
-Motor On	I	16	15
-Direction Select	I	18	17
-Step	I	20	19
-Write Data	I	22	21
-Write Gate	I	24	23
-Track 00	O	26	25
-Write Protect	O	28	27
-Read Data	O	30	29
-Side 1 Select	I	32	31
Reserved	-	34	33

All signals operate between +5 V dc and ground with the following definitions:

	Outputs	Inputs
Inactive Level:	+2.5 to +5.25 V dc	+2.5 to +5.25 V dc
Active Level:	0.0 to +0.4 V dc	0.0 to +0.8 V dc

All outputs from the drive can sink 40 mA at the active level. The system provides pull-up registers.

Following are the signals and pin assignments for the dc power interface.

Figure A-6. DC Power Interface (P2/J2)

Signal	Pin
+ 12 V dc	1
+ 12 V dc Return	2
+ 5 V dc Return	3
+ 5 V dc	4

Specifications

The following are physical specifications for the 5.25-inch double-sided diskette drive.

Size

- Width: 146 millimeters (5.8 inches)
- Depth: 203.2 millimeters (8.0 inches)
- Height: 41 millimeters (1.6 inches).

Weight

- 1.6 kilograms (3.52 pounds).

Electrical

- 11 Watts (typical).

The following are performance specifications for the 5.25-inch double-sided diskette drive:

Capacity unformatted	500KB
Capacity formatted	
9 sectors per track	360KB
Recording density	5,876 bits per inch
Track density	48 TPI (tracks per inch)
Cylinders	40
Heads	2
Encoding method	MFM
Rotational speed	300 RPM ±1.5%
Transfer rate	250K bits per second
Latency (average)	100 milliseconds
Access time:	
Average	81 milliseconds
Track to track	6 milliseconds
Settling time	15 milliseconds
Head load time	0 milliseconds
Motor start time	500 milliseconds

5.25-Inch High Capacity Diskette Drive

Description

The IBM PS/1 computer 5.25-inch High Capacity Diskette Drive is a direct-access device that can store 1.2MB of data on a dual-sided 5.25-inch diskette. All data format and access control is in the system. The following figure describes the type of high-density diskette required by this drive. Diskettes which meet these specifications may not be used in either a 160/180KB or a 320/360KB diskette drive.

Figure A-7. Diskette Requirements

Characteristic	Requirement
Certification	Double sided
	96 TPI (tracks per inch)
	80 tracks per surface
	Soft Sector
Recording Density	9,646 bits per inch
Media Coercivity	600 to 650 Oersteds
Jacket	Standard 5.25-inch

Note: This drive also can read diskettes formatted for a 320/360KB dual-sided drive or a 160/180KB single-sided drive.

Interfaces

The diskette drive has two types of interface: control and dc power. The following figure shows the signals and pin assignments for the control interfaces.

Figure A-8. Control Interface (P1/J1)

Signal Name	I/O	Signal Pin	Ground Pin
-Reduced Write	I	2	1
Reserved	-	4	3
-Drive Select 3	I	6	5
-Index	O	8	7
-Drive Select 0	I	10	9
-Drive Select 1	I	12	11
-Drive Select 2	I	14	13
-Motor On	I	16	15
-Direction Select	I	18	17
-Step	I	20	19
-Write Data	I	22	21
-Write Gate	I	24	23
-Track 00	O	26	25
-Write Protect	O	28	27
-Read Data	O	30	29
-Side 1 Select	I	32	31
-Diskette Change	O	34	33

All signals operate between +5 V dc and ground with the following definitions:

	Outputs	Inputs
Inactive Level:	+2.5 to +5.25 V dc	+2.5 to +5.25 V dc
Active Level:	0.0 to +0.4 V dc	0.0 to +0.8 V dc

All outputs from the drive can sink 40 mA at the active level. The system provides pull-up registers.

Following are the signals and pin assignments for the dc power interface.

Figure A-9. DC Power Interface (P2/J2)

Signal	Pin
+ 12 V dc	1
+ 12 V dc Return	2
+ 5 V dc Return	3
+ 5 V dc	4

Specifications

The following are physical specifications for the 5.25-inch high capacity diskette drive.

Size

- Width: 146 millimeters (5.8 inches)
- Depth: 203.2 millimeters (8.0 inches)
- Height: 41 millimeters (1.6 inches).

Weight

- 1.6 kilograms (3.52 pounds).

Electrical

- 11 Watts (typical).

The following are performance specifications for the 5.25-inch high capacity diskette drive:

Capacity unformatted	1604KB
Capacity formatted	
15 sectors per track	1.2MB
Recording density	9,646 bits per inch
Track density	96 TPI (tracks per inch)
Cylinders	80
Heads	2
Encoding method	MFM
Rotational speed	360 RPM
Transfer rate	500K bits per second
Latency (average)	83 milliseconds
Access time:	
Average	91 milliseconds
Track to track	3 milliseconds
Settling time	18 milliseconds
Head load time	50 milliseconds
Motor start time (including head load time)	750 milliseconds

Adapter Card Unit

Description

The Adapter Card Unit attaches to the top of the system unit, allowing the attachment of up to three adapter cards to the system. Two cards up to 280 mm (11 inches) long and one card up to 241 mm (9.5 inches) long can be installed. The adapter card unit consists of an expansion card, a power card, a brushless 12V dc fan, and a metal cover set.

The expansion card attaches to the adapter card unit connector on the system board. The card carries system bus signals between the system unit and the three 2 by 49 adapter card connectors. Also, the fan and the power card connect to the expansion card. The I/O Connector assignments are shown in Figure A-10.

The power card receives 30 – 40V bulk dc (36V nominal) from the system unit (via the expansion card) and generates + 5V dc at 6A maximum. The card uses ac/dc switching technology operating at a frequency of approximately 1 MHz. The card also receives –12V and generates –5V at 70 mA maximum using a linear regulator. See Section 4, "Power Supply" for details.

Power Supply

Four voltage levels are provided for adapter cards. The total current available for each voltage in the adapter card unit is as follows:

- + 5V dc (+ 5%, – 3%) at 4.2 A
- – 5V dc (+ 10%, – 10%) at 0.60 A
- + 12V dc (+ 5%, – 3%) at 0.66 A
- – 12V dc (+ 10%, – 10%) at 0.27 A.

The total power used by the cards must be less than 30 watts.

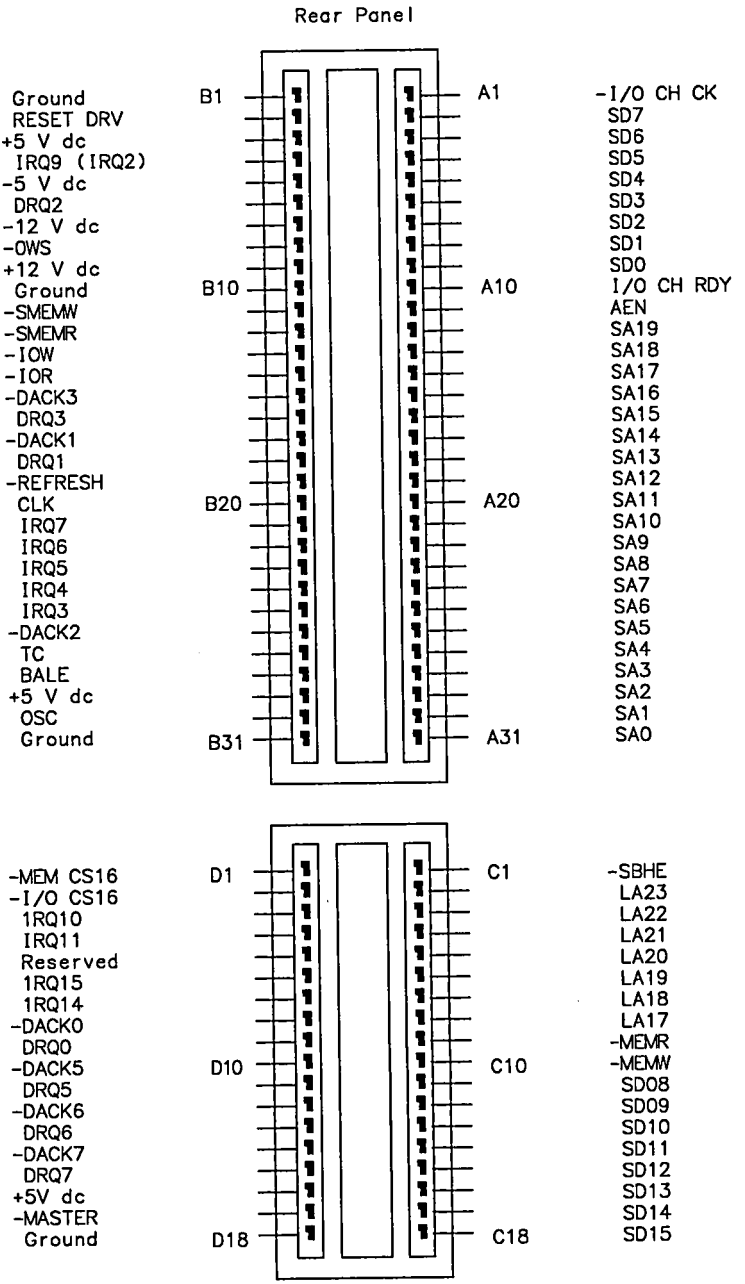


Figure A-10. I/O Channel Connectors.

Specifications

The following are specifications for the Adapter Card Unit:

Size

- Width: 274 millimeters (10.8 inches)
- Depth: 320 millimeters (12.6 inches)
- Height: 69 millimeters (2.7 inches).

Weight

- 2.3 kilograms (5 pounds).