
Section 8. Drives

3.5-Inch 30MB Fixed Disk Drive and Controller	8-3
Description	8-3
Fixed Disk Controller	8-4
Programming	8-5
Registers	8-6
Data Register, Hex 320	8-6
Attachment Status Register, Hex 322	8-6
Attachment Control Register, Hex 322	8-7
Interrupt Status Register, Hex 324	8-8
Attention Register, Hex 324	8-9
Control Blocks	8-10
Command Control Block	8-10
Command Specify Block	8-12
Sense Summary Block	8-13
Status Bytes	8-14
Format Control Block	8-17
Commands	8-19
Connector	8-24
Signal Description	8-25
Specifications	8-26
3.5-Inch 1.44MB Diskette Drive	8-27
Description	8-27
Programming Considerations	8-28
Signal Levels	8-28
Connector	8-28
Specifications	8-29

(

(

(

3.5-Inch 30MB Fixed Disk Drive and Controller

Description

This section describes the 30MB fixed disk drive for the IBM PS/1 computer. The drive is attached to a dedicated I/O channel connector on the system board through a single flat cable. This channel supplies all the necessary power and control signals.

The drive and controller is buffered on the I/O bus and use the system's direct memory access (DMA) for fixed-disk-drive data transfers. When enabled, an interrupt request to the system occurs on the interrupt line, IRQ14. The interrupt controller then causes an interrupt hex 76.

The drive and controller provide automatic 48-bit error checking and correction (ECC).

The device-level control for the fixed disk is in the system BIOS.

The last cylinder on the fixed disk drive is reserved for diagnostic use. The diagnostic write test destroys any data on this cylinder.

Important: IBM provides a BIOS interface to insulate the programmer from hardware dependences. IBM recommends that all applications use the BIOS interface, or the operating system interface, to prevent incompatibilities caused by differences in hardware.

Fixed Disk Controller

The disk controller has five registers that may be accessed by the system microprocessor: two status registers, a data register, and two control registers.

The two status registers contain the status information of the disk controller and can be accessed at any time. These registers are read-only and indicate the status of data transfers between the microprocessor and disk controller.

The data register (consisting of several registers in a stack with only one register presented to the data bus) stores data, commands, and parameters and provides the disk controller's sense information. Data bytes are read from, or written to the data register in order to program or obtain the results after a particular command.

The two control registers initiate the transfer of commands, data, and sense information through the data registers and enable DMA and interrupt requests. The controller-select signal (-DISK CS) is generated by writing to port hex 32x.

The following is a block diagram of the disk drive and controller.

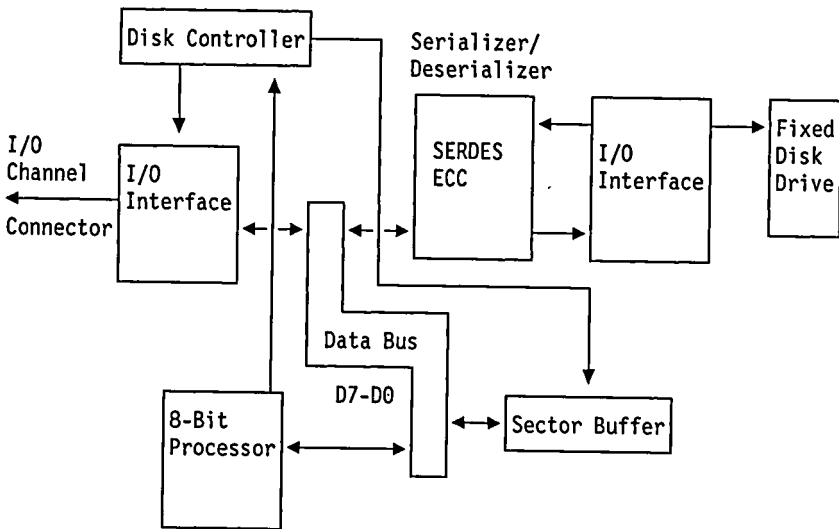


Figure 8-1. Fixed Disk and Controller

Programming

Before enabling the DMA controller or the interrupt controller, the request enable bits in the Attachment Control register should be set to enable the requests. This prevents erroneous DMA transfers or interrupts.

Because the system has a dedicated I/O channel for the fixed disk, the I/O address decoding is done on the system board. The system activates the disk address signal (-DISK CS) using the 16 most-significant address bits; the 3 least-significant address bits select the various registers.

Because the drive and controller logic are integrated and the controller is dedicated to the one drive type, the controller has no switch settings or drive select requirements.

The drive and controller operate using a control block architecture that minimizes system interaction. Control blocks can be transferred to the drive by the microprocessor or DMA controller. These transfers and data transfers are initiated through the Attention register. Completion of the operation is signaled through the two status registers and the system interrupt.

The following figure is a table of the I/O ports and their function.

R/W	Port Address	Function
Read	320	Read data from drive
Write	320	Write data to drive
Read	322	Read Attachment Status register
Write	322	Write Attachment Control register
Read	324	Read Interrupt Status register
Write	324	Write Attention register

Registers

Data Register, Hex 320

The data register is read/write and transfers data between the controller and the system. This register consists of two register stacks. A sector of data is transferred into the first stack. While that data is transferred out of the first stack, the second stack receives the second sector of data.

Attachment Status Register, Hex 322

This register is read-only and contains status information on the present state of the controller. The following are bit descriptions.

Figure 8-3. Attachment Status Register

Bit	Function
7 - 5	Reserved
4	Data Request
3	Direction
2	Busy
1	Interrupt Request
0	Transfer Enable

Bit 7 - 5 Reserved.

Bit 4 Data Request: This bit is set by the controller to request a data transfer. This bit does not cause an interrupt, so it must be polled by the microprocessor before an I/O Read or Write to the data register.

Bit 3 Direction: This bit indicates the direction of the data transfer associated with bit 4. When set, the direction is from the controller.

Bit 2 Busy: When set to 1, this bit indicates that the controller is processing a command through the Attention register.

- Bit 1** **Interrupt Request:** This bit is set to indicate that a command has been completed and the content of the Interrupt Status register is valid. If the interrupt is enabled, this bit causes an interrupt. This bit is cleared when the register is read.
- Bit 0** **Transfer Enable:** When set, this bit indicates that data is being transferred.

Attachment Control Register, Hex 322

The Attachment Control register controls the fixed-disk interrupt and DMA channel, and resets the drive. The write address is hex 322.

<i>Figure 8-4. Attachment Control Register</i>	
Bit	Function
7	Reset
6 - 2	Reserved = 0
1	Interrupt Enable
0	DMA Enable

Bit 7 **Reset:** When set to 1, this bit causes a hardware reset. The sequence of the reset is:

1. Write this register with this bit set.
2. Write this register with all bits clear.
3. Write this register with bits set as desired.

Bits 6 - 2 Must be written as 0.

- Bit 1** **Interrupt Enable:** When set to 1, this bit enables the interrupt signal to the system.
- Bit 0** **DMA Enable:** When set, this bit enables DMA requests to the system. When clear, the microprocessor performs the transfers.

Interrupt Status Register, Hex 324

At the end of all commands from the microprocessor, the disk controller returns completion status information to this register. This byte informs the system if an error occurred during the execution of the command. The following shows the format of this byte.

Figure 8-5. Interrupt Status Register

Bit	Function
7	Termination Error
6	Invalid Command
5	Command Reject
4 - 2	Reserved
1	ERP Invoked
0	Equipment Check

- Bit 7** Termination Error: When set, this bit indicates a severe error has occurred. The specific error is indicated by other bits in this register or in the Sense Summary Block described later in this section.
- Bit 6** Invalid Command: When set, this bit indicates that the Command Control Block, Command Specify Block, or the Attention register contains an invalid command or parameter.
- Bit 5** Command Reject: When set, this bit indicates the controller cannot execute the command. This bit is also set if a transaction other than a request for a Sense Summary Block is initiated before a required reset.
- Bits 4 - 2** Reserved.
- Bit 1** ERP Invoked: When set, this bit shows an error has occurred during command execution and error recovery procedures (ERP) have been done. If the procedures were not successful, the termination error bit is set. This bit is used to track soft errors.
- Bit 0** Equipment Check: When set, this bit indicates an internal hardware error has occurred. This error is cleared by resetting the drive.

Attention Register, Hex 324

The system uses this register to initiate all transactions with the drive. The write address is hex 324. The bits are set according to the type of transaction and are defined as follows:

Figure 8-6. Attention Register

Bit	Function
7	CCB Request
6	CSB Request
5	SSB Request
4	Data Request
3 - 0	Reserved = 0

- Bit 7** **Command Control Block:** When set, this bit signals the drive that a Command Control Block is pending transfer. The drive then requests the control block through the data request bit of the Attachment Status register.
- Bit 6** **Command Specify Block:** When set, this bit signals the drive that a command specify block is pending transfer. The drive then requests the specify block.
- Bit 5** **Sense Summary Block:** When set, this bit signals a request for a Sense Summary Block. The drive then sends the summary block.
- Bit 4** **Data Request:** When set, this bit indicates that the system is ready to start a data transfer.
- Bits 3 - 0** Must be written as 0.

Control Blocks

Command Control Block

The system specifies the operation by sending the 6-byte command control block to the controller. It can be sent through a DMA or I/O operation. The figure below shows the format of the command control block (CCB) and defines the bytes that make up the CCB.

	7	6	5	4	3	2	1	0
Byte 0	Command Code			ND	AS	0	EC	
Byte 1	Head Number			0	0	Cyl High		
Byte 2	Cylinder Low							
Byte 3	Sector Number							
Byte 4	0	0	0	0	0	0	1	0
Byte 5	Number of Sectors							

Byte 0

Bit 7 - 4 The codes and their commands are explained later in this section.

Bit 3 When set, this bit indicates that the data transfer is only between the disk drive and the sector buffer. No data is transferred to the system. When this option is specified, only one sector is transferred to prevent overrun errors.

Bit 2 When set, this bit instructs the drive to seek the cylinder specified in the command block. When clear, the head positioning mechanism must be positioned to the desired cylinder using the Seek command before any other operation.

Bit 1 Must be written as 0.

Bit 0 When set, this bit indicates that data fields or sectors are processed using error checking and correction (ECC) rather than cyclic redundancy checking (CRC).

Byte 1

Bits 7 - 4 These four bits define the head number selected. Because there are only two heads, the three most-significant bits are always 0.

Bits 3, 2 Must be written as 0.

Bits 1, 0 These are the two most-significant bits of the cylinder number.

Byte 2 Cylinder Low: This byte contains the eight least-significant bits of the cylinder number.

Byte 3 Sector Number: This byte specifies the sector number being processed. For multiple sector operations, it specifies the starting sector number.

Byte 4 Sector Size: This byte contains the encoded value for the sector size. The value is always hex 02 to indicate 512 bytes.

Byte 5 Number of Sectors: This byte specifies the number of sectors that are to be processed. The system must provide for the correct amount of data transferred because the controller does not interrupt the system between sectors.

Command Specify Block

The command specify block (CSB) controls the error recovery procedures of the drive. The drive assumes the default parameters following power on and reset. These default values can be overridden by issuing a command specify block after initialization of the drive. All 14 bytes of the CSB are not used by the drive and controller; however, all bytes must be sent.

The command specify block is described in the following.

	7	6	5	4	3	2	1	0
Byte 0	En	0	0	0				Retries
Byte 1	Reserved = 0							
to								
Byte 13	Reserved = 0							

Byte 0 Control

Bit 7 When set, this bit causes the drive to correct an ECC error in the sector buffer. The default is ECC enabled.

Bits 6 - 4 Must be written as 0.

Bits 3 - 0 These bits specify the number of retries that the drive performs on an operation before reporting the error. The default is 15 retries.

Sense Summary Block

The sense summary block contains the current status of the drive. The information in the summary block is updated after each command is completed, after an error, or before the block is transferred.

If the Interrupt Status register shows an error (bit 1 set), the system requests 14 bytes of sense data by setting bit 5 in the Attention register. The format for the summary block is:

Figure 8-9. Sense Summary Block

	7	6	5	4	3	2	1	0
Byte 0	-R	SE	0	WF	CE	0	0	T0
Byte 1	EF	ET	AM	BT	WC	0	0	ID
Byte 2	0	RR	RG	DS				Hd Sel State
Byte 3	Cylinder Low							
Byte 4	DS	Cyl High	0					Hd Number
Byte 5	Sector Number							
Byte 6	Sector Size (hex 02)							
Byte 7		Hd Number		0	0			Cyl High
Byte 8	Cylinder Low							
Byte 9	Number of Sectors Corrected							
Byte 10	Number of Retries							
Byte 11	Command Syndrome							
Byte 12	Drive Type Identifier							
Byte 13	Reserved							

Status Bytes

The first three bytes contain status information on the drive and controller signals.

Status Byte 0

- Bit 7** When set, this bit indicates that the drive is not ready.
- Bit 6** When set, this bit indicates that the drive has completed a seek operation.
- Bit 5** Reserved.
- Bit 4** When set, this bit indicates that the drive has shown a write-fault condition.
- Bit 3** When set, this bit indicates that the controller has received a request to step beyond the limit of the last cylinder. The park option of the Seek command does not cause this bit to be set.

When the CCB specifies a cylinder beyond the limit, no step operation is done and the heads do not move. When the CCB started at a valid cylinder but involved multiple track operations that exceeded the limit, the heads are at the limit.

Bits 2, 1 Reserved.

- Bit 0** When set, this bit indicates the heads are at track 0.

Status Byte 1

- Bit 7** This bit indicates the type of field (ID or data) that caused the uncorrectable error. When set, this bit indicates an ID field.
- Bit 6** When set, this bit indicates a CRC or uncorrectable ECC error occurred. The field is identified by bit 7.
- Bit 5** When set, this bit indicates that the address mark for the data field of the requested sector was not found.
- Bit 4** When set, this bit indicates an ID field with all bits set was detected.
- Bit 3** When set, this bit indicates that the cylinder bytes read did not match the cylinder requested in the CCB.
- Bit 2, 1** Reserved.
- Bit 0** When set, this bit indicates an ID match was not found and the complete track was searched.

Status Byte 2

Bit 7 Reserved.

Bit 6 When set, this bit indicates that the drive needs to be reset.

Bit 5 When set, this bit indicates that the read or write retry corrected the error condition.

Bit 4 When set, this bit indicates that the defective sector bit in the ID field is set to 1.

Bits 3 - 0 These bits reflect the state of the head select signals to the drive.

Bytes 3 through 6 Last ID: These bytes represent the cylinder, head, sector number, and sector size of the last ID field processed. The most-significant bit of byte 4 is set if the operation was to a defective sector.

Bytes 7 and 8 Present ID: These bytes represent the true cylinder and head numbers of the present head location in the same format as bytes 1 and 2 of the CCB.

Byte 9 NSC: This byte contains the number of sectors corrected by the ECC before transfer.

Byte 10 Retry Tally: This byte contains the number of retries attempted during the last operation. When this byte reaches the maximum value, the controller halts operation until it is reset. This value, 255, does not depend on the value allowed for any one sector.

Byte 11 Command Syndrome: This byte shows the progress of the controller through the last command. It allows the system to monitor the controller and determine if a reset is needed. When the transfer of the control block is started, the value is set to hex 00. The progress indicated by this byte is:

1. Set to hex 01 after the control block is successfully transferred.
2. Set to hex 02 when the command is valid and the drive is ready.
3. Set to hex 03 when the head is in the correct track. The most-significant four bits (high nibble) are then used to indicate the successful stages of the data transfer.

Bit 7 A sector was transferred between the system and the sector buffer.

Bit 6 A sector was transferred between the controller and the sector buffer.

Bit 5 An error was detected and error recovery procedures have been started.

Bit 4 The controller has completed the operation and is now not busy.

4. When the transfer is complete, the low nibble equals hex 4 and the high nibble is unchanged.

Byte 12 Drive Type Identifier: This byte contains an 8-bit identifier code for the fixed disk drive installed. The system can read this code to set the drive type using the drive configuration table.

Byte 13: This bit is reserved.

Format Control Block

The format control block (FCB) specifies the ID data used in formatting the track. It is used by the Format Track and Format Disk commands and contains five bytes for each sector formatted on that track.

When the Format Disk command is used, the control block contains the sector information of all sectors for head 0, cylinder 0. The drive will use the same block to format the rest of the disk and automatically increment the head number and cylinder number for the remaining tracks. The sector numbers, sector size, and the fill byte will be the same for each track.

The drive formats the sector IDs on the disk in the same order as they are specified in the control block. Therefore, sector interleaving is accomplished by filling in the control block with the desired interleave. For example, when formatting 17 sectors per track with an interleave of 2, the control block has the first 5 bytes with a sector number of 1, the second with a sector number of 10, the third with a sector number of 2, and continuing until all 17 sectors for that track are defined.

The format for the format control block is described in the following. The five bytes are repeated for each sector on the track. The control block must contain an even number of bytes. If an odd number of sectors are being formatted, an additional byte is sent with all bits 0.

Figure 8-10. Format Control Block

	7	6	5	4	3	2	1	0
Byte 0	Hd Number				0	DS	Cyl High	
Byte 1	Cylinder Low							
Byte 2	Sector Number							
Byte 3	0	0	0	0	0	0	1	0
Byte 4	Fill Byte							

Sector Information: The five bytes of sector information contains the same basic information for Format Disk and Format Track.

Byte 0: This byte contains the head select bits (7 through 4), the defective sector bit (2), and the two most-significant bits for the cylinder number (1 and 0).

Byte 1: This byte contains the low-order bits of the cylinder number.

Byte 2: This byte contains the sector number written in the ID field for that sector.

Byte 3: This byte specifies the sector size.

Byte 4: This byte contains the fill character for each sector. This is the value that is written into each byte in the data field of the formatted sector. To identify an entire track as defective, the system performs a Format Track command with all five bytes of the FCB for each sector set to hex FF.

Commands

The commands to the controller are in the first byte of the CCB. The command determines the number of bytes and the particular bits used, even though the CCB always contains the full six bytes.

Read Data: This command is the normal Read command. The number of sectors specified is read from the disk and transferred to the system. Up to 255 sectors can be specified in one CCB. The controller automatically increments the head and cylinders as necessary to satisfy the sector count. If this feature is used, the sectors must be numbered the same for all tracks. The CCB for the Read Data command is:

<i>Figure 8-11. Read Command</i>	
	7 6 5 4 3 2 1 0
Byte 0	0 0 0 1 ND AS 0 E
Byte 1	Hd Number 0 0 Cyl High
Byte 2	Cylinder Low
Byte 3	Sector Number
Byte 4	0 0 0 0 0 0 1 0
Byte 5	Number of Sectors

Read Check: This command reads the data from the disk without transferring it to the system. It serves to verify the readability of the data and the correctness of the CRC or ECC field. Multiple sectors, up to 255, can be tested in this manner. This command is similar to the Read Data command with the No Data option specified. The difference is that the Read Check command can specify more than one sector.

<i>Figure 8-12. Read Check Command</i>	
	7 6 5 4 3 2 1 0
Byte 0	0 0 1 0 0 AS 0 E
Byte 1	Hd Number 0 0 Cyl High
Byte 2	Cylinder Low
Byte 3	Sector Number
Byte 4	0 0 0 0 0 0 1 0
Byte 5	Number of Sectors

Read Extended: This command reads and transfers the specified sector along with the associated CRC or ECC bytes to the system. Six bytes of error checking are transferred with the sector data regardless of the error checking used. When using this command, the controller does not check the data for errors.

Figure 8-13. Read Extended Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	1	1	0	AS	0	E
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	Sector Number							
Byte 4	0	0	0	0	0	0	1	0
Byte 5	X	X	X	X	X	X	X	X

Read ID: This command reads the ID from the first sector encountered on the specified head and cylinder. This command is used to verify the current head position on the drive.

Note: Because of the freedom allowed in the Format Track command, it is possible to format a track with IDs containing different cylinder values than the actual cylinder.

Figure 8-14. Read ID Command

	7	6	5	4	3	2	1	0
Byte 0	0	1	0	1	0	AS	0	0
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	X	X	X	X	X	X	X	X
to								
Byte 5	X	X	X	X	X	X	X	X

Recalibrate: This command moves the heads to cylinder 0. If the operation fails, the termination error bit is set in the Interrupt Status register.

Figure 8-15. Recalibrate Command

	7	6	5	4	3	2	1	0
Byte 0	1	0	0	0	0	0	0	0
Byte 1	X	X	X	X	X	X	X	X
to								
Byte 5	X	X	X	X	X	X	X	X

Write Data: This command is the normal Write command. Data is written on the fixed disk in consecutive sectors, beginning with the sector number in byte 3. Up to 255 sectors can be processed with each command. When more than one track of data is being transferred, the controller automatically increments the head and cylinder number as necessary.

There are two items to consider when performing multiple track transfers:

1. Because the controller adjusts the head and cylinder number automatically, all cylinders must have the same sector numbering.
2. Because the system is not interrupted until the entire operation is completed or an error occurs, the system must be sure to transfer the stated amount of data.

Figure 8-16. Write Data Command

	7	6	5	4	3	2	1	0
Byte 0	1	0	0	1	ND	AS	0	E
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	Sector Number							
Byte 4	0	0	0	0	0	0	1	0
Byte 5	Number of Sectors							

Write Verify: This command is a combination of two commands, Write Data and Read Check. After the data is written, the controller reads the data for ECC errors. For multiple track operations, the read check is performed on the track boundary to prevent unnecessary track steps.

Figure 8-17. Write Verify Command

	7	6	5	4	3	2	1	0
Byte 0	1	0	1	0	ND	AS	0	E
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	Sector Number							
Byte 4	0	0	0	0	0	0	1	0
Byte 5	Number of Sectors							

Write Extended: This command is similar to the Read Extended command. The data and the six bytes of error checking are written to the specified sector. The drive does not error check. If the error checking option is CRC, then only the first two bytes are written but all six bytes must be sent.

Figure 8-18. Write Extended Command

	7	6	5	4	3	2	1	0
Byte 0	1	0	1	1	0	AS	0	E
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	Sector Number							
Byte 4	0	0	0	0	0	0	1	0
Byte 5	X	X	X	X	X	X	X	X

Format Disk: This command writes the entire disk with the filler and ID information supplied in the format control block. This control block contains the format for head 0 of cylinder 0. The controller then increments the head and cylinder numbers as needed until the disk is completely formatted.

The number of sectors specified in byte 5 is the number of sectors per track.

Figure 8-19. Format Disk Command

	7	6	5	4	3	2	1	0
Byte 0	1	1	0	1	0	0	0	E
Byte 1	X	X	X	X	X	X	X	X
Byte 2	X	X	X	X	X	X	X	X
Byte 3	X	X	X	X	X	X	X	X
Byte 4	0	0	0	0	0	0	1	0
Byte 5	Number of Sectors							

Seek: This command causes the drive to position the heads at the specified cylinder. The position is not verified, even though the Present Cylinder Number fields are updated in the sense summary block. In all Read and Write commands, an implicit Seek command can be performed by choosing the Auto Seek option.

When the park option bit is set (bit 0 of byte 0), the controller positions the heads over the landing zone. No cylinder or head information is needed because it is assumed to be the last cylinder, therefore, bytes 1 and 2 become "don't care."

Figure 8-20. Seek Command

	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	0	P
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	X	X	X	X	X	X	X	X
to								
Byte 5	X	X	X	X	X	X	X	X

Format Track: This command writes a single track with ID and filler information. This information is supplied by the system in the FCB. In contrast to the Format Disk command, Format Track command allows the system to format defective or other non-standard tracks.

Figure 8-21. Format Track Command

	7	6	5	4	3	2	1	0
Byte 0	1	1	1	1	0	AS	0	E
Byte 1	Hd Number				0	0	Cyl High	
Byte 2	Cylinder Low							
Byte 3	X	X	X	X	X	X	X	X
Byte 4	0	0	0	0	0	0	1	0
Byte 5	Number of Sectors							

Connector

The fixed disk drive and controller connector and interface specifications are shown below.

Pin numbers are consistent with those numbers on the system board and cable connector.

Figure 8-22. Fixed Disk Connector

Pin	I/O	Signal	Pin	I/O	Signal
44	I	RESET DRV	43	O	-DISK Installed
42	I/O	D0	41	N/A	Ground
40	I/O	D1	39	N/A	Ground
38	I/O	D2	37	N/A	Ground
36	I/O	D3	35	N/A	Ground
34	I/O	D4	33	N/A	Ground
32	I/O	D5	31	N/A	Ground
30	I/O	D6	29	N/A	Ground
28	I/O	D7	27	N/A	Ground
26	I	-IOR	25	N/A	Ground
24	I	-IOW	23	N/A	Ground
22	I	-DISK CS	21	N/A	Ground
20	I	A0	19	N/A	Ground
18	I	A1	17	N/A	Ground
16	I	A2	15	N/A	+5
14	I	A3	13	I/O	+5
12	I/O	-DACK3	11	N/A	Ground
10	I/O	DRQ3	9	N/A	Ground
8	O	IRQ 14	7	N/A	Ground
6	O	IO CH RDY	5	I	+12
4	N/A	Spare	3	I	+12
2	N/A	Spare	1	I	+12

Signal Description

The following lines are used by the drive and controller:

- A0 – A3** These four address bits are used to select the specific register within the controller. The other address lines are not needed because address decoding is done on the system board.
- D0 – D7** Positive 8-bit data bus over which data and status information is passed between the system and the controller.
- IOR** When active, the “-I/O read” signal instructs the controller to write its data onto the data bus.
- IOW** When active, the “-I/O write” signal instructs the controller to read the data on the data bus.
- RESET DRV** When active, the “reset driver” signal forces the controller to a reset state. The controller initializes when RESET DRV goes inactive.
- IRQ 14** This signal is made active by the controller after status information is returned. This signal is enabled and disabled through the Attachment Control register.
- IO CH RDY** This signal is used to lengthen I/O and DMA operations. The controller makes the signal inactive to add wait states.
- DRQ 3** This signal is activated by the controller when data is available for transfer under DMA control and remains active until the “DMA acknowledge” signal (-DACK 3) becomes active. It is enabled and disabled through the Attachment Control register.
- DACK 3** This signal is active in response to a DMA request.
- DISK CS** The address decode logic for the fixed disk is on the system board. It is enabled through the Planar Control register. When the logic is enabled, the “-disk card select” signal goes active on a valid decode of A4 through A19 equal to hex 032x.
- DISK Installed** When active, this signal indicates that the drive and controller are installed.

Specifications

There are two 30MB fixed disk drives and controllers. Each system's read-only memory (ROM) contains a parameters table. If a fixed disk drive is supported by a system, the drive type will be listed on the parameters table.

The following are specifications for the 30MB fixed disk drives and controllers.

	Drive Type 35	Drive Type 38
Formatted Capacity		
• Bytes/Sector	512	512
• Sectors/Track	33	36
• Cylinders	921	845
• Heads	2	2
Rotational Speed	3600 rmp	3700 rpm
Transfer Rate	10.2M bps	10.8M bps
Access Time*		
• Track to Track	8 ms	9 ms
• Average (transverse 1/3 cylinder)	19 ms	21 ms
• Maximum	40 ms	40 ms
Interleave	4:1	4:1

* Nominal environmental and voltage conditions.

Figure 8-23. DC Power Specifications (for both drives)

• Nominal Supply	+5 V	+12 V
• Tolerance	±5%	±8%
• Supply Current		
Idle, R/W Mode	0.4 A max	0.6 A max
Seeking	0.4 A max	0.8 A max
Startup	0.4 A max	1.2 A max

3.5-Inch 1.44MB Diskette Drive

Description

This section describes the 3.5-inch 1.44MB diskette drive option. This drive is a direct-access device containing a spindle drive, head positioning mechanism, and read/write/erase logic. A drive-in-use indicator lights when the drive is selected.

The 3.5-inch 1.44MB diskette drive accepts either 1MB or 2MB capacity diskettes with 80 tracks on each side. The 3.5-inch 1.44MB diskette drive is identified externally by a "1.44" printed on its diskette eject button.

The spindle mechanism spins the diskette at a constant speed of 300 revolutions per minute (rpm). A sensor generates an index signal once per rotation of the spindle motor. The two read/write heads are positioned over the desired track of the diskette by a stepper motor. One step of the stepper motor results in a one-track linear movement of the read/write heads. An optical sensor generates a signal when the heads are over track 0.

During a write operation, data is provided to the drive in modified frequency modulation (MFM) coded form by a diskette drive controller.

If the diskette is write-protected, the drive's write-protect sensor inhibits the write operation.

Programming Considerations

The following describes the interface to the diskette drive:

Signal Levels

All input signals operate between +5 V dc and ground with the following definitions:

- The inactive level is +2.0 V dc minimum
- The active level is +0.8 V dc maximum.

All outputs from the drive can sink 4.0 mA at the active (low) level. All interface signals are CMOS compatible.

Connector

The interface is divided into three categories: Control, Data, and DC power. These signals are all provided through a 34-pin header connector. Even-numbered pins are located on the top row and odd-numbered pins are located on the bottom row (closest to the PC board). Pins are located on 2.54-millimeter centers.

Figure 8-24. Connector Pin Assignments

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Signal Ground	2	I	-High Density Select
3	I	+5 V	4	O	-Drive Type 1
5	N/A	Signal Ground	6	I	+12 V
7	N/A	Signal Ground	8	O	-Index
9	N/A	Signal Ground	10	N/A	-Open
11	N/A	Signal Ground	12	I	-Drive Select
13	N/A	Signal Ground	14	N/A	-Open
15	N/A	Signal Ground	16	I	-Motor Enable
17	N/A	Signal Ground	18	I	-Direction
19	N/A	Signal Ground	20	I	-Step
21	N/A	Signal Ground	22	I	-Write Data
23	N/A	Signal Ground	24	I	-Write Enable
25	N/A	Signal Ground	26	O	-Track 0
27	N/A	Signal Ground	28	O	-Write Protect
29	N/A	Signal Ground	30	O	-Read Data
31	N/A	Signal Ground	32	I	-Head 1 Select
33	N/A	Signal Ground	34	O	-Diskette Change

Specifications

The following are specifications for the 3.5-inch diskette drive.

Size

- Width: 102 millimeters (4.0 inches)
- Depth: 150 millimeters (5.9 inches)
- Height: 25.4 millimeters (1.0 inch).

Weight 0.45 kilograms (1.0 pound).

Voltage

- +12 V dc
- +5 V dc.

Media

- 3.5-inch ANSI compatible
- Media Capacity 1MB 2MB
 - Unformatted 500KB per side 1MB per side
 6.25KB per track 12.50KB per track
 - Formatted 720KB (360KB
 per side) 1.44MB (720KB
 4.5KB per track. 9KB per track.

Track Density 135 tracks per inch.

Tracks 80.

Number of Heads 2.

Transfer Rate

- 3.5-inch 720KB diskette: 250,000 bps (MFM)
- 3.5-inch 1.44MB diskette: 500,000 bps (MFM).

Access Time

- Track-to-Track: 3 milliseconds
- Seek Settle Time: 15 milliseconds
- Motor Start Time: 500 milliseconds (maximum).

Disk Speed 300 rpm \pm 1.5%.

