CA810 Motherboard Specification Update

Release Date: April 2000

Order Number: 738240-009

The CA810 motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call in North America 1-800-548-4725, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333, other Countries 708-296-9333

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
March 1999	-001	This document is the first Specification Update for the Intel® CA810 motherboard.
July 1999	-002	Added Documentation Change 1.
August 1999	-003	Added Specification Change 1 and Documentation Change 2.
September 1999	-004	Modified Specification Change 1. Added Specification Changes 2-4 and Documentation Changes 3-5.
October 1999	-005	Added Errata 1-2.
January 2000	-006	Added Erratum 3 and updated Erratum 1.
February 2000	-007	Modified Specification Change 4. Added Errata 4-7 and Documentation Change 6.
March 2000	-008	Added Specification Change 5 and Errata 8-10.
April 2000	-009	Added Specification Change 6 and Erratum 11.

PREFACE

This document is an update to the specifications contained in the CA810 Motherboard Technical Product Specification (Order number 733082). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Celeron™ Processor Specification Update* (Order number 243748) for specification updates concerning the Intel Celeron processor. Items contained in the *Intel Celeron Processor Specification Update* that either do not apply to the CA810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) for specification updates concerning the 82810 GMCH Controller. Items contained in the *82810 GMCH Specification Update* that either do not apply to the CA810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any GMCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82801 I/O Controller Hub (ICH) Specification Update* (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the *Intel 82801 ICH Specification Update* that either do not apply to the CA810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *Intel® 82802 Firmware Hub (FWH) Specification Update* (Order Number TBD) for specification updates concerning the 82802 Firmware Hub. Items contained in the *Intel 82802 FWH Specification Update* that either do not apply to the CA810 desktop board or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the CA810 motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for CA810 Motherboards

GENERAL INFORMATION

Basic CA810 Motherboard Identification Information

AA Revision	PBA Revision	BIOS Revision	Notes
730959-422	730960-422	8C1A100A.86A.0010.P03	1-6
730959-443	730960-443	8C1A100A.86A.0015.P07	1-6
744854-421	744855-421	8C1A100A.86A.0010.P03	1-6
744854-441	744855-441	8C1A100A.86A.0013.P06	1-6
744854-442	744855-442	8C1A100A.86A.0015.P07	1-6
744854-443	744855-443	8C1A100A.86A.0015.P07	1-6
744854-444	744855-444	8C1A100A.86A.0015.P07	1-6
A09251-300	A09252-300	8C1A100A.86A.0019.P10	1-6
A09253-300	A09255-300	8C1A100A.86A.0019.P10	1-6

NOTES:

1. The PBA number or AA number is found on a small label on the component side of the board.
2. The 82810 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82810 GMCH	A2	SL35X
82801AB ICH	B0	SL38J
82802AB FWH	A0	SB48

3. The following errata are contained in the *Intel® Celeron™ Processor Specification Update* (Order Number 243748) for the Celeron processor and either do not apply to the CA810 motherboard or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
4. The following items are contained in the *Intel® 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) and either do not apply to the CA810 motherboard or have been worked around in this PBA and/or BIOS revision:
   1 in BIOS Revision 8C1A100A.86A.0010.P03 and greater
   12 in BIOS Revision 8C1A100A.86A.0012.P05 and greater
   All other errata associated with the GMCH apply to this PBA revision.
5. The following items are contained in the *Intel® 82801 I/O Controller Hub Specification Update* (Order Number TBD) and either do not apply to the CA810 motherboard or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.
6. The following items are contained in the *Intel® 82802 Firmware Hub Specification Update* (Order Number TBD) and either do not apply to the CA810 desktop board or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the FWH apply to this PBA revision.

7. The 82810 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82810 GMCH	A3	SL3P7
82801AB ICH	B0	SL38J
82802AB FWH	A0	SB48

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the CA810 motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	New BIOS Features
2	Doc	Change to Section 4.4.4, Table 62, IDE Configuration Submenus
3	Doc	Change to Section 4.5, Security Menu
4	Doc	Support for faster Intel® Celeron™ processors
5	Doc	Support for the Intel® Pentium® III processor
6	Doc	Diagnostic LED display changes
NO.	**PLANS**	**ERRATA**
1	Fixed	Multi-language support is not available
2	Fixed	Suspend to RAM does not function
3	Fixed	System does not boot to network using PXE option
4	Fixed	Onboard audio distorts certain files during playback
5	Fixed	Some presentation applications may fail with an illegal operation
6	Fixed	Video drivers incompatible with LDCM version 6.0
7	Fixed	Wake on LAN* may not function
8	Fixed	BIOS does not fill DMI memory structure
9	Fix	BIOS setup does not allow user to define IRQ 5
10	Fix	Fan tach header control not supported
11	Fix	BIOS does not generate error when an unformatted floppy is in the floppy drive during system boot
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Change to Description of Supported Memory
2	Doc	In Table 60, Peripheral Configuration Submenu, the default interrupt for the parallel port should be IRQ 7

NO.	PLANS	DOCUMENTATION CHANGES
3	Doc	Change in Section 4.4, Table 58, Advanced Menu
4	Doc	Change in Section 4.4.2, Table 60, Peripheral Configuration Submenu
5	Doc	Change in Section 4.6, Table 66, Power Menu
6	Doc	Change to description of manufacturing options

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual erratum referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
730960-422	8C1A100A.86A.0010.P03	1-3,6-8,11
	8C1A100A.86A.0011.P04	1-3,6-8,11
	8C1A100A.86A.0012.P05	1-3,6-8,11
	8C1A100A.86A.0013.P06	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
730960-443	8C1A100A.86A.0010.P03‡	1-3,6-8,11
	8C1A100A.86A.0011.P04‡	1-3,6-8,11
	8C1A100A.86A.0012.P05‡	1-3,6-8,11
	8C1A100A.86A.0013.P06‡	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
744855-421	8C1A100A.86A.0010.P03	1-3,6-8,11
	8C1A100A.86A.0011.P04	1-3,6-8,11
	8C1A100A.86A.0012.P05	1-3,6-8,11
	8C1A100A.86A.0013.P06	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
744855-441	8C1A100A.86A.0010.P03‡	1-3,6-8,11
	8C1A100A.86A.0011.P04‡	1-3,6-8,11
	8C1A100A.86A.0012.P05‡	1-3,6-8,11
	8C1A100A.86A.0013.P06	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11

PBA Revision	BIOS Revision	Errata That Apply
744855-441	8C1A100A.86A.0019.P10	9,11
744855-442	8C1A100A.86A.0010.P03‡	1-3,6-8,11
	8C1A100A.86A.0011.P04‡	1-3,6-8,11
	8C1A100A.86A.0012.P05‡	1-3,6-8,11
	8C1A100A.86A.0013.P06‡	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
744855-443	8C1A100A.86A.0010.P03‡	1-3,6-8,11
	8C1A100A.86A.0011.P04‡	1-3,6-8,11
	8C1A100A.86A.0012.P05‡	1-3,6-8,11
	8C1A100A.86A.0013.P06‡	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
744855-444	8C1A100A.86A.0010.P03‡	1-3,6-8,11
	8C1A100A.86A.0011.P04‡	1-3,6-8,11
	8C1A100A.86A.0012.P05‡	1-3,6-8,11
	8C1A100A.86A.0013.P06‡	1-3,6-8,11
	8C1A100A.86A.0015.P07	1,3,9,11
	8C1A100A.86A.0017.P08	9,11
	8C1A100A.86A.0018.P09	9,11
	8C1A100A.86A.0019.P10	9,11
A09252-300	8C1A100A.86A.0019.P10	9,11‡‡
A09255-300	8C1A100A.86A.0019.P10	9,11‡‡

‡ Note: This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

‡‡ Note: Due to hardware changes, BIOS 8C1A100A.86A.0019.P10 or later should be used only on PBA's that are -300 or later.

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *CA810 Motherboard Technical Product Specification* (Order Number 733082). All Specification Changes will be incorporated into a future version of that specification.

1. New BIOS Features

Several new features have been added in BIOS revision 8C1A100A.86A.0010.P03 and later. The following documentation changes will be made in Chapter 4, BIOS Setup Program, to describe how to control these features.

In Table 54, Setup Menu Bar, the description of the Maintenance and Main items is as follows:

BIOS Setup Program Menu Screen	Description
Maintenance	Used for clearing the BIOS Setup program passwords and extended configuration options. This menu is only available in configure mode.
Main	Displays system configuration information and allows user to reset the time and date.

A new Extended configuration option has been added to the Maintenance menu. This menu is for clearing the Setup Password and extended configurations. This option will be added to Table 56, Maintenance Menu.

Feature	Options	Description
Extended Configuration	No options	Allows user to manually configure advanced memory settings.

A new section will be inserted to describe the functions available through the extended configuration option. Following sections and tables will be renumbered as needed.

Extended Configuration Menu

This menu allows the user to manually configure memory settings that are highly technical.

CAUTION

Choosing the wrong settings could cause system problems. Do not change these settings unless you have all the necessary information about the installed memory.

Table 1. Extended Configuration Menu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User defined	Enables access to the extended memory configuration options.
SDRAM Auto-Configuration	• **Auto (default)** • User defined	Sets extended memory configuration options to auto or user defined.
SDRAM CAS# Latency	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.

The Main Menu displays the type of memory installed in the system and allows the system time and date to be changed. Table 57, Main Menu, will be updated with the following changes:

Feature	Options	Description
Bank 0 Bank 1	No options	Displays size and type of DIMM installed in each memory bank.
System Time	Hour, minute, and second	Displays and allows system time to be set.
System Date	Month, day, and year	Displays and allows system date to be set.

Two options have been added to Table 58, Advanced Menu.

Feature	Options	Description
Extended Configuration	No options	Indicates whether extended configuration settings have been modified from the default setting.
PCI Configuration	No options	Allows access to PCI IRQ mapping.

The PCI Configuration Submenu option has been added to allow PCI interrupts for slots 2, 3, and 4 to be assigned a priority mapping to a specific IRQ. The following section has been added to document this feature. Following sections and tables will be renumbered as needed.

PCI Configuration Submenu

This menu is for accessing PCI IRQ mapping.

Table 2. PCI Configuration Submenu

Feature	Options	Description
PCI Slot2 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 2 to a particular hardware interrupt.
PCI Slot3 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 3 to a particular hardware interrupt.
PCI Slot4 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows the user to map the PCI IRQ for slot 4 to a particular hardware interrupt.

The Video Configuration Submenu has been added to allow the user to specify which video adapter to use as the primary adapter in a multimonitor system. Following sections and tables will be renumbered as needed.

VIDEO CONFIGURATION SUBMENU

This submenu is for configuring video features.

Table 3. Video Configuration Submenu

Feature	Options	Description
Primary Video Adapter	• **AGP (default)** • PCI	Allows the user to select between the onboard direct AGP graphics or a PCI add-in graphics card as primary graphics adapter in a multi-monitor system.

In Table 66, Power Menu, an option has been added for selecting the ACPI suspend state.

Feature	Options	Description
ACPI Suspend State	• **S1 State (default)** • S3 State	Selects the suspend state the system will use when ACPI power management is active. To enable an instantly available configuration, this must be set to the S3 state and an operating system which fully supports the ACPI S3 suspend state must be installed.

2. Change to Section 4.4.4, Table 62, IDE Configuration Submenus

Ultra DMA Mode 4 is supported and will be added to the Ultra DMA options in Table 62.

3. Change to Section 4.5, Security Menu

Table 65 will be replaced in its entirety as follows:

Feature	Options	Description
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.

4. Support for Faster Intel® Celeron™ Processors

The following will be added to Table 1, Processor Speeds Supported by the Motherboard, in Section 1.3, Processor:

Processor Speed	Host Bus Frequency	Cache Size
500 MHz	66 MHz	128 KB
533 MHz	66 MHz	128 KB

5. Support for the Intel® Pentium® III Processor

The following will be added to Section 1.1, Overview, as a bullet under the heading Processor:

- Pentium® III processor, in a 370-pin PPGA socket, with 100 MHz host bus speed

Section 1.3, Processor, will be replaced in its entirety as follows:

1.3 PROCESSOR

The motherboard supports a single Pentium III or Celeron™ processor. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. The host bus frequency of 66 MHz or 100 MHz is automatically selected. The processor connects to the motherboard through the 370-pin PPGA socket.

The motherboard supports the processors listed in Table 4.

Table 4. Processors Supported by the Motherboard

Processor Type	Processor Speed	Host Bus Frequency	Cache Size
Celeron Processors	333 MHz	66MHz	128KB
	366Mhz	66MHz	128KB
	400Mhz	66MHz	128KB
	433Mhz	66MHz	128KB
	466Mhz	66MHz	128KB
	500Mhz	66MHz	128KB
	533Mhz	66MHz	128KB
Pentium III Processors	500EMhz	100MHz	256KB
	550EMhz	100MHz	256KB
	600EMhz	100MHz	256KB
	650Mhz	100MHz	256KB
	700Mhz	100MHz	256KB
	750Mhz	100MHz	256KB
	800Mhz	100MHz	256KB

All supported onboard memory can be cached, up to the cacheability limits of the processor.

For the latest information on processor support for the CA810 motherboard, refer to the Intel boxed motherboard web site at:

http://support.intel.com/support/motherboards/desktop/

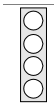
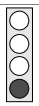
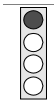
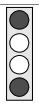
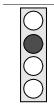
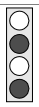
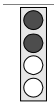
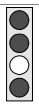
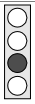
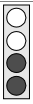
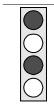
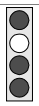
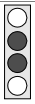
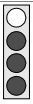
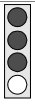
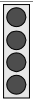
The following motherboard revisions, or later, support the Pentium® III processor at 500 MHz or faster with BIOS version 8C1A100A.86A.0019.P10 or later. Earlier motherboard and BIOS revisions do not support the Pentium III processor.

Product Code	MM#	AA#	PBA#
BECAPA413	827937	A09253-300	A09255-300
BECAPA41L3	827938	A09251-300	A09252-300

6. Diagnostic LED Display Changes

Section 5.6 Enhanced Diagnostics, Table 74 will be updated to reflect the following changes of the diagnostic LED's.

Table 74. Diagnostic LED Codes

Display		BIOS Operation	Display		BIOS Operation
	Amber Amber Amber Amber	Power on, starting BIOS		Amber Amber Amber Green	Undefined
	Green Amber Amber Amber	Recovery mode		Green Amber Amber Green	Undefined
	Amber Green Amber Amber	Processor, cache, etc.		Amber Green Amber Green	Undefined
	Green Green Amber Amber	Memory, auto-size, shadow, etc.		Green Green Amber Green	Undefined
	Amber Amber Green Amber	PCI bus initialization		Amber Amber Green Green	Undefined
	Green Amber Green Amber	Video		Green Amber Green Green	Undefined
	Amber Green Green Amber	IDE bus initialization		Amber Green Green Green	Reserved
	Green Green Green Amber	USB initialization		Green Green Green Green	Booting operating system

ERRATA

1. Multi-language Support not Available

PROBLEM: The option to choose a different language in BIOS Setup is not available.

IMPLICATION: The user will not be able to choose an alternate BIOS Setup language. The only language available is US English.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 8C1A100A.86A.0017.P08.

2. Suspend to RAM does not Function

PROBLEM: The Suspend to RAM (ACPI S3 State) feature of the motherboard will not function correctly.

IMPLICATION: The operating system will not be able to suspend the system to RAM. When set to suspend, the system will not go into the S3 State. The ACPI S1 State will function normally.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 8C1A100A.86A.0013.P06.

3. System Does Not Boot to Network Using PXE Option

PROBLEM: If the PXE option is selected as the first boot option in the BIOS setup program and a bootable IDE hard disk drive is attached and selected as the second or third boot device, then the system will bypass the PXE option and boot to the hard disk drive instead of the network. BIOS 8C1A100A.86A.0013.P06 and earlier are not subject to this erratum.

IMPLICATION: Users who require the PXE network boot option will not be able to boot to the network with an IDE hard disk drive attached and selected as the second or third boot option.

WORKAROUND: After selecting the PXE option as the first boot device, upon reboot (during POST) and after the keyboard has been detected, simultaneously press both shift keys. This will bring up a bootstrap selection menu. Choose option 3 or 4. Subsequent boots will allow booting to the network.

STATUS: This was fixed in BIOS revision 8C1A100A.86A.0017.P08.

4. Onboard Audio Distorts Certain Files During Playback

PROBLEM: Wave files in the Microsoft ADPCM stereo format sampled at 44Kbit per second will be distorted during playback.

IMPLICATION: The user may experience intermittent crackling or dropout during playback.

WORKAROUND: None.

STATUS: This erratum was fixed in audio driver revision 4.10.55.

5. Some Presentation Applications May Fail With an Illegal Operation

PROBLEM: When the option to create a new presentation is chosen, the user will experience illegal operation errors when selecting a template and the program will terminate.

IMPLICATION: These applications will be unusable unless audio drivers are upgraded.

WORKAROUND: None.

STATUS: This erratum was fixed in audio driver revision 4.06.1167.

6. Video Drivers Incompatible With LDCM Version 6.0

PROBLEM: Intel® LANDesk® Client Manager version 6.0 will not operate correctly with early versions of CA810 graphics drivers.

IMPLICATION: The LDCM version 6.0 application will fail to run if using early video drivers.

WORKAROUND: Use standard VGA drivers.

STATUS: This erratum was fixed with video driver revision 4.11.01.2523 and BIOS revision 8C1A100A.86A.0015.P07.

7. Wake On LAN* May Not Function

PROBLEM: Using WOL, the system may not wake from power down or standby modes.

IMPLICATION: The user may not be able to awaken the system from standby or power down states using the LAN.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 8C1A100A.86A.0015.P07.

8. BIOS Does Not Fill DMI Memory Structure

PROBLEM: At system boot, the BIOS does not fill in all entries in the DMI system memory structure.

IMPLICATION: A user with third party system management software may receive an error that the system memory is not recognized.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 8C1A100A.86A.0015.P07.

9. BIOS Setup Does Not Allow User to Define IRQ5

PROBLEM: IRQ 5 is not an available option in the PCI Configuration menu of the system BIOS.

IMPLICATION: If the user wishes to reserve IRQ 5 in the system BIOS, this option is not available.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future BIOS revision.

10. Fan Tach Header Control Not Supported

PROBLEM: Fan tach header control is not supported on the CA810 as implied by the *CA810 Technical Product Specification*.

IMPLICATION: Users who wish to utilize the fan tach feature of system management will not have this option.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA A09252-300, A09255-300 and later revisions.

11. BIOS Does Not Generate Error When an Unformatted Floppy is in The Floppy Drive During System Boot

PROBLEM: If an unformatted floppy is in the floppy drive during system boot, there will be no error message presented to the user and the system will continue to boot to the operating System.

IMPLICATION: Users who place an unformatted floppy in the floppy drive will not be alerted during boot and the system will continue to boot the operating system.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future BIOS revision.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *CA810 Motherboard Technical Product Specification* (Order Number 733082). All Documentation Changes will be incorporated into a future version of that specification.

1. Change to Description of Supported Memory

Section 1.4, System Memory, includes conflicting information on whether 66 MHz DIMMs are supported. Only 100 MHz DIMMs are supported by the CA810 motherboard. Section 1.4 will be replaced in its entirety as follows:

1.4 System Memory

The motherboard has two DIMM sockets. SDRAM can be installed in one or both sockets. Minimum memory size is 32 MB; maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Due to the video requirements of the CA810 motherboard, minimum memory for the Windows NT* 4.0 operating system is 64 MB.

The motherboard supports memory with the following features:

- 168-pin DIMMs with gold-plated contacts
- 100 MHz unbuffered SDRAM
- Non-ECC (64-bit) memory
- Either Serial Presence Detect (SPD) or non-SPD memory
- 3.3 V memory only

CAUTION

*Because the main system memory is also used as video memory, the motherboard requires 100 MHz SDRAM DIMMs even though the processor front side bus is 66 MHz. It is **highly** recommended that SPD DIMMs be used, since this allows the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.*

The motherboard supports single- or double-sided DIMMs in the following sizes:

DIMM Size	Non-ECC Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB	32 Mbit x 64

NOTE

All memory components and DIMMs used with the CA810 motherboard must comply with the PC SDRAM Unbuffered DIMM Specification. You can access this document through the Internet at:
http://www.intel.com/design/chipsets/memory/index.htm

See Section 6.2 for information about this SDRAM DIMM specification.

2. Refer to Summary Table of Changes

3. Change in Section 4.4, Table 58, Advanced Menu

Boot Settings Configuration in this table will be changed to Boot Settings.

4. Change in Section 4.4.2, Table 60, Peripheral Configuration Submenu

The LAN feature in this table will be changed as follows:

LAN Device	• Disabled • **Enabled (default)**	Enables or disables the optional onboard 10/100 Ethernet.

5. Change in Section 4.6, Table 66, Power Menu

The description for Power Management will be replaced in its entirety as follows:

Enables or disables the APM BIOS power management feature.

The description for Inactivity Timer will be replaced in its entirety as follows:

Specifies the amount of time before the computer enters standby mode, when APM power management is active.

The description for Hard Drive will be replaced in its entirety as follows:

Enables power management for hard disks during standby and suspend modes, when APM power management is active.

The description for Video Power Down will be replaced in its entirety as follows:

Specifies power management for video during standby and suspend modes, when APM power management is active.

6. Change to Description of Manufacturing Options

In section 1.1, feature summary table will be changed as follows:

Manufacturing Options

Audio	Sony/Phillips digital interface format (S/P-DIF) connector
Chassis Intrusion	Support for chassis intrusion detection
Fan Connector	The fan 2 connector is optional
Hardware Monitor Subsystem	• Wired for Management (WfM) compliant (see section 6.2 for compliance level) • Voltage sensor to detect out of range values
Graphics Subsystem	Intel® 82810 DC-100 Graphics/Memory Controller Hub with support for 1 M x 16 (4 MB) display cache
Enhanced Diagnostics	Embedded diagnostics and LEDs that supplement beep codes during POST
LAN Controller	• Intel® 82559 PCI LAN controller with RJ-45 LAN connector • Wake on LAN* technology
Power Management	• Alert on LAN* component