



Pentium® II Processor Identification Information

S-Spec	Core Steppings	CPUID	Speed (MHz) Core/Bus	L2 Size (Kbytes)	TagRAM/Stepping	ECC/Non-ECC	Processor Substrate Revision	Package and Revision	Notes
SL264	C0	0633h	233/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL265	C0	0633h	266/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL268	C0	0633h	233/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL269	C0	0633h	266/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL28K	C0	0633h	233/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 3, 9, 13, 20, 21
SL28L	C0	0633h	266/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 3, 9, 13, 20, 21
SL28R	C0	0633h	300/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2MZ	C0	0633h	300/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 3, 13, 20, 21
SL2HA	C1	0634h	300/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2HC	C1	0634h	266/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2HD	C1	0634h	233/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2HE	C1	0634h	266/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2HF	C1	0634h	233/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 13, 20, 21
SL2QA	C1	0634h	233/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 3, 9, 13, 20, 21
SL2QB	C1	0634h	266/66	512	T6/B0	non-ECC	D	SECC 3.00	1, 2, 3, 9, 13, 20, 21
SL2QC	C1	0634h	300/66	512	T6/B0	ECC	D	SECC 3.00	1, 2, 3, 13, 20, 21
SL2KA	dA0	0650h	333/66	512	T6P/A3	ECC	B1	SECC 3.00	4, 5, 8, 14, (20 or 21)
SL2QF	dA0	0650h	333/66	512	T6P/A3	ECC	B1	SECC 3.00	3, 4, 5, 8, 14
SL2K9	dA0	0650h	266/66	512	T6P/A3	ECC	B1	SECC 3.00	4, 5, 8, 14, 21
SL35V	dA1	0651h	300/66	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 5, 7, 8, 15
SL2QH	dA1	0651h	333/66	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 5, 7, 8, 15
SL2S5	dA1	0651h	333/66	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 5, 7, 8, 15, (20 or 21)



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SL2ZP	dA1	0651h	333/66	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 5, 7, 8, 15, 19, 20
SL2ZQ	dA1	0651h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 5, 7, 8, 15, 19, 20
SL2S6	dA1	0651h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 15, (20 or 21), 22
SL2S7	dA1	0651h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 10, 15, (20 or 21)
SL2SF	dA1	0651h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 15
SL2SH	dA1	0651h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 10, 15
SL2VY	dA1	0651h	300/66	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 15
SL33D	dB0	0652h	266/66	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 5, 7, 8, 15, 20
SL2YK	dB0	0652h	300/66	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 5, 7, 8, 15, 20
SL2WZ	dB0	0652h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 15, 20
SL2YM	dB0	0652h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 10, 15, 20
SL37G	dB0	0652h	400/100	512	T6P-e/A0	ECC	B1	SECC2 OLGA	3, 7, 10, 12, 15, 18
SL2WB	dB0	0652h	450/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 7, 8, 10, 11, 15, 20
SL37H	dB0	0652h	450/100	512	T6P-e/A0	ECC	B1	SECC2 OLGA	3, 4, 7, 8, 10, 15, 18
SL2KE	TdB0	1632h	333/66	512	C6C/A3	ECC	N/A	PGA	4, 7, 8, 12
SL2W7	dB0	0652h	266/66	512	T6P-e/A0	ECC	B1	SECC 2.00	4, 5, 7, 8, 15, 20
SL2W8	dB0	0652h	300/66	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 5, 7, 8, 15, 20
SL2TV	dB0	0652h	333/66	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 5, 7, 8, 15, 20
SL2U3	dB0	0652h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 15, 20
SL2U4	dB0	0652h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 15, 20



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SL2U5	dB0	0652h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 10, 15, 20, 22
SL2U6	dB0	0652h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 10, 15, 20
SL2U7	dB0	0652h	450/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 7, 8, 10, 11, 15, 20
SL356	dB0	0652h	350/100	512	T6P-e/A0	ECC	B1	SECC2 PLGA	4, 7, 8, 10, 15, 16, 20, 22
SL357	dB0	0652h	400/100	512	T6P-e/A0	ECC	B1	SECC2 OLGA	4, 7, 8, 10, 15, 18, 20
SL358	dB0	0652h	450/100	512	T6P-e/A0	ECC	B1	SECC2 OLGA	4, 7, 8, 10, 15, 17, 18, 20
SL37F	dB0	0652h	350/100	512	T6P-e/A0	ECC	B1	SECC2 PLGA	3, 4, 7, 8, 10, 15, 16, 20
SL3FN	dB0	0652h	350/100	512	T6P-e/0	ECC	B1	SECC2 OLGA	4, 7, 8, 10, 15, 18, 20
SL3EE	dB0	0652h	400/100	512	T6P-e/0	ECC	B1	SECC2 PLGA	1, 7, 8, 15, 16, 20, 22
SL3F9	dB0	0652h	400/100	512	T6Pe/A0	ECC	B1	SECC2 PLGA	3, 4, 7, 8, 10, 15, 16
SL38M	dB1	0653h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 10, 15, 20
SL38N	dB1	0653h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	3, 4, 6, 7, 8, 10, 15, 20
SL36U	dB1	0653h	350/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 10, 15, 20
SL38Z	dB1	0653h	400/100	512	T6P-e/A0	ECC	B1	SECC 3.00	4, 6, 7, 8, 10, 15, 20
SL3D5	dB1	0653h	400/100	512	T6P-e/A0	ECC	B1	SECC2 OLGA	3, 7, 8, 10, 15, 18
SL3J2	dB1	0653h	350/100	512	T6P-e/A0	ECC	B1	SECC2 PLGA	4, 7, 8, 10, 15, 16, 22

NOTES:

1. VCC\_CORE is specified for 2.8 V +100/-70 mV for all Pentium® II processors.
2. TPLATE is specified for 5° C – 75° C for these Pentium II processors with S.E.C. cartridge packages except for s-specs SL28R , SL2HA, SL2MZ, and SL2QC which have a TPLATE specification for 5° C – 72° C.
3. This is a boxed Pentium II processor with an attached fan heatsink.
4. VCCCORE is specified for 2.0 V +100/-70 mV for these Pentium II processors.
5. TPLATE is specified for 5° C – 65° C for these Pentium II processors.
6. TPLATE is specified for 5° C – 75° C with ETP (extended thermal plate) for these Pentium II processors.



7. Cacheable address space supports up to 4 Gbytes for these Pentium II processors.
8. These processors will not shut down automatically on THERMTRIP#.
9. These boxed processors may have packaging which incorrectly indicates ECC support in the L2 cache.
10. These processors are affected by Erratum A56.
11. T<sub>PLATE</sub> is specified for 5° C – 70° C with ETP (extended thermal plate) for these Pentium II processors.
12. This is a boxed Pentium II OverDrive® processor with an attached fan heatsink.
13. This TagRAM notation is equivalent to part number 82459AB.
14. This TagRAM notation is equivalent to part number 82459AC.
15. This TagRAM notation is equivalent to part number 82459AD.
16. T<sub>CASE (MAX)</sub> is specified as 80° C for these Pentium II processors.
17. These processors are affected by Erratum A67.
18. T<sub>JUNCTION (MAX)</sub> is specified as 90° C for these Pentium II processors.
19. These processors require a dual reset BIOS.
20. These parts will only operate at the specified core to bus frequency ratio at which they were manufactured and tested. It is not necessary to configure the core frequency ratios by using the A20M#, IGNEE#, LINT[1]/NMI and LINT[0]/INTR pins during RESET.
21. These parts require the inputs from A20M#, IGNEE#, LINT[1]/NMI and LINT[0]/INTR pins during RESET to set the correct core to bus frequency ratio.
22. This part also ships as a boxed processor with an attached fan heatsink.