SSH4 BIOS Release Notes

Enterprise Platform & Services Marketing

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DATE: Nov. 5, 2004
TO: Intel **SSH4** customers
SUBJECT: Intel® SSH4 BIOS Release Notes
P15 Build 99:

About This Release

Build # : 0099
Build Stamp : SSH40.86B.0099.P15.0411051004
Build Date : Nov. 5, 2004

BIOS Components/Contents

Processor stepping(s) supported: Intel® Xeon™ processors
Microcode update versions:

CPUID	Code Name	Microcode update ID
0F11h	MP Foster C0	0A (MU2F110A)
0F22h	Gallatin A0	05 (MU2F2205)
0F25h	Gallatin B1	2A (MU2F252A)
0F26h	Gallatin C0	10 (MU2F2610)

System hardware configurations supported: SSH4 Beta 2 / Silver / Gold board

System FW Requirements/Revisions

BMC FW : 9 or later revision

Important Installation Notes

NOTICE1:
Systems with any BIOS revision earlier than Build 59, must first update to Build 59 or later using Phoenix Phlash (i. e. BIOS59PH.ZIP). Once the system has been updated to Build 59 or later, it can be updated to later releases using Phoenix Phlash or Intel iFlash.

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NOTICE2:
There is a limitation when BIOS is updated on windows 2003 system using BIOS P08 or before. If you update BIOS to BIOS Build 0086 or later on your Windows 2003 system, must first delete the IBM Active PCI device driver from your system, and then please update BIOS. At the end, reinstall the IBM Active PCI device driver to your system.

1. Updating Boot Block

Boot Block update required: No

2. Upgrading BMC

Note: BMC must be updated with BMC09 or later before upgrading the BIOS.
The new sensor number specification was supported from BIOS 0038 and BMC 09. So, BIOS and BMC FW can't handle some sensors correctly except for the combination of revision number designated by BIOS or FW release notes.
In updating function, they do not have any limitations each other about the revision number.

3. Upgrading SDR

The FRU SDR must be updated to AC1 or later before updating the BIOS.
The new sensor number specification was supported from BIOS 0038. So, SDR also must support it , AC1 or later are supporting it.
In updating function, they do not have any limitations each other about the revision number.
Please read the release notes for the FRUSDR package prior to performing this update.

4. Creating a Bootable Floppy

- You must use a DOS system to create the bootable floppy.
- Place an unformatted floppy diskette in the floppy drive and format the floppy using the /S option. Example: "format a: /s"
- Alternatively, place a formatted floppy in the floppy drive and use the "sys" command. Example: "sys a:"

5. Making a BIOS Upgrade Floppy

- Follow the instructions (above) for creating a bootable floppy to create a bootable floppy diskette.
- Insert the bootable floppy into drive a:.
- Extract the contents of the BIOS zip file onto the bootable floppy.

6. Upgrading a BIOS

- Note the settings of the SETUP parameters. Enter SETUP by hitting the F2 key during boot up. Write down the settings for each of parameters. At the end of the BIOS update process you should set the parameters to default values by hitting the F9 key, and then re-enter these values you have written down.
- Place the bootable floppy containing the BIOS into drive a: of the system that you want to upgrade and boot the system while the floppy diskette is in the drive.
- Boot the system from the floppy disk drive. Automatically, system BIOS is updated.
- This update processing takes 3 to 4 minutes. Never turn off the system during the update processing. The following message appears when the update processing is finished.

Flash memory has been successfully programmed
PRESS ANY KEY TO RESTART THE SYSTEM

If the system does not restart,
TURN THE POWER OFF, THEN ON

- Remove the floppy and Press the Enter key to reboot the system.
- Check to make sure the BIOS version is the new version as the system reboots.
- Enter Setup by pressing the F2 key during boot up. Once in Setup, press the F9 to set the parameters back to default values. Re-enter the values you wrote down at the beginning of this process. If you do not set the CMOS values back to defaults using the F9 key, the system may function erratically.

Note: You may encounter a CMOS Checksum error or other problem after reboot. Try shutting down the system and booting up again. CMOS checksum errors require that you enter Setup, check your settings, save your settings, and exit Setup.

7. Performing a BIOS Recovery

- Unzip the crisis zip file to a temp directory on a system
- Insert a blank, formatted floppy in A and run CRISDISK.BAT. Follow the instructions on the screen thoroughly. This makes the diskette.
- With the system powered off, insert this diskette.
- Place a jumper on BIOS Recovery (Alpha/Beta board: pins 9-10, Silver or later boards: pins 3-4) of the BIOS jumper block (see jumper diagram to locate the jumper block).
- Place a jumper on header JP5 to disable the FRB3 timer if you update BIOS from Build 1012, 0012 or 0006.
- Power up the system. System will beep intermittently for about 2 minutes.
- When it stops beeping, power the system off, remove the jumper, remove the floppy diskette and power the system back up.
- Make sure you clear CMOS as well after this is all done.

Known Issues/Workarounds

1. You can not update the system that has former version BIOSes using the iFlash utility. Because the Data area mismatch is detected by changing BIOS area in this version. You must first update your systems to 0044 using the Phlash utility.

2. BIOS Build0099 does not support –321 boards which has an AIC7902 A1.

3. Set the FRB3_Disabled Jumper when you update BIOS from Build 1012, 0012 or 0006 by Crisis recovery.

4. This BIOS can use on Power On Refresh system

5. BIOS Build0099 supports both 7899 and 7902 A2 SCSI BIOS as onboard device on same PCID. (7899 BIOS: v2.57S13, 7902 BIOS: 4.10.1)

6. Please select following BIOS setup option according with Hot-Added PCI spec.

   Setup Item: Advanced>>PCI Configuration>>Hot-Plug PCI Control

   >>Reserving memory space for PhP

   Option:

   [Disabled] = (Default)

   Memory hole for empty slots are not reserved.

   [Minimum] = 6MB.

   Memory hole for each empty slots are reserved to 6MB.

   [Middle] = 48MB

   Memory hole for each empty slots are reserved to 48MB.

   [Maximum] =96MB

   Memory hole for each empty slots are reserved to 96MB.

7. Please install the filter driver (ibmhpf.sys/imbhpa.sys) for Windows 2000.

   Note that Windows2000 will detect an Unknown device error in Device manager if these drivers are not installed.

Features added in this release

- None

Issues fixed since last release

Trackers

Tracker#	Title	Note

Change List History

- BIOS Build 0099 [P15]
It's based on Build 0098 [RC32].
(1) Banner was changed for production phase, [P15].

- BIOS Build 0098 [RC32]
It's based on Build 0097 [P14].
(1) Applied the latest Production MU for Gallatin B1/C0 stepping.

- BIOS Build 0097 [P14]
It's based on Build 0096 [RC31].
(1) Applied the latest Production MU for Gallatin B1/C0 stepping.

(2) Banner was changed for production phase, [P14].

- BIOS Build 0096 [RC31]
It's based on Build 0095 [RC30].
(1) Modification for solving the tracker #15378.
Applied BIOS workaround for CMIC autocompensation issue.
[Workaround]
-If CMIC Function 2 register 64h is 7Bh or greater, change register 64 to 77h.
-If CMIC Function 2 register 64h is 7Ah or less, allow to automatically set register 64h.

(2) Modification for solving the tracker #15979.
I/O reservation region of PhP function was extended.

(2) Modification for solving the tracker #15707.
INTERRUPT SOURCE OVERRIDE ENTRY of ACPI table was deleted.

- BIOS Build 0095 [RC30]
It's based on Build 0094 [P13].
(1) Modification for solving the tracker #15657.
Modified the _CRS method of USB device.

(2) Modification for solving the tracker #16186.
Applied the latest Production MU(0D) for Gallatin C0 stepping.

- BIOS Build 0094 [P13]
It's based on Build 0093 [P12].
(1) Applied the latest Production MU for Gallatin B1/C0 stepping.

(2) Enabled Fast-Strings(MSR 1A0h.bit0).

(3) Updated the BIOS Copyright to 2004.

- BIOS Build 0093 [P12]
It's based on Build 0092 [P11].
(1) Modification for solving the tracker #14820.

Applied the latest Production MU for Gallatin C0 stepping.

- BIOS Build 0092 [P11]
It's based on Build 0091 Beta
(1) Banner was changed for production phase, [P11].

- BIOS Build 0091 Beta
It's based on Build 0089 [P10]
(1) Modification for solving the tracker #15013.
-Note that the detecting option ROM error issue isn't fixed by a new BIOS because the bug is only to display wrong messages (Requested 00Kb) when option rom error is detected.

(2) Modification for solving the tracker #15300.
-Supported additional request from Intel. BIOS will display POST messages to indicate sparing/mirroring mode when it is enabled by setup. Please refer to DR15300.

(3) Applied the latest MU for MP Foster C0/Gallatin A0/Gallatin B1-Step.

- BIOS Build 0089 [P10]
It's based on Build 0088 Beta
(1) Removed a MU (MU2F2604) for Gallatin 4M cache.

(2) Banner was changed for production phase, [P10].

- BIOS Build 0088 Beta
It's based on Build 0086 Beta
(1) Modification for solving the tracker #14509.
-Modified a BIOS issue in emulating INT10h Function 13h.

(2) Modification for supporting Sparing/Mirroring memory features.
Note that BMC FW 00.25 or later revisions are needed to support them.

- BIOS Build 0086 Beta
It's based on Build 0083 [P08]
(1) Modification for solving the tracker #14744.
-Added a _HPP method in ASL.
-Modified a _HID method of IBM Active PCI Device so that Filter driver (IBMHPF.SYS) can not be loaded.
NOTICE:
This modification has a limitation when BIOS is updated on windows 2003 system using BIOS P08 or before. If you update BIOS to BIOS Build 0086 or later on your Windows 2003 system, must first delete the IBM Active PCI device driver from your system, and then please update BIOS. At the end, reinstall the IBM Active PCI device driver to your system.

(2) Modification for solving the tracker #14772.
-NUMLOCK is forcibly disabled when a keyboard is not attached.

(3) Modification for solving the tracker #14799.
-Modified a function for detecting miss matched processors.

(4) Modification for solving the tracker #14820.
-Applied Micro code M02F26041 (MU2F2604) for Gallatin 4M Cache.

(5) Modified Multi Language messages for PnP POST error messages.

- BIOS Build 0083 [P08]
It's based on Build 0082 Beta.
(1) Modification for solving the tracker #13687.
-Applied the latest MU (MU2F250E) for Gallatin B1-Step.

(2) Banner was changed for production phase, [P08].

- BIOS Build 0082 Beta
It's based on Build 0081 Beta
Modification for solving the tracker #13687.
-Applied the latest MU (MU2F250B) for Gallatin B1-Step.

- BIOS Build 0081 Beta
It's based on Build 0080 [P07].
(1) Modification for solving the tracker #11923.
Applied the BIOS recommendation on GCHE Newsletter No.15.
Alert on PLL losing lock is disabled.

(2) Modification for solving the tracker #13091.
Supported PME# signals from Slot#3 and Slot#4.
BIOS checks the FRU on the baseboard. If the Board Part Number bytes is A60891-704 or later, BIOS will handle PME# from Slot 3-4.

(3) Modification for solving the tracker #13687.
-Applied the latest MU (MU2F2504) for Gallatin B1-Step.
-Modified the function for detecting Unsupported CPU Error so that the error is not detected if Gallatin B1-step processors are populated.

(4) Modification for solving the tracker #14041.
Provided the BIOS proc frequency menu if BIOS detects unlocked processors.
Note that this BIOS proc frequency menu is not supported on Production BIOS.

(5) Modification for solving the tracker #14087.
Changed the Refresh Delay value. ServerWorks recommends that this value is set to RCR-2 (RCR is Bus=0, Device=0, Function=0, Offset=79h). BIOS applied it.

(6) Modification for solving the tracker #14089.
Enabled the optimal timing between writes and reads.
(Bus=0, Device=0, Function=0, Offset=9Bh, bit5: 1b).

(7) Modification for solving the tracker #14099.
Changed the Processor Family in type4 structure to B5h from B3h.
The B3h indicates "Intel(R) Xeon(TM) processor" as Processor Brand. It should be B5h that indicates "Intel(R) Xeon(TM) processor MP".

(8) Modification for solving the tracker #14118.
Updated the BIOS Copyright to 2003.

(9) Modification for supporting Windows 2003.
Added the BMC resource information to ASL to pass the HCT11.1a.

- BIOS Build 0080 [P07]
It's based on Build 0079 Beta.
Banner was changed for production phase, [P07].

- BIOS Build 0079 Beta
It's based on Build 0077 [P06].
Modification for solving the tracker #13830.
Modified a handling of VGA refresh during int16h(Keyboard services) process.

- BIOS Build 0077 [P06]
It's based on Build 0076 Beta.
Banner was changed for production phase, [P06].

- BIOS Build 0076 Beta
It's based on Build 0075 Beta.
(1) Modification for solving the tracker #13185.
Modified a semaphore process to check in/out SMM to fix SMI failure issue with 8 logical processors.

(2) Modification for solving the tracker #13196.
Removed a "WINCRIS.EXE" from the recovery zip file.

- BIOS Build 0075 Beta
This is based on Build 0074 [P05].
(1) Modification for solving the tracker #12160.
BIOS configures 08Bh to the slew rate in CIOB if CPU board is Fab6.

(2) Modification for solving the tracker #12195.
BIOS checks if a Gallatin family processor is installed in the system and if so, reads the FRU on the SSH4 CPU board and if the rev is –5xx or earlier displays the unsupported processor message and logs POST Error SEL.

(3) Modification for solving the tracker #13042.
Modified a function of "Empty Bus Default Speed" in BIOS Setup.
The Empty Bus Default Speed option becomes to be able to change the default speed for empty slot and have it written to CMOS even if a card is populated in the slot.

(4) Modification for solving the tracker #13078.
Added PCI-X66 and PCI-X100 selections to "Empty Bus Default Speed" in BIOS Setup if the motherboard is Fab7.

- BIOS Build 0074 [P05]
It's based on Build 0073 Beta.
(1) Modification for solving the tracker #12344.
Modified a function to detect a PCI initialization Error if PCI option ROM area is insufficient.

(2) Modification for solving the tracker #12244.
Applied the latest MU (MU2F1108) for MP Foster C0-Step.

(3) Modification for solving the tracker #12752.
Applied the latest BIOS for onboard AIC7902 (v4.10.1)

- BIOS Build 0073 Beta
It's based on Build 0071 [P04].
(1) Modification for solving the tracker #11378.
Modified configuration for SuperIO.

(2) Modification for solving the tracker #11655.
Changed the "Supervisor" string to "Administrator" for Intel Shasta.

(3) Modification for solving the tracker #12344.
Added new function to detect a PCI initialization Error if PCI option ROM area is insufficient.

(4) Modification for solving the tracker #12547.
Modified how to use the conventional memory when serial and LAN redirection are enabled.

(5) Modification for solving the tracker #12846.
Applied the workaround for PCI Hot Plug Controller's issue.

(6) Modification for solving the tracker #12852.
Changed processor's messages in POST.

(7) Modification for solving the Dodson's DR9902.
Title: Dodson hangs during POST with Adaptec ASR-2100, video corruption
Modified INT10h function 11h.

(8) Modification for solving the Hodges's DR9729.
Title: Option ROM characters are blue
Modified INT10h function09h.

(9) Modification for solving the Hodges's DR12485.
Title: Divide by Zero overflow error on FRU update w/c1 step CPU
Modified INT15h function 0DA92h.

(10) Modification for solving the Hodges's DR12570.
Title: User Binary update causes failures during next BIOS post
Modified int19h path so that SSU can be booted if User Binary updated.

- BIOS Build 0071 [P04]
It's based on Build 0070 beta.
Banner was changed for production phase, [P04].

- BIOS Build 0070 Beta
It's based on Build 0069 [P03].
(1) Modification for solving the tracker #11725.

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BIOS uses the CPUID instruction for displaying POST messages and SMBIOS Type4. Added a modification that BIOS will recognize as the Brand ID 0Bh even if BIOS gets Brand ID 0Eh.

(2) Modification for solving the tracker #11889.
Modified ASL to reduce its size.

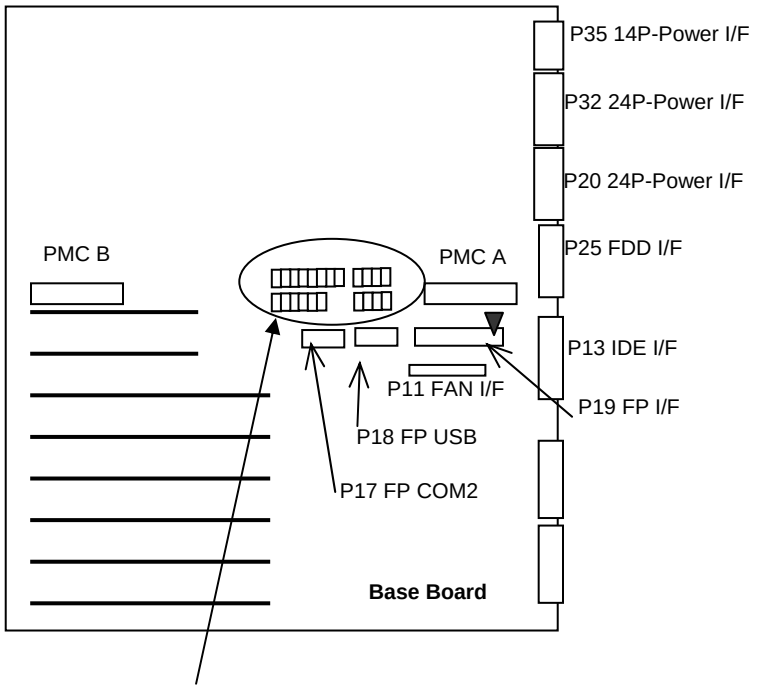
(3) Modification for solving the tracker #11966.
System BIOS size is reduced by 6KB in POST 98h. So the Upper limit address of Option ROM size when POST 98h phase becomes 0E1800h-1.
And the Legacy USB code was moved to near EBDA from Option ROM area.

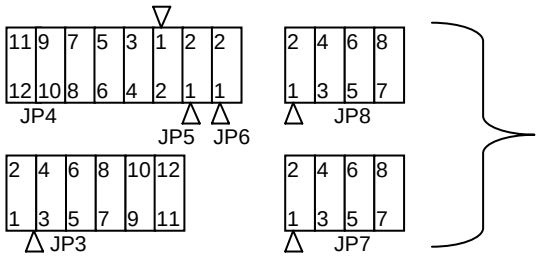
(4) Modification for solving the tracker #12191.
Modified the table of int15 0E820h.

(5) Modification for solving the tracker #12269.
Modified strings for processors.

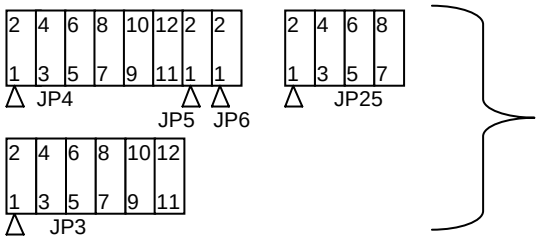
Helpful Reference Material

< Shasta Base Board Block diagram >





For Alpha/Beta Base Board Jumper Layout



For Silver Base Board Jumper Layout

G7FTW Jumper（Shasta Alpha Base Board）

Location	Function	Pin description	
8H(JP3)	Clock ratio	Short/Open=Low/High 1-2:INTR 3-4:NMI 5-6:IGNNE 7-8:A20M 9-10:unused 11-12:unused	
8H1(JP4)		Short＝Enable 1-2:CMOS CLEAR 3-4:Password Disable 5-6:inspection mode1 (ignore voltage observation) 7-8:inspection mode2 (high speed) 9-10:BIOS Recovery 11-12:dummy(default)	
8H11(JP5)	FRB3 stop	1-2:short=FRB timer disable (Default = open)	
8H12(JP6)	BMC FRC update	1-2:short=Update disable	
8H8(JP7)	Front cover CI	1-2:Logging & power-off enable 3-4:Power off enable 5-6:Logging enable 7-8:Disable(Default)	
8H9(JP8)	Side cover CI	1-2:Logging & power-off enable 3-4:Power off enable 5-6:Logging enable 7-8:Disable(Default)	
8J8(JP9)	COM2	1-2:short DSR DCD connect	
8J16(JP10)	COM2	1-2:short DSR connect	
10H(JP11)	CSB5 GEVENT11	1-2:short=High after PCI reset (Default＝open)	
12L9(JP12)	Write enable for BIOS Boot block area	1-2:short 12V input to RESET pin#12	
13H(JP13)	Power switch	1-2:short=power on	
13H3(JP14)	RESET switch	1-2:short=reset	No assy
14G9(JP15)	Expansion BMC Flash memory Enable	1-2:short=Enable (for debugging) 2-3:short=normal	
14H1(JP16)	Write enable for BMC Boot block area	1-2:short 12V input to RESET pin#12	
16M7(JP17)	X-bus debug port		
16N(JP18)	X-bus debug port		

G7GAN Jumper（Shasta Beta Base Board）

Location	Function	Pin description	
8H(JP3)	Clock ratio	Short/Open=Low/High 1-2:INTR 3-4:NMI 5-6:IGNNE 7-8:A20M	**Can not use!**
	Write enable for BMC Boot block area	9-10:short 12V input to RESET pin#12	
	Write enable for BIOS Boot block area	11-12:short 12V input to RESET pin#12	
8H1(JP4)		Short＝Enable 1-2:CMOS CLEAR 3-4:Password Disable 5-6:inspection mode1 (ignore voltage observation) 7-8:inspection mode2 (high speed) 9-10:BIOS Recovery 11-12:dummy(default)	
8H11(JP5)	FRB3 stop	1-2:short=FRB timer disable (Default = open)	
8H12(JP6)	BMC FRC update	1-2:short=Update disable	
8H8(JP7)	Front cover CI	1-2:Logging & power-off enable 3-4:Power off enable 5-6:Logging enable 7-8:Disable(Default)	
8H9(JP8)	Side cover CI	1-2:Logging & power-off enable 3-4:Power off enable 5-6:Logging enable 7-8:Disable(Default)	
8J8(JP9)	COM2	1-2:short DSR DCD connect	
8J16(JP10)	COM2	1-2:short DSR connect	
10H(JP11)	CSB5 GEVENT11	1-2:short=High after PCI reset (Default＝open)	
13H(JP13)	Power switch	1-2:short=power on	No assy
13H3(JP14)	RESET switch	1-2:short=reset	No assy
14G9(JP15)	Expansion BMC Flash memory Enable	1-2:short=Enable (for debugging) 2-3:short=normal	
16M7(JP17)	X-bus debug port		No assy
16N(JP18)	X-bus debug port		No assy

G7GEW Jumper（Shasta Silver Base Board）

Location	Function	Pin description	Default
8H(JP3)	Clock ratio	Short/Open=Low/High 1-2:INTR 3-4:NMI 5-6:IGNNE 7-8:A20M	All Open **Can not use!**
	Write enable for BMC Boot block area	9-10:short 12V input to RESET pin#12	All Open
	Write enable for BIOS Boot block area	11-12:short 12V input to RESET pin#12	
8H1(JP4)		Short＝Enable 1-2: dummy 3-4: BIOS Recovery 5-6: inspection mode2 (high speed) 7-8: inspection mode1 (ignore voltage observation) 9-10: Password Disable 11-12: CMOS CLEAR	1-2:Short
8H11(JP5)	FRB3 stop	1-2:short=FRB3 disable	Open
8H12(JP6)	BMC FRC update	1-2:short= BMC force update	Open
8J12(JP25)	COM2	1-2:DSR – DSR connect 3-4:DSR – DCD connect 5-6:DCD – DCD connect 7-8:dummy	(Di2/Cab3Front) 1-2,3-4,7-8:Short (Cab3Rear) 1-2,5-6,7-8:Short