

# SR870BN4 BIOS Release Notes



## Enterprise Platform & Services Marketing

• Intel Corporation • 2800 Center Drive • DuPont, WA 98327

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**DATE:** September 26, 2006  
**TO:** Intel® SR870BN4 customers  
**SUBJECT:** Intel® SR870BN4 BIOS Release Notes  
Production Release 3.0 Build # 1001

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### About This Release

**Release #** : 1001.P03\* (Itanium 2 Processor with up to 9M L3 cache PR3.0 BIOS)  
**Build Stamp** : S870BN4A.86B.1001.P03.0606130958  
**Build Date** : Jun 13, 2006

### BIOS Components/Contents

**PAL Ver.** : 2.20\*  
**SAL-A / SAL-B Ver.** : 3.0/3.0 (SAL3.20 spec update changes)  
**EFI Spec. Ver.** : 1.10.14.62  
**FPSWA Ver.** : 1.18  
**SCSI BIOS Ver. (QL12160)** : 7.30  
**SCSI BIOS Ver. (LSI1030)** : 01.03.10  
**ATI BIOS** : 0101145700000112  
(\* indicates new for this release)

**Processor stepping(s) supported:** Intel® Itanium® 2 Processors with up to 9MB L3 Cache-A1, A2 stepping

**System hardware configurations supported:** Production Released systems

### System FW Requirements/Revisions

**BMC FW** : BMC35\*  
**FRU/SDR** : SDR21  
**HSC FW** : HSC15

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## Important Installation Notes

### USE LATEST VERSION OF IFLASH64.EFI

To eliminate the chance of flashing an incompatible BIOS binary, please use IFLASH64.efi Version 1.02 or greater with P04. Starting with Version 1.02, Iflash64.efi is capable of verifying that the selected BIOS binary is compatible with the system's Processors type, by matching the Processor's CPU ID. If an incapability is detected, then an error message is displayed. Refer IFLASH64.EFI Ver1.02 Release notes for details. Note that the IFLASH64.efi ver 1.02 is not backward compatible with RC3 BIOS or any of the previous releases, in which case the older version of IFLASH64.efi should be used.

### Other instructions:

1. CLEAR CMOS! after updating to this BIOS.
2. Preferably clear the Processor history, by going to the Setup and issuing a Re-arm.
3. Beta3 and greater Bios will detect mismatched DIMMs and incorrect SPD data on DIMMs. Check and replace DIMMs with incorrect SPD data. A faulty DIMM in any row, will cause subject row to be mapped out. In case of systems with only single Row populated, a bad DIMM will prevent it from booting, since no Memory is detected because of the faulty Row.
4. Refer to the user notes below for flash update requirements.
5. See NOTE below for flash upgrade and jumper definitions
6. BIOS BETA3 and greater allows the BMC to program the Core-Ratio for the Processor speed. BMC8 or greater is also required for this functionality. The Core Ratio jumpers on the CPU board at location J8C2 override the auto programming of the Core-Ratio. If jumpers are installed at location J8C2, they can be removed after updating to BIOS RC1 or greater and BMC 11.

## Known Issues / Workarounds

- Service Partition testing requires RELEASE 2.2 BUILD 3 of Service Partition or newer.
- .Net installation (3621 and 3642 builds) hangs in the menu generated after pressing <F6> or <F2> key during installation. This issue has been fixed in the setup loader of build 3652 or higher.
- PXE installation requires .Net build 3652 or greater.
- SOL (Serial on LAN) feature requires BMC07 or greater and pre-Beta hardware
- FRB feature requires BMC07 or greater support.
- Total memory and configured memory messages are not displayed, in case the SEEPROM behind MRHD is not functional.

## Features added in this release

- None

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## Issues Fixed

### Changes in PR3.0

- ASSERT FAILED Error when copy attached file using USB FDD
- SMBIOS cache entries present and enabled for empty proc sockets
- SR870BN4 BIOS not setting LastBlock for DVD block device in EFI block IO protocol
- skipping the INIT Dump Work around
- PAL 2.20 related changes
- Video is displayed thru add-in PCI video card in mfg. mode.

### Changes in PR2.4

- EBC fix for Emulex, Qlogic EFI configuration utility hang issue
- "Proc speed mismatch" error occurs with other errors.
- SMBIOS type 11 (OEM String) not properly terminated, has garbage characters.
- SAL to OS handoff does not set psr.ac,psr.mfh,psr.mfl as per SAL spec
- Different speed DIMM do not cause mismatch
- Lexar 256MB USB2.0 Keyfob does not work in EFI
- Duplication keyboard instructions for "Enter" in BIOS Setup.
- Extraneous BIOS Setup keyboard instructions in Processor Info sub-menus
- Missing keyboard instructions for right arrow key in BIOS Setup

### Changes in PR2.3

- PAL 2.14 fixes erratum #108 & #109 in PAL 2.10
- Cannot install/boot windows on Emulex LP9802 SAN
- Intermittent boot issues or mapped out rows using 1GB and 4GB DIMMs
- BIOS build 894 RC1.3 sees phantom legacy keyboard

### Changes in PR2.1

- PAL 2.10 change in the PAL\_VERSION pal proc and PAL\_CACHE proc to fix errors

### Changes in PR2.0

- PAL 2.04 to support Itanium® 2 Processors with up to 9MB of L3 cache H6 stepping
- SMBIOS implementation reports memory size 0 for all modules
- SAL PAL shadow base alignment to 1MB boundary in SAL to fix Windows RTM page boundary issue
- PR 7.0 BIOS fails EFI\_MTA CPU64 Branch Regs test
- Processor Retest fails if you enable clear SEL and Proc Retest at same time in BIOS.

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- SAL misfunctioning towards INIT interrupt management
- SAL - 3.2 SPEC change
- SAL init handler checksum fix
- SAL cache flush procedure modified to handle bigger cache size
- Some USB keyfobs do not work in EFI

### Changes in PR1.3

- SMBIOS table CPU max Speed incorrect
- SMBIOS table type 16 max memory wrong

### Changes in PR1.2

- Error running some EFI shell scripts: "Cannot read from file - Device Error"

## Helpful Reference Material

- *Intel® Server System SR870BN4 Product Guide*

## BIOS Recovery Instructions

To recover the SR870BN4 platform BIOS follow the procedure outlined below:

### Package Contents:

This package contains the BIOS Recovery file S870BN4C.REC used for recovering the system to BIOS 1001.P03. Instructions on using Recovery are described below.

### Getting Started:

Copy the S870BN4C.rec file to a blank LS-240 diskette from a Win32 system. Alternatively, the S870BN4C.rec file may be burned to a CDROM using the El Torito format.

### BIOS Recovery Procedure:

1. With the system switched off and AC power disconnected:
2. Place I/O Riser board jumper switch #1 to the ON position for BIOS recovery
3. Insert the LS-240 diskette or CDROM containing ONLY the file S870BN4C.REC
4. Reconnect the AC power and switch server power on.
5. LS-240 diskette/CDROM activity will start and one full beep is heard (start load SR870BN4C.REC from disk to memory).
6. Wait two minutes. No indication of LS-240/CDROM activity will be seen until two full beeps are heard that indicate the BIOS recovery has completed successfully
7. Remove the LS-240 recovery diskette or CDROM, switch system power off, and disconnect AC power.
8. Replace I/O Riser jumper switch #1 to the OFF position
9. Reconnect AC power and switch the system on.
10. When the system reboots, go into BIOS setup by hitting 'F2' function key.

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11. Tab to the 'Exit' menu. Select 'Load Setup defaults'. Press 'yes' to 'Load Setup Defaults'?
12. Make any changes that you need to do in setup. Press F10 to save and exit.
13. System will automatically reboot to EFI.

### **Verification of State:**

Determine your BIOS version. Read the version in the BIOS banner string.

### **Final Configuration:**

After the update, the following should be the configuration of the system.

S870BN4A.86B.1001.P03

### **Safety Notice**

THE INTERNAL WORKINGS OF OEM UNITS CARRY HIGH STANDBY VOLTAGES DESPITE BEING POWERED DOWN BY FRONT PANEL. USERS SHOULD UNPLUG BOTH POWER CORDS TO THE UNIT BEFORE ACCESSING THE SYSTEM OR REMOVING ANY BOARDS.