



REALTEK

ALC269
(ALC269Q-GR, ALC269QSRS-GR)

HIGH DEFINITION AUDIO CODEC WITH EMBEDDED CLASS-D SPEAKER AMPLIFIER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC269 codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/04/15	First Release
1.1	2008/04/25	Revised Figure 1 Block Diagram, page 5. Revised Table 83 Analog Performance, page 64 (DAC/ADC Full-Scale Input Voltage).
1.2	2008/12/24	Update analog performance in section 9.3, page 64.

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1. General Description

The ALC269 is a High Definition Audio Codec that integrates a 2+2-channel DAC, a 4-channel ADC, and a Class-D Speaker Amplifier.

The 2+2-channel DAC supports two independent stereo sound outputs simultaneously. The 4-channel ADC integrates two stereo and independent analog sound inputs (multiple streaming).

The ALC269 incorporates Realtek converter technology to achieve a 98dB dynamic range playback quality and a 98dB dynamic range recording quality. It meets the current WLP3.10 (Windows Logo Program) and future WLP requirements that become effective from 01 June 2008.

The ALC269 also supports stereo digital microphone channels (microphone array) with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology simultaneously, significantly improving voice quality for PC VoIP applications.

As well as basic audio functions, the ALC269 has two independent S/PDIF outputs; one could be used to connect a PC to high-quality consumer electronic products such as digital decoders and speakers, the other could provide a dedicated digital output to a HDMI transmitter (common in high end PCs).

There are three integrated power amplifiers. The first is a linear headphone amplifier at port C. The second headphone amplifier at port A removes the need for external DC blocking capacitors, eliminating pop noise caused by these capacitors. The third is an integrated stereo Class-D amplifier to directly drive a mini-speaker. The Class-D amplifier is designed to drive speakers with as low as 4Ω impedance. Its maximum output power is 2.3W per channel at 5V power supply. The advantage of an integrated Class-D amplifier in the ALC269 is high efficiency with low power consumption.

The ALC269 integrates five hardware equalizer bands composed of one low-pass filter, one high-pass filter, and three band-pass filters to compensate for mini-speaker frequency response. All the equalizer filters are programmable via the BIOS, allowing the equalizer to function without the need to customize the audio driver.

The ALC269 conforms to Intel's Audio Codec low power state white paper and is ECR compliant.

Note: ALC269 version differences are listed in section 12 Ordering Information, page 71.

2. Features

2.1. *Hardware Features*

- 98dB Signal-to-Noise Ratio (A-weighting) for DAC output
- 98dB Signal-to-Noise Ration (A-weighting) for ADC input
- Meets WLP (Windows Logo Program) 3.10 and future WLP requirements that become effective from 01 June 2008
- 2+2-channel DAC supports 16/20/24-bit PCM format for independent two stereo channel audio playback
- 4-channel ADC supports 16/20/24-bit PCM format for independent two stereo channel audio inputs
- All DACs supports 44.1/48/96/192kHz sample rate
- All ADCs support 44.1/48/96kHz sample rate
- S/PDIF-OUT support 16/20/24-bit format and 32/44.1/48/88.2/96/192kHz rate
- Supports MONO line level output
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.2V/4.2V VREFOUT as bias voltage for analog microphone input
- Two jack detection pins each designed to detect up to 4 jacks
- 1dB resolution of input and output volume control
- Programmable +10/+20/+30dB boost gain for analog microphone input
- Built-in headphone amplifiers for port-A and port-C.
- 2 GPIOs are supported for customized applications (pin shared with digital microphone interface)
- EAPD (External Amplifier Power Down) is supported (pin shared with secondary S/PDIF-OUT)
- Supports Anti-pop mode when analog power AVDD is on and digital power is off
- Power support: 3.3V digital core power; 1.5V~3.3V digital IO power for HDA link; 3.3V~5.0V analog power; 3.3V~5.0V power stage voltage
- Enhanced power management features

- Secondary S/PDIF-OUT supports 16/20/24-bit format and 32k/44.1k/48k/88.2k/96k/192kHz rate
- Supports stereo digital microphone input
- Programmable boost gain and volume control for digital microphone input
- Headphone amplifier for port-A does not require DC blocking capacitors
- Stereo Bridge-Tied Load Class-D amplifier at port-D has 2Watt (rms)/4 Ω per channel output
- Short circuit and thermal overload protection for Class-D amplifier
- Supports digital PWM output at port-D which system integrator can easily connect the output to external power amplifier receives digital audio stream
- Five band hardware equalizer designed for BTL output (port-D) to compensate for frequency response while driving the mini-speaker
- Intel low power ECR compliant: supports power status control, jack detection, and wake-up event in D3 mode
- 48-pin QFN 'Green' package

2.2. Software Features

- Compatible with Windows Logo Program 3.10 and future requirements that become effective from 01 June 2008
- WaveRT-based audio function driver for Windows Vista
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio (Windows XP only)
- Emulation of 26 sound environments to enhance gaming experience
- Multi-band software equalizer and tools
- Voice Cancellation and Key Shifting in Karaoke mode

- Dynamic range control (expander, compressor, and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Provides 10-foot GUI for Windows Media Center
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Dolby[®] PCEE program[™] (optional software feature)
- SRS[®] TrueSurround HD (optional software feature)
- Fortemedia[®] SAM[™] technology for voice processing (Beam Forming and Acoustic Echo Cancellation) (optional software feature)

3. System Applications

- Windows Vista premium desktop and laptop PCs
- Information appliances (IA) with High Definition Audio Controller

4. Block Diagram

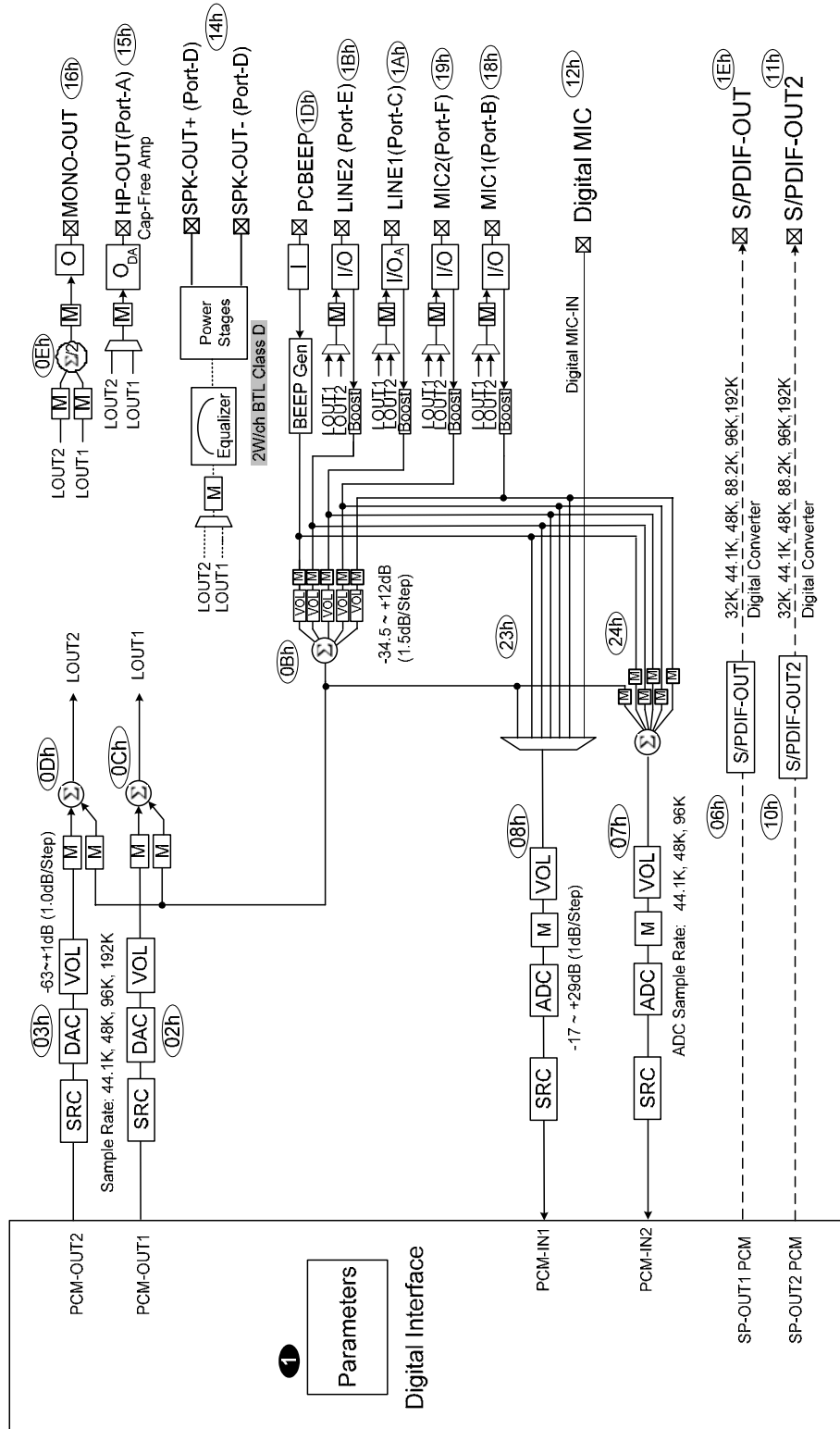


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin widgets NID=18h, 19h, 1Ah, and 1Bh are re-tasking IO supporting input units. NID=15h and 1Ah support amplifier units.

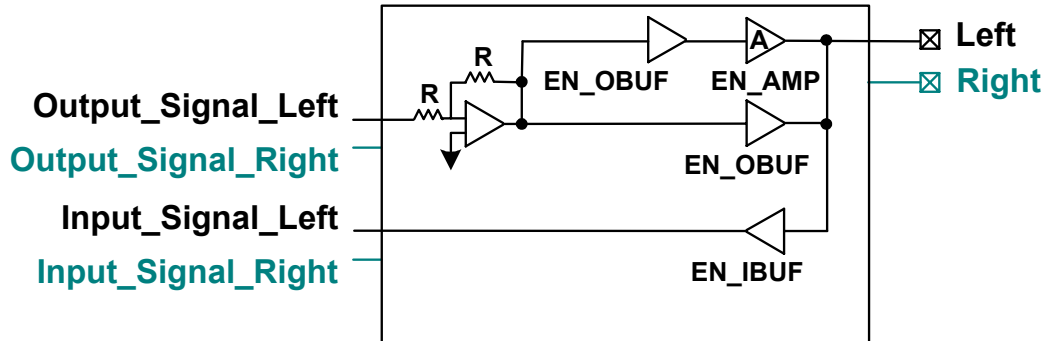


Figure 2. Analog Input/Output Unit

5. Pin Assignments

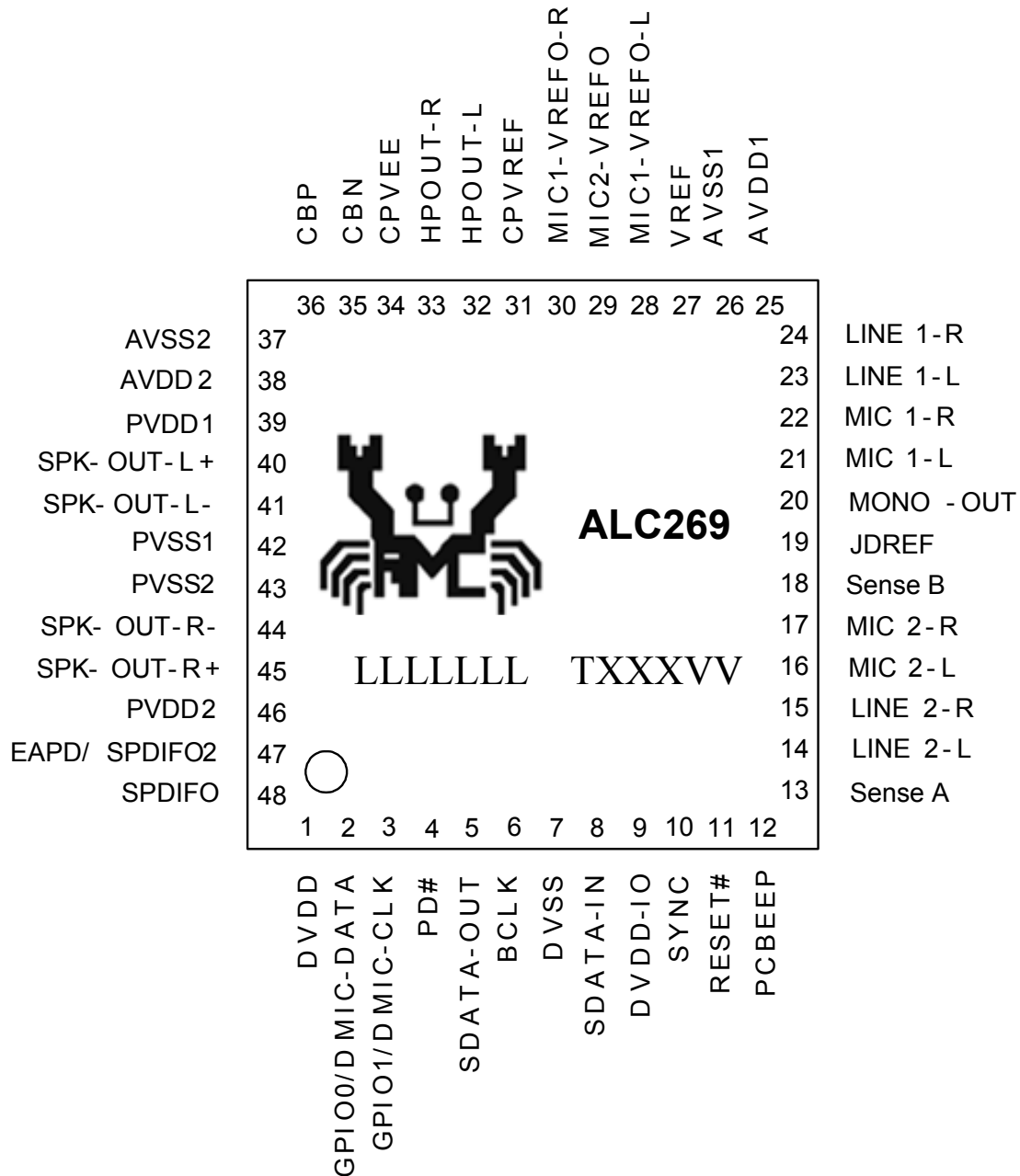


Figure 3. Pin Assignments - ALC269 (QFN-48)

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'VV'.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
RESET#	I	11	H/W Reset Control	$V_i=0.5*DVDD$
SYNC	I	10	Sample Sync (48kHz)	$V_i=0.5*DVDD$
BCLK	I	6	24MHz Bit Clock Input	$V_i=0.5*DVDD$
SDATA-OUT	I	5	Serial TDM Data Input	$V_i=0.5*DVDD$
SDATA-IN	O	8	Serial TDM Data Output	$V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD$
EAPD / SPDIFO2	O	47	Signal to power down ext. amp Secondary S/PDIF output	Output to mute/un-mute external amplifier Output has 12 mA@75Ω driving capability.
SPDIFO	O	48	S/PDIF Output	Output has 12mA@75Ω driving capability.
GPIO0 / DMIC-DATA	IO	2	General Purpose Input/Output 0 Data input from digital MIC1&2	Input $V_t=(1/2)*DVDD$, output $V_{OH}=DVDD$, $V_{OL}=DVSS$, internal pulled up by 50KΩ
GPIO1 / DMIC-CLK	IO	3	General Purpose Input/Output 1 Clock output for digital MIC	Input $V_t=(1/2)*DVDD$, output $V_{OH}=DVDD$, $V_{OL}=DVSS$, Default 2.048MHz clock output
PD#	I	4	Low to Power Down Speaker (BTL) Output	Input $V_t=(1/2)*DVDD$, internal pulled up by 50KΩ
				Total: 10 pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
PCBEEP	I	12	External PCBEEP Input	Analog input, 1.6Vrms of full-scale input
LINE2-L	IO	14	2 nd Line Input Left Channel	Analog input/output, default is input (JACK-E)
LINE2-R	IO	15	2 nd Line Input Right Channel	Analog input/output, default is input (JACK-E)
MIC2-L	IO	16	2 nd Stereo Microphone Input Left Channel	Analog input/output, default is input (JACK-F)
MIC2-R	IO	17	2 nd Stereo Microphone Input Right Channel	Analog input/output, default is input (JACK-F)
MONO-OUT	O	20	MONO Output	Analog mono output is summation of (L+R)/2.
MIC1-L	IO	21	1 st Stereo Microphone Input Left Channel	Analog input/output, default is input (JACK-B)
MIC1-R	IO	22	1 st Stereo Microphone Input Right Channel	Analog input/output, default is input (JACK-B)
LINE1-L	IO	23	1 st Line Input Left Channel	Analog input/output, default is input (JACK-C)
LINE1-R	IO	24	1 st Line Input Right Channel	Analog input/output, default is input (JACK-C)
SPK-OUT-L+	O	40	BTL Mode Positive Left Channel	Pulse width modulation output (JACK-D)
SPK-OUT-L-	O	41	BTL Mode Negative Left Channel	Pulse width modulation output (JACK-D)
SPK-OUT-R-	O	44	BTL Mode Negative Right Channel	Pulse width modulation output (JACK-D)
SPK-OUT-R+	O	45	BTL Mode Positive Right Channel	Pulse width modulation output (JACK-D)

Name	Type	Pin	Description	Characteristic Definition
HP-OUT-L	O	32	First Out Left Channel	Analog output (JACK-A)
HP-OUT-R	O	33	First Out Right Channel	Analog output (JACK-A)
Sense A	I	13	Jack Detect Pin L	Resistor (5.1K, 10K, 20K, 39.2K) w/ 1% accuracy
Sense B	I	18	Jack Detect Pin 2	Resistor (5.1K, 10K, 20K, 39.2K) w/ 1% accuracy
				Total: 18 pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
JDREF	-	19	Ref. Resistor for Jack Detect	20K, 1% accuracy resistor to analog ground
VREF	-	27	2.5V Reference Voltage	1 μ f capacitor to analog ground
MIC1-VREFO-L	O	28	Bias Voltage for MIC1 Jack	2.5V/3.2V/4.2Vreference voltage
MIC2-VREFO	O	29	Bias Voltage for MIC2 Jack	2.5V/3.2V/4.2Vreference voltage
MIC1-VREFO-R	O	30	Secondary Bias voltage for MIC1 jack	2.5V/3.2V/4.2Vreference voltage
CPVREF		31	0V Reference Voltage	Analog ground
CBN	-	35	Reference Capacitor	2.2 μ f capacitor to CBP
CBP	-	36	Reference Capacitor	2.2 μ f capacitor to CBN
				Total: 8 pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
AVDD1	P	25	Analog VDD (5.0V or 3.3V)	Analog power for mixer and amplifier
AVSS1	G	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	P	38	Analog VDD (5.0V or 3.3V)	Analog power for DACs and ADCs
AVSS2	G	37	Analog GND	Analog ground for DACs and ADCs
DVDD	P	1	Digital VDD (3.3V)	Digital core power for core logic
DVDD-IO	P	9	Digital VDD (3.3V or 1.5V)	Digital I/O power for HDA link
DVSS	G	7	Digital GND	Digital ground
PVDD1	P	39	Power Stage VDD 5.0V	Power supply for full-bridge left channel
PVSS1	G	42	Power Stage GND	Ground for full-bridge left channel
PVSS2	G	43	Power Stage GND	Ground for full-bridge right channel
PVDD2	P	46	Power Stage VDD 5.0V	Power supply for full-bridge right channel
CPVEE	P	34	Reference Voltage Output	2.2 μ f capacitor to analog ground
				Total: 12 pins

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

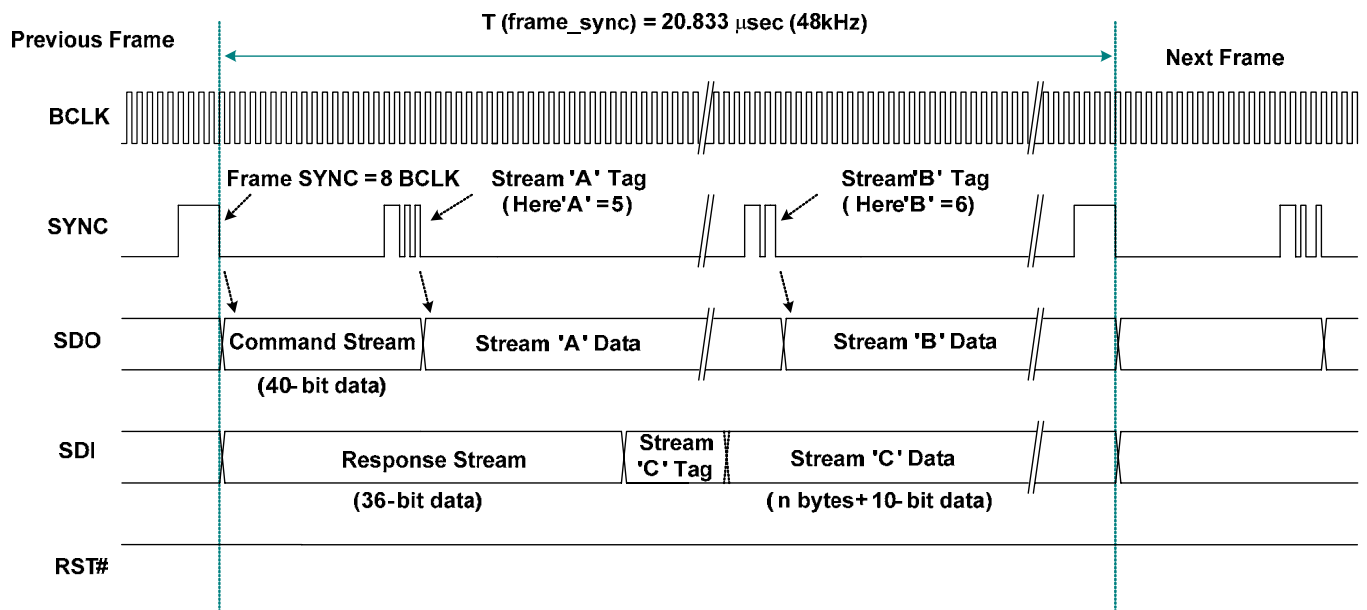


Figure 4. HDA Link Protocol

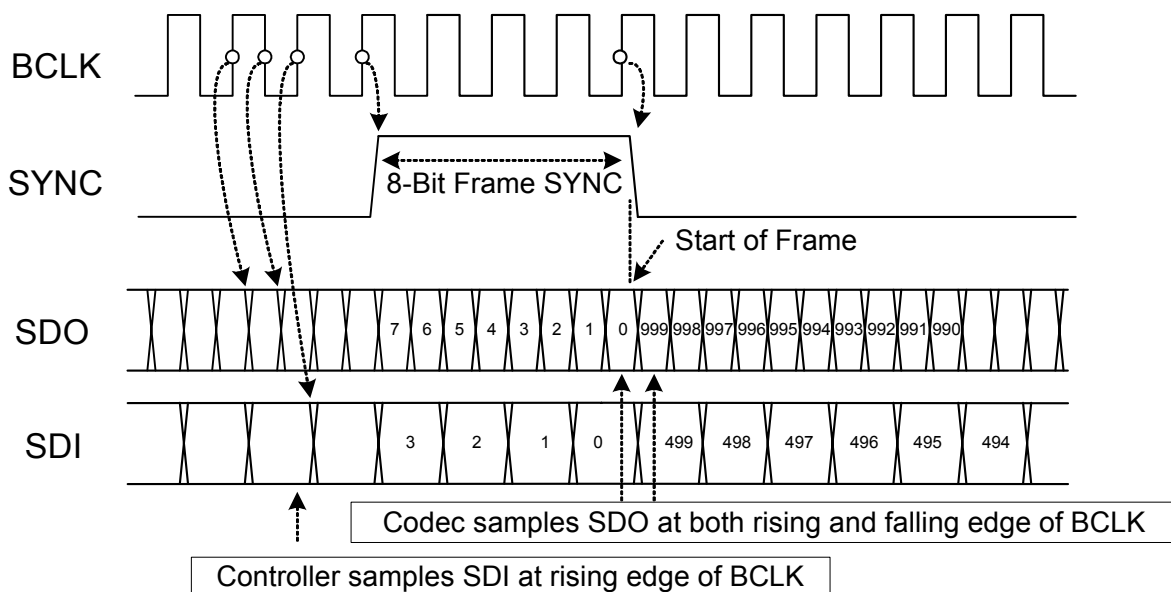
7.1.1. Signal Definitions

Table 5. Link Signal Definitions

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connected to all codecs.
SYNC	48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial Data Output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial Data Input signal driven by the codec. It is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.

Table 6. HDA Signal Definitions

Signal Name	Source	Controller Type	Description
BCLK	Controller	Output	Global 24.0MHz Bit Clock.
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal.
SDO	Controller	Output	Serial Data Output from Controller.
SDI	Codec/Controller	Input/Output	Serial Data Input from codec. Weakly pulled down by the controller.
RST#	Controller	Output	Global Active Low Reset Signal.


Figure 5. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 13 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC269 is designed to receive a single SDO stream.

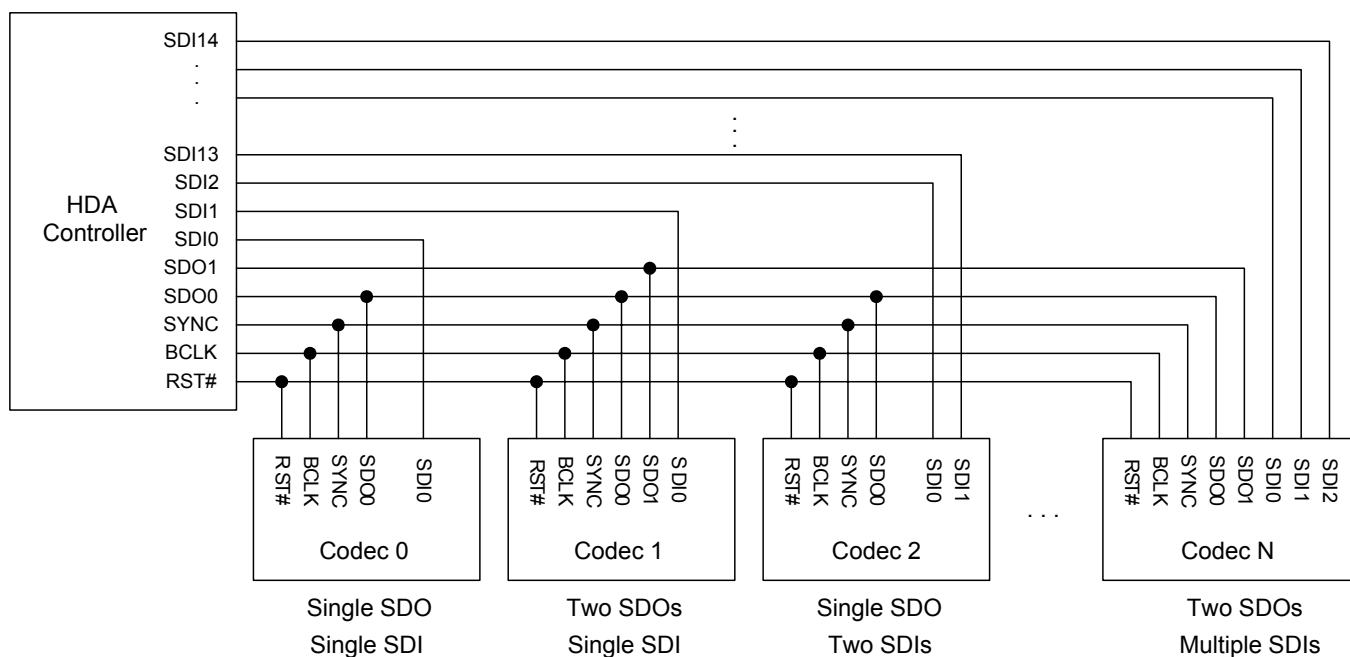


Figure 6. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-Bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-Bit preamble and 4-Bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

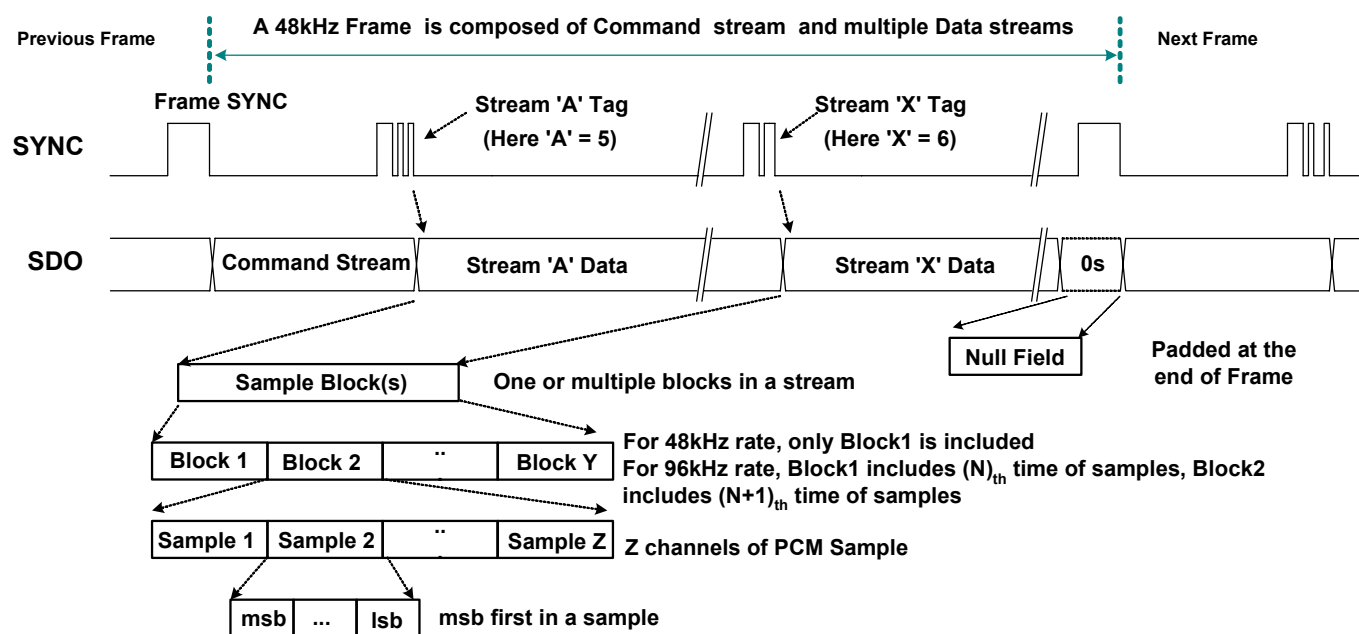


Figure 7. SDO Outbound Frame

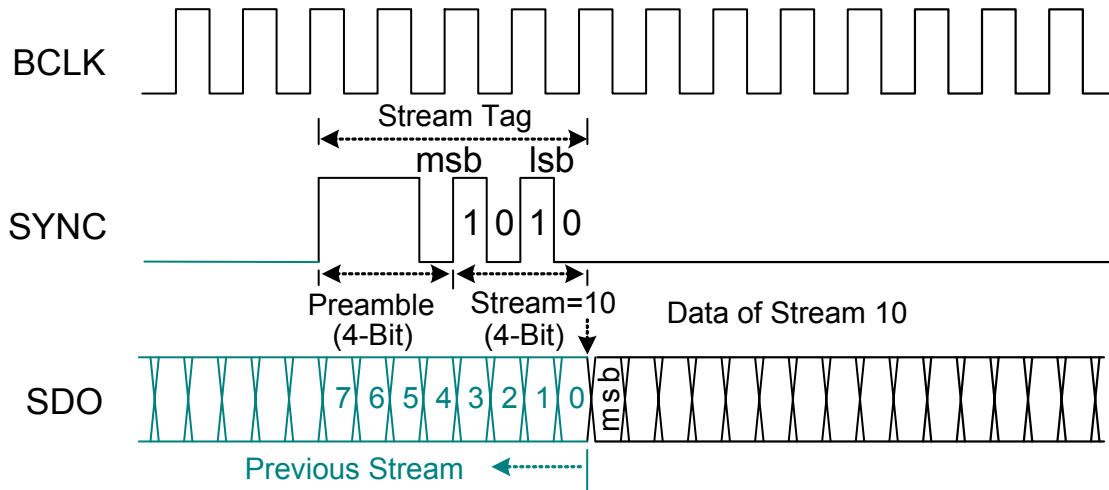


Figure 8. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDO

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the stripe control bit in the controller's Output Stream Control Register to initiate a specific stream (Stream 'A' in Figure 9) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

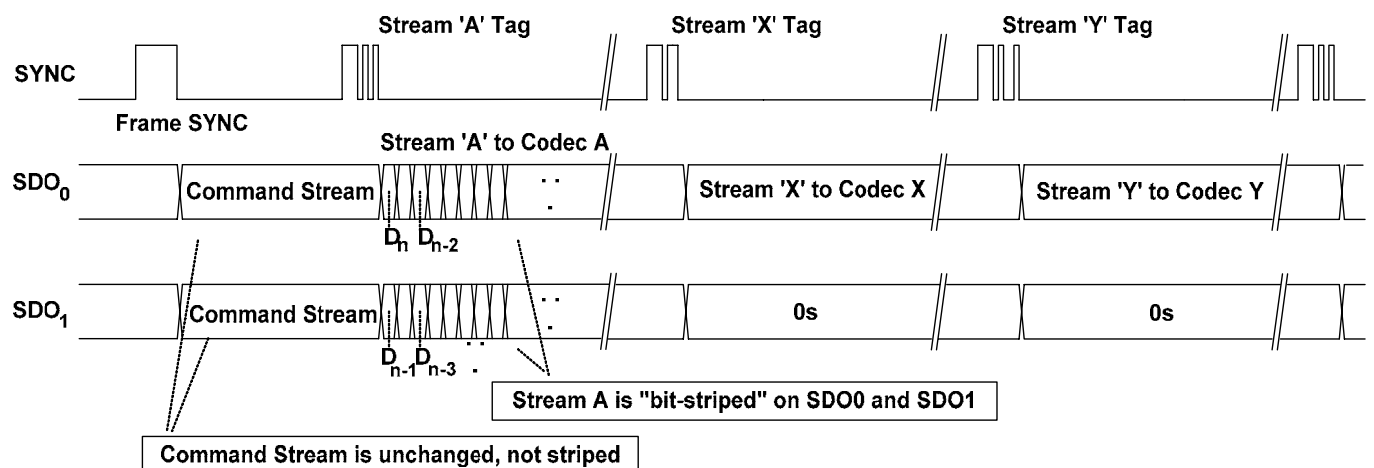


Figure 9. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – Single SDI is composed of one 36-Bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 10).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-Bit stream tag, one 6-Bit data length, and n-Bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 11).

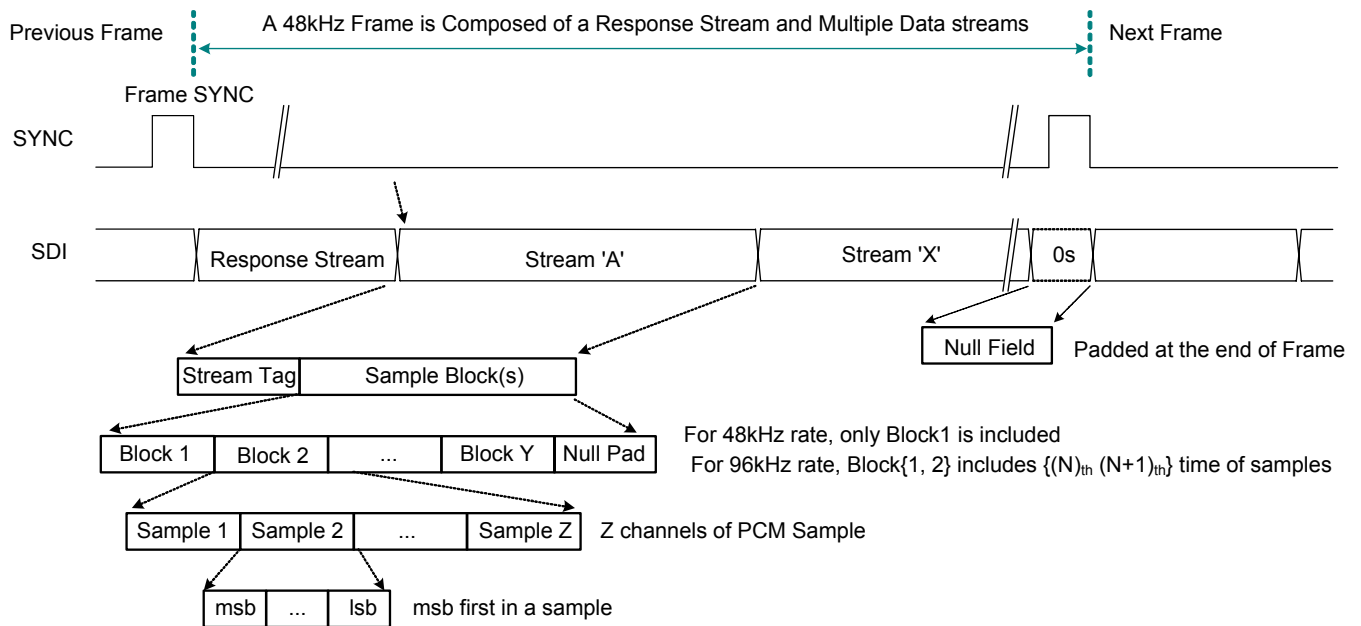


Figure 10. SDI Inbound Stream

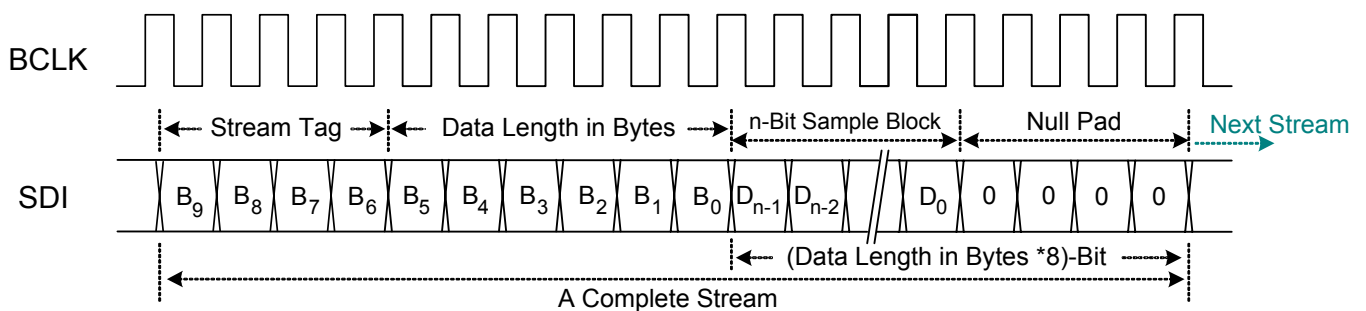


Figure 11. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDI

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data onto separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

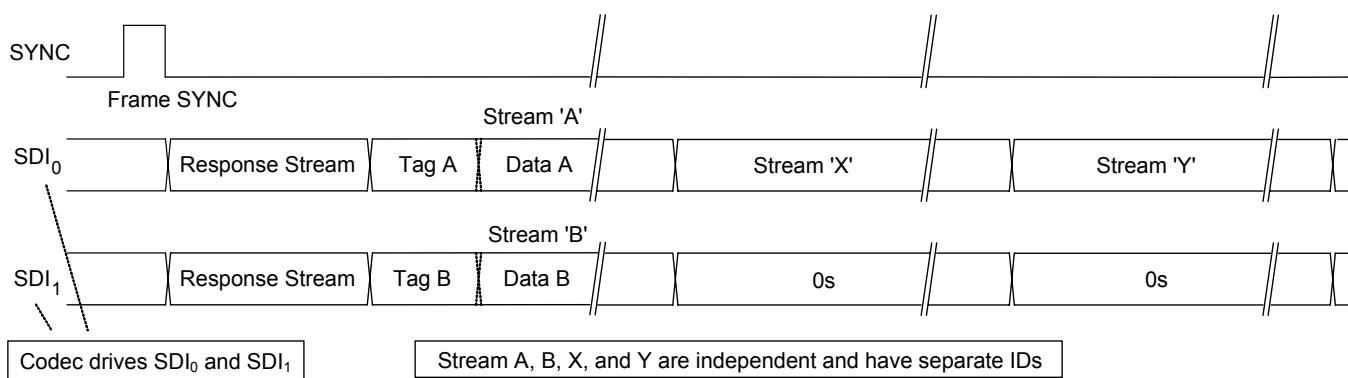


Figure 12. Codec Transmits Data Over Multiple SDIs

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 17, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 17, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence ‘12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)’ interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 9, page 18).

Table 7. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 8. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y ² NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y ² (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y ⁴ (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame. Y: One sample block in a frame. Yx: X sample blocks in a frame.

Table 9. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-}
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-}{11}{-}
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² - (repeat)
174.4kHz	12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ - (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN
 {11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN
 {-}=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYNYNYNYNYN
 {11}=YNYNYNYNYNYNYNYNYNYNYNYNYNYNYNYN
 {-}=NN

44.1kHz: 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz: 12²- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

176.4kHz: 12⁴- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset
2. Codec Reset
3. Codec changes its power state (For example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the ‘CRST’ bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 13, page 20, shows the ‘Link Reset’ timing including the ‘Enter’ sequence (❶~❺) and ‘Exit’ sequence (❻~❾)

Enter ‘Link Reset’:

- ❶ Software writes a 0 to the ‘CRST’ bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ As the controller completes the current frame, it does not signal the normal 8-Bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RST# signal to low, and enters the ‘Link Reset’ state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from ‘Link Reset’:

- ⑥ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)
- ⑦ Software is responsible for de-asserting RST# after a minimum of 100μsec BCLK running time (the 100μsec provides time for the codec PLL to stabilize)
- ⑧ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC
- ⑨ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

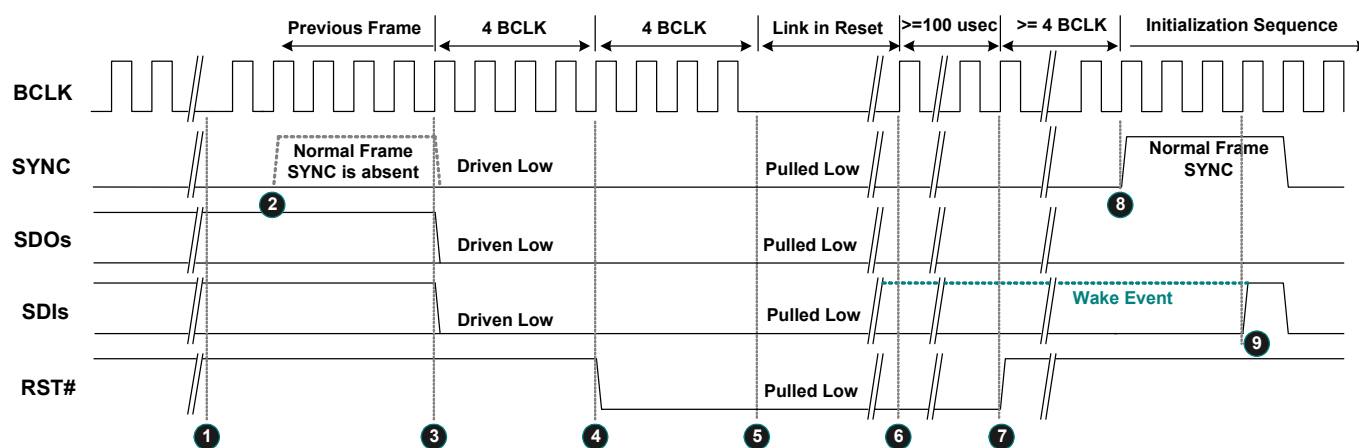


Figure 13. Link Reset Timing

7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec will stop driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operation state

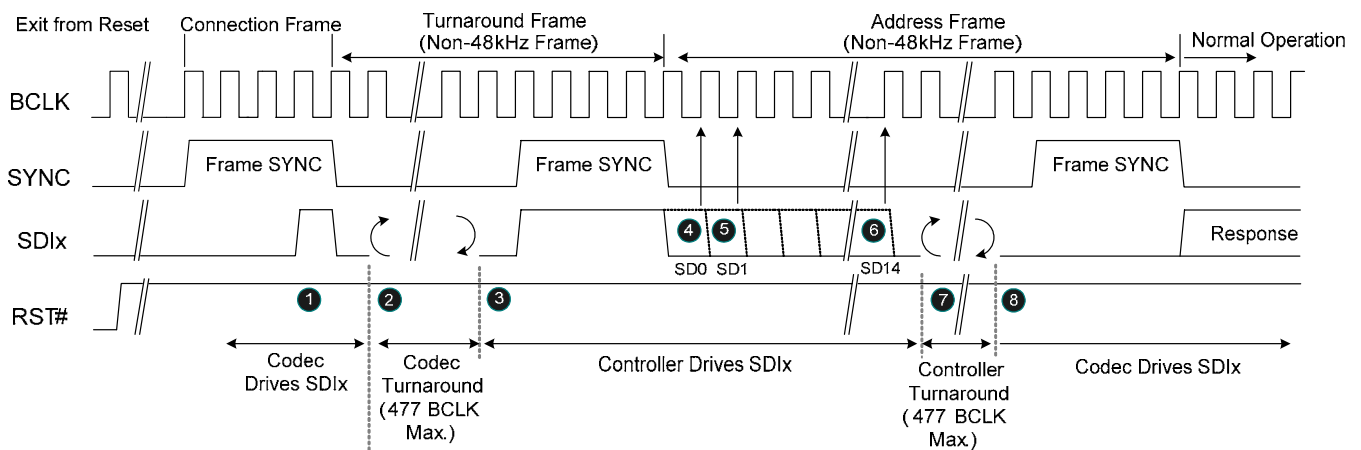


Figure 14. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-Bit identifiers (4-Bit verbs) and 16-Bits of data, the other with 12-Bit identifiers (12-Bit verbs) and 8-Bits of data. Table 10 shows the 4-Bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-Bit verb structure that gets and controls parameters in the codec.

Table 10. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 11. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-Bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The ‘Tag’ in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 13. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-Bits wide. The response is placed in the lower 32-bit field. Bit-35 is a ‘Valid’ bit to indicate the response is ‘Ready’. Bit-34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions.

In the ALC269, all the widgets include output/input converters support power control. Software may have various power states depending on system configuration.

Table 15 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-grained power control.

Table 14. System Power State Definitions

Power States	Definitions
D0	All power on. Individual DACs and ADCs can be powered up or down as required.
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up.
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference off (D1 + analog reference off).
D3 (Hot)	Power still supplied. The codec stops the internal clock. State is maintained.
D3 (Cold)	All power removed. State lost.

Table 15. Power Controls in NID=01h

	Description	D0	D1	D2	D3 (Hot/Cold)	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	DACs	Normal	PD	PD	PD	PD
	ADCs	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down

Table 16. Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
DAC powered down	Analog block and digital filter are powered down.
ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
Headphone Driver powered down	All headphone drivers are powered down.
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive.
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off.

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC269. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. Refer to section 7.4.1 Command Verb Format, page 22, to get detailed information about supported parameters.

Table 17. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format

Codec Response Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]

Response [31:0]
32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format

Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID).
15:0	Device ID=0269h.

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 19. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC269 is fully compliant.
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC269 is fully compliant.
15:8	Revision ID. The vendor's revision number. 00h is for the first silicon version A, 01h is for the second version B, etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID.

Note: The Root Node (NID=00h in the ALC269) supports this parameter.

For example, Revision ID=00h and Stepping ID=01h indicates the silicon is the A1 version.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node. For function group nodes, it provides the total number of widgets associated with this function node.

Table 20. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:16	Starting Node Number. The starting node number in the sequential widgets.
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group.

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 21. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's.
8	UnSol Capable. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 22. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's.
16	Beep Generator. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group.
15:12	Reserved. Read as 0's.
11:8	Input Delay.
7:4	Reserved. Read as 0's.
3:0	Output Delay.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 23. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	Widget Type. 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets.
15:11	Reserved. Read as 0's.
10	Power Control. 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital. 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List. 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable. 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget. 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0.
4	Format Override.
3	AmpParOvr. AMP Param Override.
2	OutAmpPre. Out AMP Present.
1	InAmpPre. In AMP Present.
0	Stereo. 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameter in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

Table 24. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's.
20	B32. Indicates whether 32-Bit audio format is supported. 0: Not supported 1: Supported
19	B24. Indicates whether 24-Bit audio format is supported. 0: Not supported 1: Supported
18	B20. Indicates whether 20-Bit audio format is supported. 0: Not supported 1: Supported
17	B16. Indicates whether 16-Bit audio format is supported. 0: Not supported 1: Supported
16	B8. Indicates whether 8-Bit audio format is supported. 0: Not supported 1: Supported
15:12	Reserved. Read as 0's.
11	R12. Indicates whether 384kHz (=8*48kHz) rate is supported. 0: Not supported 1: Supported
10	R11. Indicates whether 192kHz (=4*48kHz) rate is supported. 0: Not supported 1: Supported
9	R10. Indicates whether 176.4kHz (=4*44.1kHz) rate is supported. 0: Not supported 1: Supported
8	R9. Indicates whether 96kHz (=2*48kHz) rate is supported. 0: Not supported 1: Supported
7	R8. Indicates whether 88.2kHz (=2*44.1kHz) rate is supported. 0: Not supported 1: Supported
6	R7. Indicates whether 48kHz rate is supported. 0: Not supported 1: Supported
5	R6. Indicates whether 44.1kHz rate is supported. 0: Not supported 1: Supported
4	R5. Indicates whether 32kHz (=2/3*48kHz) rate is supported. 0: Not supported 1: Supported
3	R4. Indicates whether 22.05kHz (=1/2*44.1kHz) rate is supported. 0: Not supported 1: Supported
2	R3. Indicates whether 16kHz (=1/3*48kHz) rate is supported. 0: Not supported 1: Supported
1	R2. Indicates whether 11.025kHz (=1/4*44.1kHz) rate is supported. 0: Not supported 1: Supported
0	R1. Indicates whether 8kHz (=1/6*48kHz) rate is supported. 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

Table 25. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's.
2	AC3. 0: Not supported 1: Supported)
1	Float32. 0: Not supported 1: Supported
0	PCM. 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 26. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description														
31:16	Reserved. Read as 0's.														
15:8	VREF Control Capability. '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>7:6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>100%</td> <td>80%</td> <td>Reserved</td> <td>Ground</td> <td>50%</td> <td>Hi-Z</td> </tr> </tbody> </table>	7:6	5	4	3	2	1	0	Reserved	100%	80%	Reserved	Ground	50%	Hi-Z
7:6	5	4	3	2	1	0									
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z									
7	L-R Swap. Indicates the capability of swapping the left and rights.														
6	Balanced I/O Pin. '1' indicates this pin complex has balanced pins.														
5	Input Capable. '1' indicates this pin complex supports input.														
4	Output Capable. '1' indicates this pin complex supports output.														
3	Headphone Drive Capable. '1' indicates this pin complex has an amplifier to drive a headphone.														
2	Presence Detect Capable. '1' indicates this pin complex can detect whether there is anything plugged in.														
1	Trigger Required. '1' indicates whether a software trigger is required for an impedance measurement.														
0	Impedance Sense Capable. '1' indicates this pin complex can perform analog sense on the attached device to determine its type.														

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 27. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. ‘0’ means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. ‘0’ means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 29. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0.
7	Short Form. 0: Short Form 1: Long Form
6:0	Connect List Length. Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget).

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 30. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's.
3	D3Sup. 1: Power state D3 is supported.
2	D2Sup. 1: Power state D2 is supported.
1	D1Sup. 1: Power state D1 is supported.
0	D0Sup 1: Power state D0 is supported.

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 31. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	NumCoeff. Number of Coefficient.
7:1	Reserved. Read as 0's.
0	Benign. 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 32. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0. The ALC269 does not support GPIO wake up function.
30	GPIUnsol=1. The ALC269 supports GPIO unsolicited response.
29:24	Reserved. Read as 0's.
23:16	NumGPIs=00h. No GPI pin is supported.
15:8	NumGPOs=00h. No GPO pin is supported.
7:0	NumGPIOs=02h. Two GPIO pins are supported.

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 33. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0's.
7	Delta. 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps. The number of steps in the range of the Volume Control Knob.

Note: The ALC269 does not support volume control knob.

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 34. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=F01h	0's	Bit[7:0] are Connection Index	

Codec Response for Multiplexer Widget NID=14h~15h, 18h~1Bh

Bit	Description
31:8	0's.
7:0	Connection Index currently Set (Default value is 00h). 00h: Pin Widget NID=0Ch 01h: Pin Widget NID=0Dh Other: Reserved

Codec Response for Multiplexer Widget NID=23h

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Pin Widget NID=18h 01h: Pin Widget NID=19h 02h: Pin Widget NID=1Ah 03h: Pin Widget NID=1Bh 04h: Pin Widget NID=1Dh 05h: Pin Widget NID=12h 06h: Mixer Widget NID=0Bh Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 35. Verb – Set Connection Select (Verb ID=701h)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]	0's for all nodes	

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 36. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F02h	Offset Index – N[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=07h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 24h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=08h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 23h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Ch

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LOUT1 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Dh

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 03h (LOUT2 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Eh

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Dh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 0Ch (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=14h~15h, 18h~1Bh

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Dh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 0Ch (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=16h

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 0Eh (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=1Eh)

Bit	Description
31:8	Connection List Entry (N+3, (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Return 06h (First S/PDIF-OUT converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=11h)

Bit	Description
31:8	Connection List Entry (N+3, (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Return 10h (Secondary S/PDIF-OUT converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=23h (MUX Widget)

Bit	Description
31:24	Connection List Entry (N+3). Return 1Bh (Pin Complex - LINE2) for N=0~3. Return 00h for N>3.
23:16	Connection List Entry (N+2). Return 1Ah (Pin Complex - LINE1) for N=0~3. Return 0Bh (Mixer Widget) for N=4~7. Return 00h for N>7.
15:8	Connection List Entry (N+1). Return 19h (Pin Complex - MIC2) for N=0~3. Return 12h (Pin Complex - DMIC-DATA) for N=4~7. Return 00h for N>7.
7:0	Connection List Entry (N). Return 18h (Pin Complex - MIC1) for N=0~3. Return 1Dh (Pin Complex - PCBEEP) for N=4~7. Return 00h for N>7.

Codec Response for NID=24h (Mixer Widget)

Bit	Description
31:24	Connection List Entry (N+3). Return 1Bh (Pin Complex - LINE2) for N=0~3. Return 00h for N>3.
23:16	Connection List Entry (N+2). Return 1Ah (Pin Complex - LINE1) for N=0~3. Return 00h for N>3.
15:8	Connection List Entry (N+1). Return 19h (Pin Complex - MIC2) for N=0~3. Return 0Bh (Mixer Widget) for N=4~7. Return 00h for N>3.
7:0	Connection List Entry (N). Return 18h (Pin Complex - MIC1) for N=0~3. Return 1Dh (Pin Complex - PCBEEP) for N=4~7. Return 00h for N>3.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 37. Verb – Get Processing State (Verb ID=F03h)
Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F03h	0's

Codec Response Format

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.6. Verb – Set Processing State (Verb ID=703h)

Table 38. Verb – Set Processing State (Verb ID=703h)
Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 39. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=Dh	0's	Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Coefficient Index.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 40. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]	0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 41. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Processing Coefficient.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 42. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 43. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=Bh	‘Get’ payload [15:0]	Bit[7:0] are responsible for ‘Get’	

‘Get’ Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output. 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right. 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0’s.
3:0	Index[3:0] for Input Source. Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored.

Codec Response for NID=02h (LOUT1 DAC) and 03h (LOUT2 DAC)

Bit	Description									
31:8	0’s.									
7	Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0 (No Output Amplifier Mute).									
6:0	Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0’s (No Input Amplifier Gain). Payload[15] is 1 in ‘Get Amplifier Gain’: 6-bit control specifying the volume from –63dB~ +1dB in 1dB step. <table border="1" data-bbox="365 1361 1401 1473"> <thead> <tr> <th>Node</th> <th>Gain[6:0] (Default)</th> <th>Gain Range</th> </tr> </thead> <tbody> <tr> <td>LOUT1 DAC(NID=02h)</td> <td>1000000b=3Fh (0dB)</td> <td>–63dB~+1dB in 1dB step</td> </tr> <tr> <td>LOUT2 DAC (NID=03h)</td> <td>1000000b=3Fh (0dB)</td> <td>–63dB~+1dB in 1dB step</td> </tr> </tbody> </table>	Node	Gain[6:0] (Default)	Gain Range	LOUT1 DAC(NID=02h)	1000000b=3Fh (0dB)	–63dB~+1dB in 1dB step	LOUT2 DAC (NID=03h)	1000000b=3Fh (0dB)	–63dB~+1dB in 1dB step
Node	Gain[6:0] (Default)	Gain Range								
LOUT1 DAC(NID=02h)	1000000b=3Fh (0dB)	–63dB~+1dB in 1dB step								
LOUT2 DAC (NID=03h)	1000000b=3Fh (0dB)	–63dB~+1dB in 1dB step								

Codec Response for NID=0Ch, 0Dh and 0Eh (Mixer)

Bit	Description
31:8	0’s.
7	Payload[15] is 0 in ‘Get Amplifier Gain’: 1: Mute, 0:Unmute (Input Amplifier Mute). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0’s (No Input Amplifier Gain). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Gain).

Codec Response for NID=18h, 19h, 1Ah and 1Bh (Pin widget: MIC1, MIC2, LINE1 and LINE2)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': 1: Mute, 0:Unmute (Output Amplifier Mute, default=1).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. The volume 0dB/10dB/20dB/30dB in 10dB per step (default=0, 0dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=14h, 15h and 16h (Pin widget: SPK-OUT, HP-OUT and MONO-OUT)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': 1: Mute, 0:Unmute (Output Amplifier Mute, default=1).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=0Bh (Mixer)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default for all) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. Specifying the volume from -34.5dB~+12dB in 1.5dB step (Default: 17h, 0dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

	Index=0 (MIC1)	Index=1 (MIC2)	Index=2 (LINE1)	Index=3 (LINE2)	Index=4 (PCBEEP)	Index>5 (Other)
Mute [7]	0/1	0/1	0/1	0/1	0/1	0
Gain [6:0]	0s	0s	0s	0s	0s	0
Default[7:0]	10010111	10010111	10010111	10010111	10010111	00000000

Codec Response for NID=07h, 08h (ADCs)

Bit	Description									
31:8	0's.									
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).									
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. Specifying the volume from -17dB~ 29dB in 1.0dB step. <table border="1" data-bbox="363 1713 1401 1825"> <thead> <tr> <th>Node</th> <th>Gain[6:0] Default</th> <th>Gain Range</th> </tr> </thead> <tbody> <tr> <td>MIC ADC(NID=07h)</td> <td>0010001b=11h (0dB)</td> <td>-17dB~29dB in 1.0dB step</td> </tr> <tr> <td>LINE ADC(NID=08h)</td> <td>0010001b=11h (0dB)</td> <td>-17dB~29dB in 1.0dB step</td> </tr> </tbody> </table> Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).	Node	Gain[6:0] Default	Gain Range	MIC ADC(NID=07h)	0010001b=11h (0dB)	-17dB~29dB in 1.0dB step	LINE ADC(NID=08h)	0010001b=11h (0dB)	-17dB~29dB in 1.0dB step
Node	Gain[6:0] Default	Gain Range								
MIC ADC(NID=07h)	0010001b=11h (0dB)	-17dB~29dB in 1.0dB step								
LINE ADC(NID=08h)	0010001b=11h (0dB)	-17dB~29dB in 1.0dB step								

Codec Response for NID=24h (Mixer)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default for all) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

	Index=0 (MIC1)	Index=1 (MIC2)	Index=2 (LINE1)	Index=3 (LINE2)	Index=4 (PCBEEP)	Index=5 (Mixer)	Index>5 (Other)
Mute [7]	0/1	0/1	0/1	0/1	0/1	0/1	0
Gain [6:0]	0s	0s	0s	0s	0s	0s	0
Default[7:0]	10000000	10000000	10000000	10000000	10000000	10000000	00000000

Codec Response to Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 44. Verb – Set Amplifier Gain (Verb ID=3h)
Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp. 1 indicates output amplifier gain will be set.
14	Set Input Amp. 1 indicates input amplifier gain will be set.
13	Set Left Amp. 1 indicates left amplifier gain will be set.
12	Set Right Amp. 1 indicates right amplifier gain will be set.
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets). 5 bits index offset in connection list is used to select which input gain will be set on a mixer or a multiplexer widget. The index is ignored if the node is not a mixer or a multiplexer widget, or the 'Set Input Amp' bit is not set.
7	Mute. 0: Unmute 1: Mute ($-\infty$ gain)
6:0	Gain[6:0]. A 7-bit step value specifying the amplifier gain.

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 45. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Bit[15:0] are converter format

Codec Response for NID=02h, 03h, 06h, 10h (Output Converters: LOUT1 DAC, LOUT2 DAC, S/PDIF-OUT, S/PDIF-OUT2). Codec Response for NID=07h, 08h (Input Converters: MIC ADC, LINE ADC)

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC269 does not support Divisor. Always read as 000b.
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels

	BASE	MULT	DIV	BITS	Sample Rate
NID=02h (LOUT1 DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=03h (LOUT2 DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=06h (S/PDIF-OUT)	0	000b, 001b, 011b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b, 001b	000b	001b, 010b, 011b, 100b	44.1K, 88.2K
	0	001b	010b	001, 010b, 011b	32K
NID=10h (S/PDIF-OUT2)	0	000b, 001b, 011b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b, 001b	000b	001b, 010b, 011b, 100b	44.1K, 88.2K
	0	001b	010b	001, 010b, 011b	32K
NID=07h (MIC ADC)	0	000b, 001b	000b	001b, 010b, 011b	48K, 96K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=08h (LINE ADC)	0	000b, 001b	000b	001b, 010b, 011b	48K, 96K
	1	000b	000b	001b, 010b, 011b	44.1K

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 46. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h)

Table 47. Verb – Get Power State (Verb ID=F05h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F05h	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set.
3:2	Reserved. Read as 0's.
1:0	PS-Set, Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node.

Note: Specific blocks will be powered down in each power state. Refer to section 7.5 Power Management, page 23.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.16. Verb – Set Power State (Verb ID=705h)

Table 48. Verb – Set Power State (Verb ID=705h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=F06h	0's	Stream & Channel [7:0]	

Codec Response for NID=02h, 03h, 06h, 10h (Output Converters: LOUT1 DAC, LOUT2 DAC, S/PDIF-OUT and S/PDIF-OUT2).

Codec Response for NID=07h, 08h (Input Converters: MIC ADC, LINE ADC)

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 49. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]	0's for all nodes	

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Set Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Note: This verb assigns stream and channel for output converters (NID=02h, 03h, 06h, 10h) and input converters (NID=07h, 08h). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 50. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for pin widget NID=12h, 14h, 15h, 16h, 18h~1Bh, 1Dh, 1Eh and 11h. (Pin Complex: DMIC-DATA, SPK-OUT, HP-OUT, MONO-OUT, MIC1, MIC2, LINE1, LINE2, PCBEEP, S/PDIF_OUT and S/PDIF-OUT2).

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O unit). 0: Disabled 1: Enabled.
6	Out Enable (Output Buffet Enable, EN_OBUF for an I/O unit). 0: Disabled 1: Enabled.
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled.
4:3	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 51. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0]: pin widget NID=12h, 14h, 15h, 16h, 18h~1Bh, 1Dh, 1Eh and 11h. (Pin Complex: DMIC-DATA, SPK-OUT, HP-OUT, MONO-OUT, MIC1, MIC2, LINE1, LINE2, PCBEEP, S/PDIF_OUT and S/PDIF-OUT2).

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable. 0: Disabled 1: Enabled
6	Out Enable. 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled
4:	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 54. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=F09h	0's	32-bit Response

Codec Response: Pin widget 15h (HP-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Bh (LINE2)

Bit	Description
31	Presence Detect Status. 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance. <i>Note: The ALC269 does not support impedance sensing. Read as 0's.</i>

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 55. Verb – Execute Pin Sense (Verb ID=709h)

Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=709h	Right Channel[0]	0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's.
0	Right (Ring) Channel Select. 0: Sense Left channel (Tip) 1: Sense Right channel (Ring)

Note: The ALC269 does not support 'Execute Pin Sense' and will ignore this verb and respond with 0's.

8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 56. Verb – Get Configuration Default (Verb ID=F1Ch)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=F1Ch	0's	32-bit Response

Codec Response for Pin Widget: NID=12h (Digital MIC), 14h (SPK-OUT), 15h (HP-OUT), 16h (MONO-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Bh (LINE2), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT), 11h (S/PDIF-OUT2)

Bit	Description
31:0	32-bit configuration information for each pin widget.

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

**Table 57. Verb – Set Configuration Default Bytes 0, 1, 2, 3
(Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)**

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]	0's for all nodes

Note: Supported by Pin Widget NID=12h (Digital MIC), 14h (SPK-OUT), 15h (HP-OUT), 16h (MONO-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Bh (LINE2), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT), 11h (S/PDIF-OUT2)

Codec Response for All NID

Bit	Description
31:0	0's.

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 58. Verb – Get BEEP Generator (Verb ID=F0Ah)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=F0Ah	0's	Divider [7:0]	

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$. The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 59. Verb – Set BEEP Generator (Verb ID=70Ah)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=Xh	Verb ID=70Ah	Divider [7:0]	0's for all nodes	

'Divider' in Set Command

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is $48\text{kHz}/(255*4)=47\text{Hz}$. The highest tone is $48\text{kHz}/(1*4)=12\text{kHz}$. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.29. Verb – Get GPIO Data (Verb ID=F15h)

Table 60. Verb – Get GPIO Data (Verb ID=F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Data. Not supported in the ALC269.
1:0	GPIO[1:0] Data. The value written (output) or sensed (input) on the corresponding pin if it is enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.30. Verb – Set GPIO Data (Verb ID=715h)

Table 61. Verb – Set GPIO Data (Verb ID=715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Output Data. Not supported in the ALC269.
1:0	GPIO[1:0] Output Data. The value written determines the value driven on a pin that is configured as an output pin.

Codec Response for All NID

Bit	Description
31:0	0's.

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 62. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Get Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=01h	Verb ID=F16h	0's	EnableMask [7:0]	

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:2	Reserved.
1:0	GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state. 1: The corresponding GPIO pin is enabled. It's behavior is determined by the GPIO direction control.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 63. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format				Codec Response Format	
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]	
Cad=X	Node ID=01h	Verb ID=716h	Enable Mask [7:0]	0's for all nodes	

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Enable Mask. Not supported in the ALC269.
1:0	GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. It's behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 64. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F17h	0's

Codec Response Format

Response [31:0]
Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Direction Control. Not supported in the ALC269.
1:0	GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 65. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=717h	Direction [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Direction Control. Not supported in the ALC269.
1:0	GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.35. Verb – Get GPIO Wake Enable Mask(Verb ID=F18h)

Table 66. Verb – Get GPIO Wake Enable Mask (Verb ID=F18h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=01h	Verb ID=F18h	0's	WakeEnalbeMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Wake Enable Mask. Not supported in the ALC269.
1:0	GPIO[1:0] Wake Enable Mask. 0: The corresponding GPIO pin will not generate a wake-up event 1: The corresponding GPIO pin will generate a wake-up event

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.36. Verb-Set GPIO Wake Enable Mask(Verb ID=718h)

Table 67. Verb – Set GPIO Wake Enable Mask (Verb ID=718h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=01h	Verb ID=718h	WakeEnalbeMask [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Wake Enable Mask. Not supported in the ALC269
1:0	GPIO[1:0] Wake Enable Mask. 0: The corresponding GPIO pin will not generate a wake-up event 1: The corresponding GPIO pin will generate a wake-up event

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.37. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 68. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=01h	Verb ID=F19h	0's	UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC269.
1:0	GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.38. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 69. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=01h	Verb ID=719h	UnsolEnable [7:0]	0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC269
1:0	GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.39. Verb – Function Reset (Verb ID=7FFh)

Table 70. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01H)				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=01h	Verb ID=7FFh	0's	0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's.

Note: The Function Reset command causes all widgets in the ALC269 to return to their power-on default state.

8.40. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Table 71. Verb –Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=F0Dh/F0Eh	0's	Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=06h, 10h (S/PDIF-OUT, S/POUT-OUT2) Response to ‘Get verb’ – F0Dh (Control 1 for SIC bit[15:0]).

NID=06h, 10h (S/PDIF-OUT, S/PDIF-OUT2) Response to ‘Get verb’ – F0Eh (Control 2 for SIC bit[15:0]).

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's.
15	Reserved. Read as 0's.
14:8	CC[6:0] (Category Code).
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's.

8.41. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 72. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Dh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Eh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=06h (S/PDIF-OUT), 10h (S/PDIF-OUT2)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

'Payload' in Set Control 2 for NID=06h (S/PDIF-OUT), 10h (S/PDIF-OUT2)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's.
6:0	CC[6:0] (Category Code).

8.42. Get/Set Volume Knob Widget (Verb ID=F0Fh/70Fh)

Table 73. Get/Set Volume Knob Widget (Verb ID=F0Fh/70Fh)

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=F0Fh	0's	Bit[31:8]=0's, Bit[7:0] is volume

Codec Response for Volume Knob Widget

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Volume in Steps.

Note: The ALC269 does not support volume knob widget will ignore this verb and respond with 0's.

Set Command Format (Verb ID=70Fh)

Set Command Format (Verb ID=70Fh)				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=70Fh	Bit[7] is 'Direct' control	0's

'Payload' in Set Command for Volume Knob Widget

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Reserved.

Note: The ALC269 does not support volume knob widget will ignore this verb and respond with 0's.

8.43. Get/Set Subsystem ID [31:0] (Verb ID=F20h/723h~720h to Set Bit[31:0])

Table 74. Get/Set Subsystem ID [31:0] (Verb ID=F20h / 723h~720h to Set Bit[31:0])

Get Command Format				Codec Response Format
Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
Cad=X	Node ID=Xh	Verb ID=F20h	0's	32 bits response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:16	Subsystem ID[23:8] (Default=10Ech).
15:8	Subsystem ID[7:0] (Default=02h).
7:0	Assembly ID[7:0] (Default=69h).

8.44. Get/Set EAPD Enable (Verb ID= F0Ch/70Ch)

Table 75. Get/Set EAPD Enable (Verb ID=F0Ch / 70Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F0Ch	0's

Codec Response Format

Response [31:0]
Bit[1] is EAPD Control

Codec response in Get Command for NID=14h (LINE-OUT Pin Widget), 15h (HP-OUT Pin Widget)

Bit	Description
31:3	Reserved.
2	L-R Swap. The ALC269 does not support swapping left and right channel, it is read as 0.
1	EAPD Value. 0: EAPD pin state is low potential to power down external amplifier in all power state of AFG. 1: EAPD pin state is high potential to power up external amplifier in all power state of AFG.
0	BTL Enable. The ALC269 does not support BTL output, it is read as 0.

Codec Response in Get Command for other NID

Bit	Description
31:0	0s.

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]	Response [31:0]
CAd = X	Node ID=Xh	Verb ID=70Ch	Bit[1] is EAPD Control	0s

Codec Response Format

Payload in Set Command for NID=14h (SPK-OUT Pin Widget), 15h (HP-OUT Pin Widget)

Bit	Description
7:3	Reserved.
2	L-R Swap. The ALC269 does not support swapping left and right channel, it is read as 0.
1	EAPD Value (Default=0). 0: EAPD pin state is low potential to power down external amplifier in all power state of AFG. 1: EAPD pin state is high potential to power up external amplifier in power state of AFG.
0	BTL Enable. The ALC269 does not support BTL output, it is read as 0.

Codec Response in Set Command for all NID

Bit	Description
31:0	0s.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 76. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DVDD	3.0	3.3	3.6	V
Digital Power for Link* ¹	DVDD-IO	1.5	3.3	3.6	V
Analog Power* ²	AVDD1, AVDD2	3.3	5.0	5.25	V
BTL Analog Power* ^{2, *3}	PVDD1, PVDD2	3.3	5.0	5.25	V
Ambient Operating Temperature	T _a	0	-	+70	°C
Storage Temperature	T _s	-	-	+125	°C
ESD (Electrostatic Discharge)					
Susceptibility Voltage					
All Pins Except PVDD1, PVDD2			4000V		
PVDD1 (Pin39), PVDD2 (Pin 46)			3500V		

Note1: DVDD-IO must be lower than DVDD.

Note2: PVDD must be greater than AVDD. Keep PVDD \geq AVDD+0.8V for best performance.

When (PVDD \geq AVDD + 1V), THD+N will be degraded when playing at full power output.

Note3: When the Class-D amplifier is operating, surges of PVDD > 7V duration for 0.1ms may damage the amplifier. To suppress such surges, 10 μ F tantalum capacitors are required at PVDD1 and PVDD2.

9.1.2. Threshold Voltage

DVDD-IO=3.3V \pm 5%, T_{ambient}=25°C, with 50pF external load.

Table 77. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V _{in}	-0.30	-	DVDD +0.30	V
Low Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V _{IL}	-	-	0.30*DVDDIO	V
High Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V _{IH}	0.65* DVDDIO	-	-	V
Low Level Input Voltage (S/PDIF-OUT, GPIOs)	V _{IL}	-	-	0.44*DVDD	V
High Level Input Voltage (S/PDIF-OUT, GPIOs)	V _{IH}	0.56* DVDD	-	-	V
High Level Output Voltage	V _{OH}	0.9*DVDD	-	-	V
Low Level Output Voltage	V _{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	μ A
Output Leakage Current (Hi-Z)	-	-10	-	10	μ A
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

9.1.3. Digital Filter Characteristics

Table 78. Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-76.0	-	dB
	Passband Ripple	-	±0.02	-	dB
DAC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-78.5	-	dB
	Passband Ripple	-	±0.02	-	dB

9.1.4. S/PDIF Output Characteristics

DVDD=3.3V, T_{ambient}=25°C, with 75Ω external load.

Table 79. S/PDIF Input/Output Characteristics

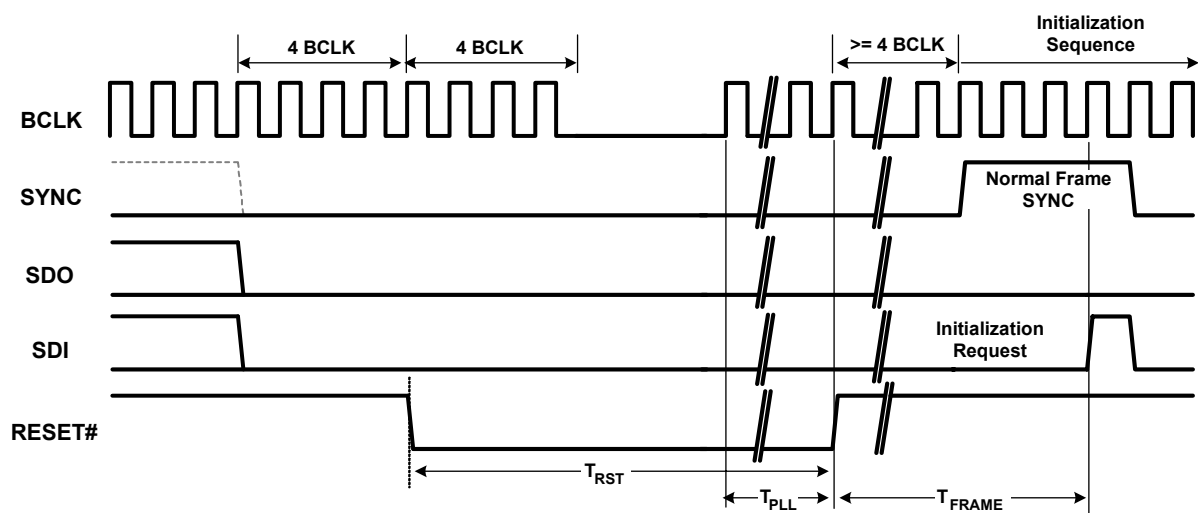
Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V _{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V _{OL}	-	0	0.3	V

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 80. Link Reset and Initialization Timing

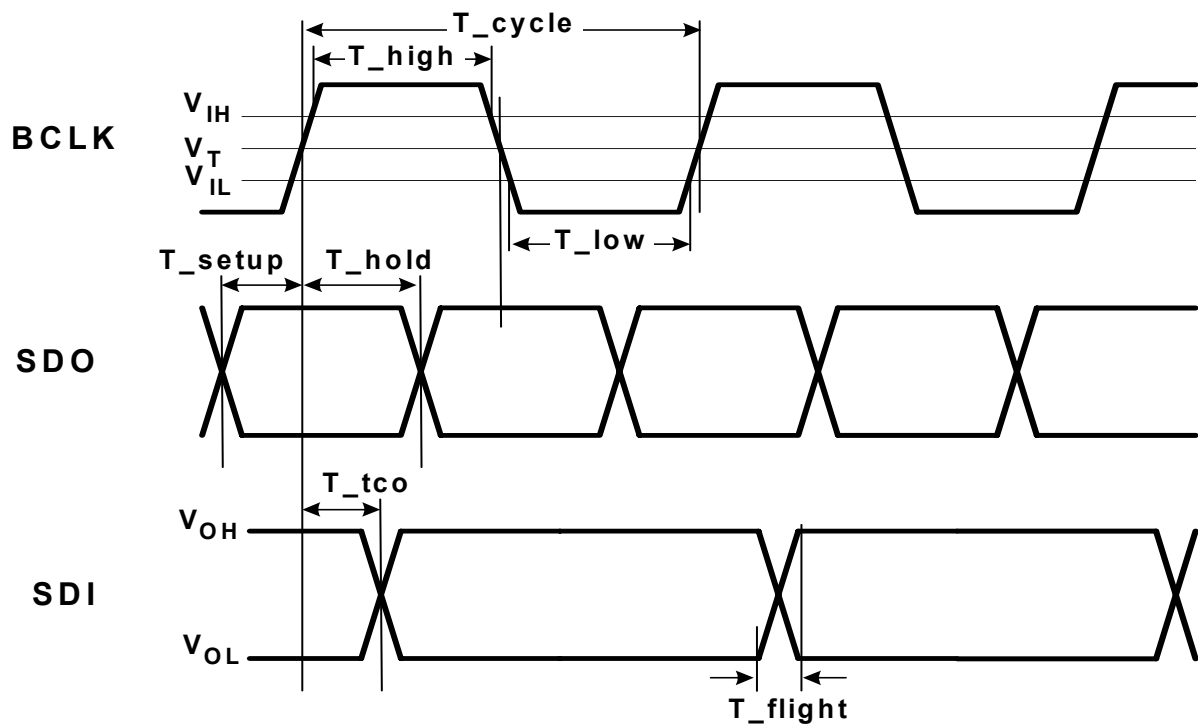
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	μs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	20	-	-	μs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time


Figure 15. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 81. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency	-	-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	T_{low}	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF external load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns


Figure 16. Link Signals Timing

9.2.3. S/PDIF Output Timing

Table 82. S/PDIF Output Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency ^{*1}	-	-	3.072	-	MHz
S/PDIF-OUT Period ^{*1}	T_{cycle}	-	325.6	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width ^{*1}	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width ^{*1}	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns

^{*1}: Bit parameters for 48kHz sample rate of S/PDIF-OUT

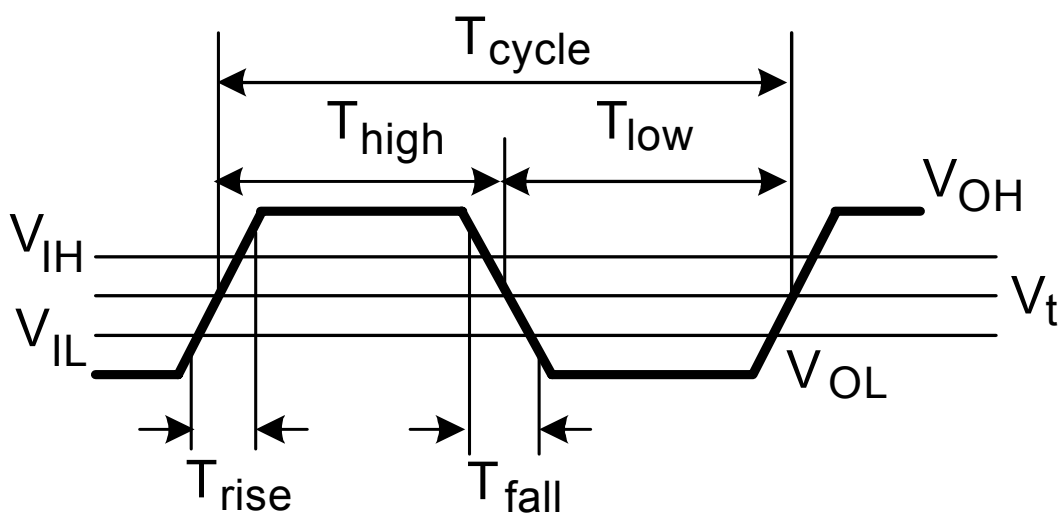


Figure 17. Output Timing

9.2.4. Test Mode

The ALC269 does not support codec test mode or Automatic Test Equipment (ATE) mode.

9.3. Analog Performance

- Standard Test Conditions
- $T_{\text{ambient}}=25^{\circ}\text{C}$, DVDD-CORE=3.3V $\pm 5\%$, AVDD=5.0V $\pm 5\%$
 - 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
 - 10K Ω /50pF load; Test bench Characterization BW:10Hz~22kHz

Table 83. Analog Performance

Parameter	Min	Typ	Max	Units
Full-Scale Input Voltage All ADC (Gain=0dB)	-	1.5	-	Vrms
Full-Scale Output Voltage All DAC (Gain=+1dB)	-	1.5	-	Vrms
Dynamic Range with 1kHz Tone, DR (A Weighted)				
ADC	-	98	-	dB FSA
DAC	-	98	-	dB FSA
Headphone Out @32 Ω Load	-	95	-	dB FSA
Total Harmonic Distortion Plus Noise, THD+N				
ADC	-	-85	-	dB FS
DAC	-	-90	-	dB FS
Headphone Out @32 Ω Load	-	-70	-	dB FS
Frequency Response				
ADC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	Hz
DAC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	Hz
Power Supply Rejection Ratio	-	-60	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step				
ADC	-	1.0	-	dB
DAC	-	1.0	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (Gain=0dB)	-	32	-	K Ω
Output Impedance				
Amplified Output	-	1	-	Ω
Non-Amplified Output	-	200	-	Ω
Digital Power Supply Current (Normal Operation) DVDD=3.3V, DVDD-IO=3.3V	-	50	-	mA
Digital Power Supply Current (Power Down Mode) DVDD=3.3V, DVDD-IO=3.3V	-	2	-	mA
Analog Power Supply Current (Normal Operation) AVDD1, AVDD2=5.0V	-	48	-	mA
Analog Power Supply Current (Power Down Mode) AVDD1, AVDD2=5.0V	-	7	-	mA
VREFOUTx Output Voltage	0	2.50	4.20	V
VREFOUTx Output Current	-	5	-	mA

Note: FSA=Full-Scale with A-weighting filter.

FS=Full-Scale.

9.4. Class-D Power Amplifier Performance

Table 84. Class-D Power Amplifier Performance

Parameter	Min	Typ	Max	Units
Output Voltage @ BTL Mode (Vrms)	-	3.07	-	Vrms
Maximum Output Peak Current @ BTL Mode	-	1.3	-	A
Maximum Output Power @ BTL Mode	-	2.0	2.3	W
Power Efficiency η @ BTL Mode into 4ohm	-	80	-	%
Power Efficiency η @ BTL Mode into 4ohm with Filter	-	84	-	%
Power Efficiency η @ BTL Mode into 8ohm	-	88	-	%
Power Efficiency η @ BTL Mode into 8ohm with Filter	-	92	-	%
Full-Scale Output Voltage @ BTL Mode PCM/PWM Converter	-	+/-4.34	-	Vpeak
S/N (A weighted) @ BTL Mode PCM/PWM Converter	-	90	-	dB FSA
THD+N @ BTL Mode at test signal 997Hz~3dB sine wave PCM/PWM Converter	-	-75	-	dB FS
THD+N @ BTL Mode at test signal around 20Hz~22KHz PCM/PWM Converter	-	-60	-	dB FS
Frequency Response @ BTL Mode PCM/PWM Converter	20	-	22K	Hz
Total Quiescent Current (Iq)	-	1.25	-	nA
P-Type MOS Output Impedence (Rds)	-	150	-	m Ω
N-Type MOS Output Impedence (Rds)	-	250	-	m Ω
PWM Frequency	-	384K	-	Hz
Dead Time (Shoot)	-	0	-	nS
Modulation Index	-	0.8896	-	N/A
Minimum Pulse Width	-	150	-	nS
LQFP-48 Package Thermal Characteristic, Θ_{JA}	-	65.4	-	$^{\circ}\text{C}/\text{W}$
QFN-48 Package Thermal Characteristic, Θ_{JA}	-	32.4	-	$^{\circ}\text{C}/\text{W}$
Output Voltage Noise(Vn) at Mute Condition	-	50	-	μV
Output Short Circuit Protection Limit	-	2.5	-	A
Class-D Output RMS Current, I_L (BTL 4 Ω Load, PVDD = 5.0V, Full Power Output)	-	0.6	-	A
Class-D Output RMS Current, I_L (BTL 4 Ω Load, PVDD = 5.0V, Power Down)	-	0	-	mA

10. Application Circuits

10.1. Filter Connection

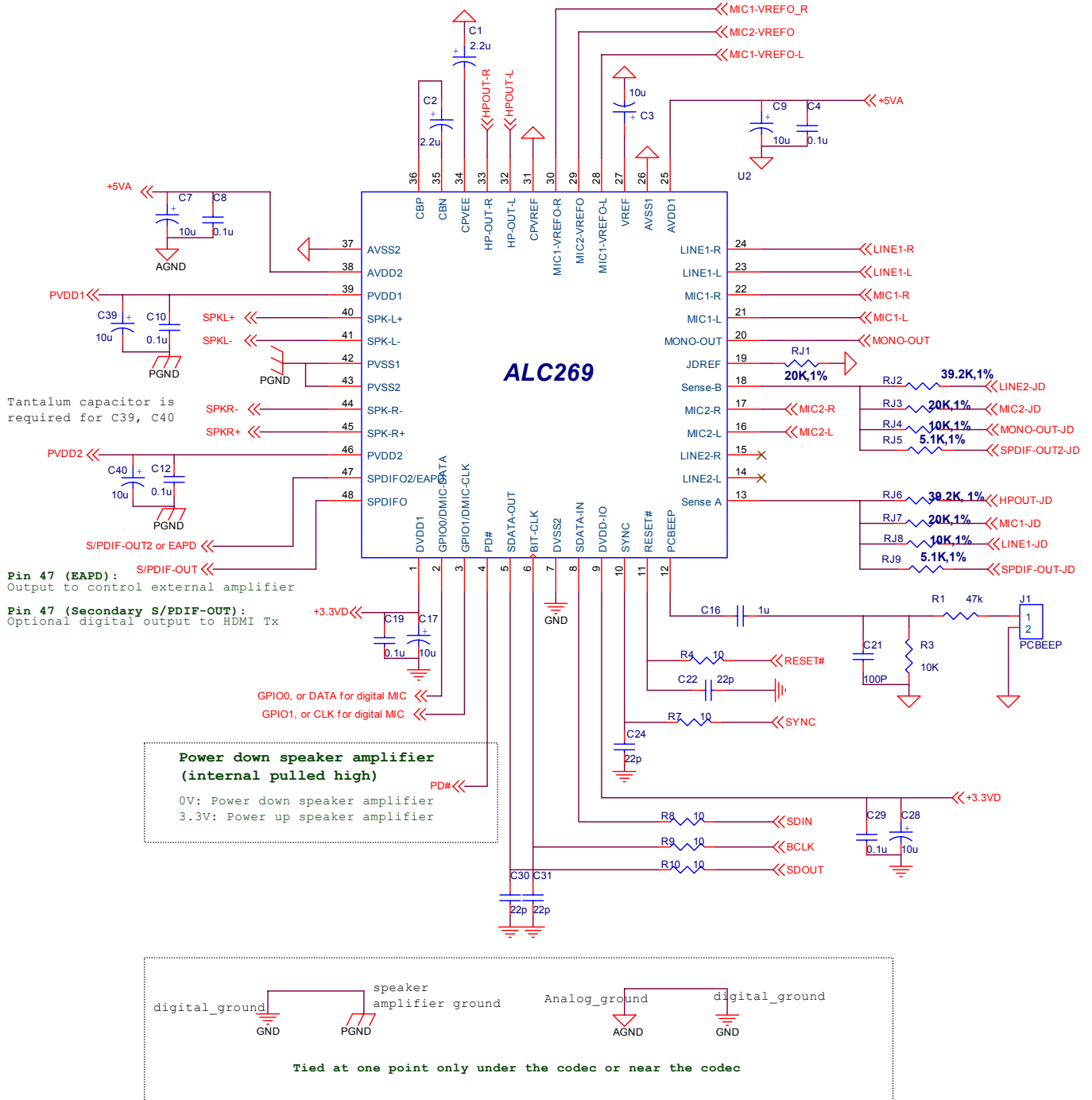
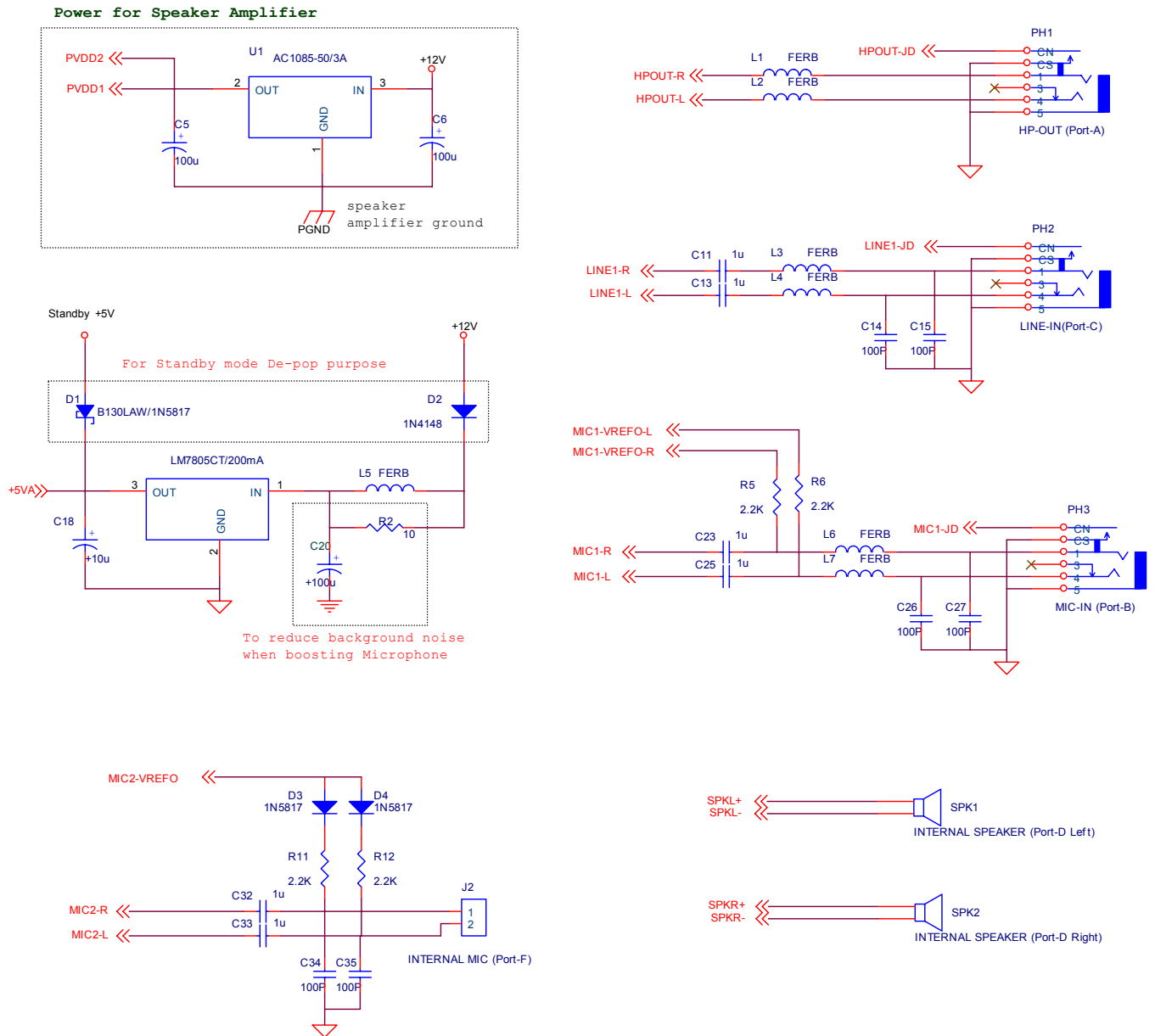


Figure 18. Filter Connection

10.2. Power and Jack Connection



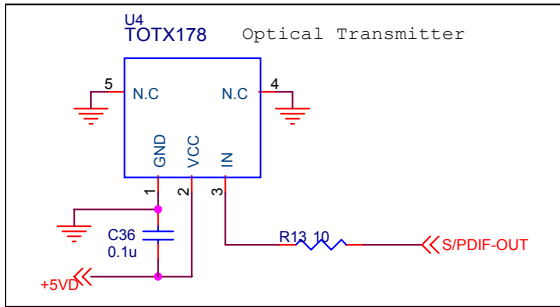
Configuration: (Standard case for Laptop)

Pin/Port Assignment	Location	Functions
HP-OUT (pin-32,33)/Port-A	Chassis	Headphone output
MIC1 (pin-21,22)/Port-B	Chassis	Mic-In for external microphone
LINE1 (pin-23,24)/Port-C	Chassis	Line-In for external line input
MIC2 (pin-16,17)/Port-F	Internal	Mic-In for internal analog microphone
SPK-OUT (pin-40,41,44,45)/Port-D	Internal	Amplifier output for internal speaker

Figure 19. Power and Jack Connection

10.3. SPDIF-OUT Connection

S/PDIF module option 1: Optical



S/PDIF module option 2: Coaxial

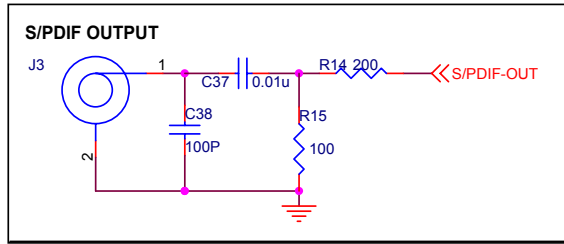
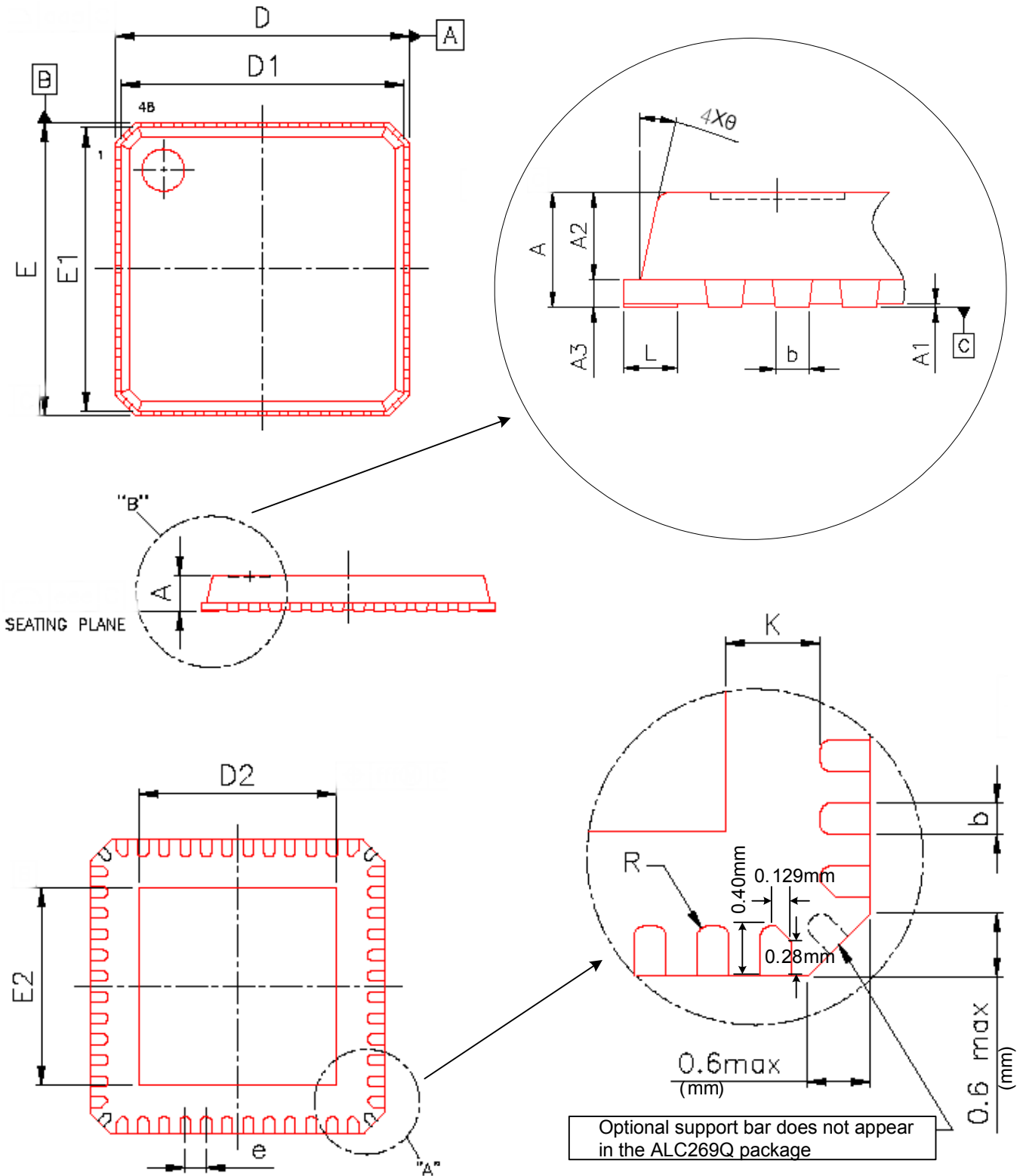


Figure 20. SPDIF-OUT Connection

11. Mechanical Dimensions



11.1. Mechanical Dimensions Notes

SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX.
A	0.75	0.85	1.00	0.030	0.034	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.55	0.65	0.80	0.022	0.026	0.032
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	4.80	5.05	5.30	0.189	0.199	0.209
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
E2	4.80	5.05	5.30	0.189	0.199	0.209
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	14°	0°	-	14°
R	0.09	-	-	0.004	-	-
K	0.20	-	-	0.008	-	-

12. Ordering Information

Table 85. Ordering Information

Part Number	Description	Status
ALC269Q-GR	QFN-48 'Green' Package	Production
ALC269QSRS-GR	ALC269Q-GR + SRS Audio Software	Production

Note: See page 7 for Green package and version identification.

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