



REALTEK

**ALC888S-VD
(PN: ALC888S-VD2-GR)**

7.1+2 CHANNEL HD AUDIO CODEC WITH TWO INDEPENDENT SPDIF OUTPUTS

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC888S-VD ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

| Revision | Release Date | Summary |
|----------|--------------|---------------|
| 1.0 | 2011/03/18 | First release |

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1. General Description

The ALC888S-VD provides ten DAC channels that simultaneously support 7.1 channel sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel stereo outputs. Three stereo ADCs and one stereo digital microphone converter are integrated and can support a microphone array with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies.

All analog I/O are input and output capable, and headphone amplifiers are also integrated at three analog output ports (port-D/port-E/port-F). All analog I/Os can be re-tasked according to user definitions.

Support for 16/20/24-bit SPDIF input and output with up to 192kHz sample rate offers easy connection of PCs to consumer electronic products such as digital decoders and speakers. The ALC888S-VD also features secondary SPDIF-OUT output and converter to transport digital audio output to a High Definition Media Interface (HDMI) transmitter.

The ALC888S-VD supports host audio from the Intel chipsets, and also from any other HDA compatible audio controller. With various software utilities like environment sound emulation, multiple-band and independent software equalizer, dynamic range compressor and expander, optional Dolby PCEE program, SRS TruSurround HD, SRS Premium Sound, Fortemedia SAM, Creative Host Audio, Synopsys Sonic Focus, DTS Surround Sensation | UltraPC, and DTS Connect licenses, the ALC888S-VD offers the highest sound quality, providing an excellent entertainment package and game experience for PC users.

The ALC888S-VD is an upgraded version of the ALC888S-VC, with lower power consumption. It also features a built-in Low-dropout (LDO) regulator to reduce customer's external circuit cost.

2. Features

2.1. Hardware Features

- DACs with 97dB SNR (A-weighting), ADCs with 90dB SNR (A-weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 channel sound playback, plus 2 channels of concurrent independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format, multiple stereo recording
- All DACs supports 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 44.1k/48k/96k/192kHz sample rate
- Primary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- Secondary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- 16/20/24-bit SPDIF-IN supports 44.1k/48k/96k/192kHz sample rate
- All analog jacks (port-A to port-G) are stereo input and output re-tasking
- Port-D/E/F built-in headphone amplifiers
- Port-B/C/E/F with software selectable boost gain (+10/+20/+30dB) for analog microphone input
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.2V/4.0V VREFOUT
- Up to four channels of microphone array input are supported for AEC/BF applications
- Two jack detection pins each designed to detect up to 4 jacks
- Supports legacy analog mixer architecture
- Up to two GPIOs (General Purpose Input and Output) for customized applications. GPIO0 and GPIO1 share pin with DMIC-CLK and DMIC-DATA
- Supports mono and stereo digital microphone interface (pins shared with GPIO0 and GPIO1)
- Supports anti-pop mode when analog power LDO-IN is on and digital power is off
- 1dB per step output volume and input volume control
- Supports 3.3V digital core power, 1.5V or 3.3V digital I/O power for HD Audio link, and 5.0V analog power

- Intel low power ECR compliant and power status control for each analog/digital converter and pin widget
- Built-in Low-dropout (LDO) regulator
- Ultra low power consumption in anti-pop mode
- 48-pin LQFP ‘Green’ package

2.2. Software Features

- Meets Microsoft WLP 3.x and future WLP audio requirements
- WaveRT-based audio function driver for Windows Vista and Windows 7
- Direct Sound 3D™ compatible
- I3DL2 compatible
- 7.1+2 channel multi-streaming enables concurrent gaming/VoIP
- Emulation of 26 sound environments to enhance gaming experience
- Multiband software equalizer and tools provided
- Voice Cancellation and Key Shifting effect
- Dynamic range control (expander, compressor, and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice applications
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Optional Dolby PCEE program, SRS TruSurround HD, SRS Premium Sound, Fortemedia SAM, Creative Host Audio, Synopsys Sonic Focus, DTS Surround Sensation | UltraPC, and DTS Connect licenses

3. System Applications

- Desktop multimedia PCs
- Notebook PCs

4. Block Diagram

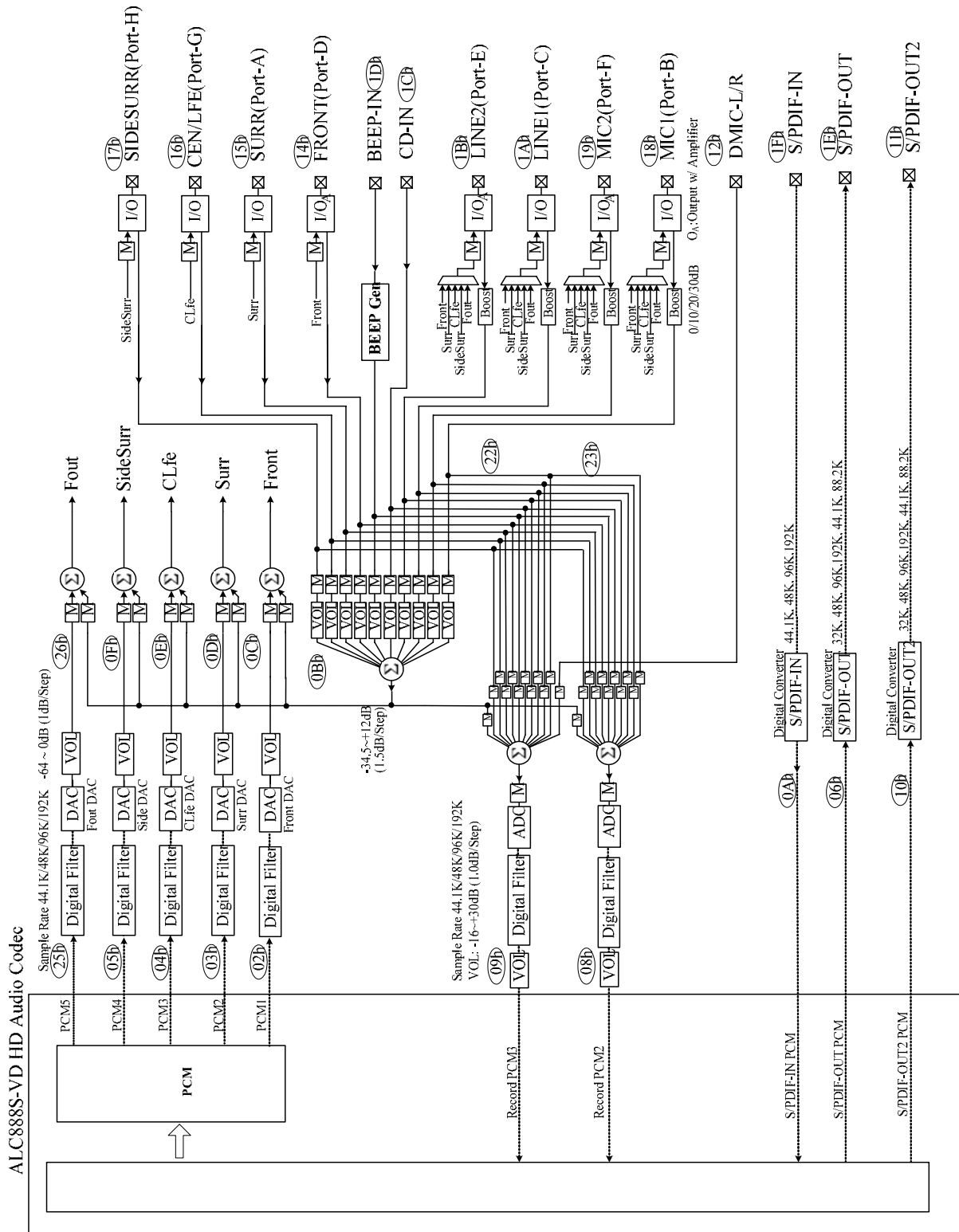


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin Complex widgets NID=14h~1Bh are re-tasking IOs.

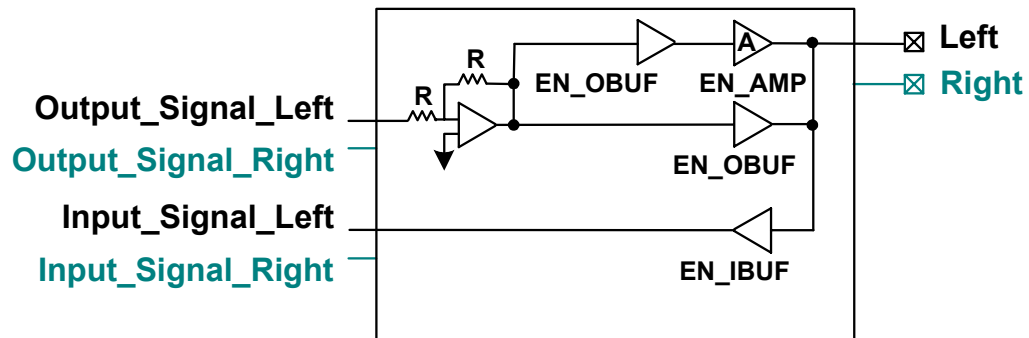


Figure 2. Analog Input/Output Unit

5. Pin Assignments

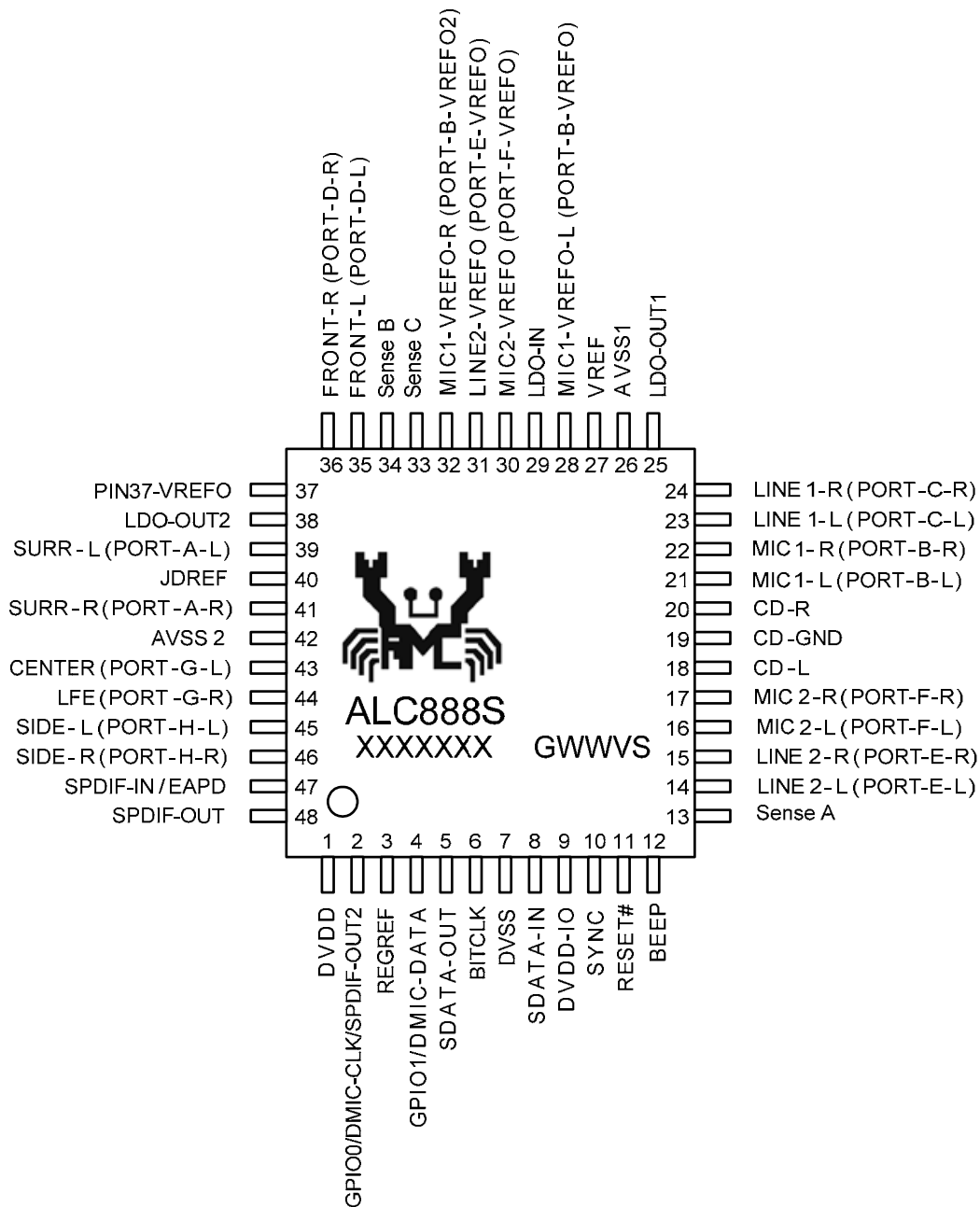


Figure 3. Pin Assignments

5.1. Package and Version Identification

Green package is indicated by the 'G' in GWWVS (Figure 3). The silicon version and step numbers are shown in the location marked 'V' and 'S'.

6. Pin Descriptions

For a convenient list of ALC888S-VD vs. ALC888S-VC pin differences, see section 6.2, page 10.

6.1. Pin Description Table

Table 1. Pin Descriptions

| Name | Type | Pin | Description | Characteristic Definition |
|-----------------------------------|-----------------|-----|--|---|
| DVDD | P | 1 | Digital Core Power | Digital VDD (3.3V) |
| GPI00/ DMIC-CLK/ SPDIF-OUT2 | IO ¹ | 2 | General Purpose Input/Output/ Digital MIC Clock Output/ Secondary SPDIF Out to HDMI Transmitter | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD$, $V_{IH} = 0.6 \times DVDD$, internal 50K pull up Digital Output: $V_{OL} < 0.1 \times DVDD$, $V_{OH} > 0.9 \times DVDD$ 6mA@75Ω Output driving |
| REGREF | - | 3 | Reference for Integrated Regulator | 10μF capacitor to digital ground |
| GPI01/ DMIC-DATA | IO ¹ | 4 | General Purpose Input/Output/ Digital MIC Stereo Channel Input | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD$, $V_{IH} = 0.6 \times DVDD$, internal 50K pull up Digital Output: $V_{OL} < 0.1 \times DVDD$, $V_{OH} > 0.9 \times DVDD$ |
| SDATA-OUT | I | 5 | Serial TDM Data Input | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD-IO$, $V_{IH} = 0.6 \times DVDD-IO$ |
| BITCLK | I | 6 | 24MHz Clock | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD-IO$, $V_{IH} = 0.6 \times DVDD-IO$ |
| DVSS | G | 7 | Digital Ground | Digital ground |
| SDATA-IN | IO | 8 | Serial TDM Data Output | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD-IO$, $V_{IH} = 0.6 \times DVDD-IO$ Digital Output: $V_{OL} < 0.1 \times DVDD-IO$, $V_{OH} > 0.9 \times DVDD-IO$ |
| DVDD-IO | P | 9 | Digital Power for HD Link | Scalable Digital VDD (1.5V~3.3V) |
| SYNC | I | 10 | 48KHz Frame SYNC Signal | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD-IO$, $V_{IH} = 0.6 \times DVDD-IO$ |
| RESET# | I | 11 | H/W Reset Input | Digital Input: Schmitt trigger, $V_{IL} = 0.4 \times DVDD-IO$, $V_{IH} = 0.6 \times DVDD-IO$ |
| BEEP | I | 12 | External PC Beep Input | Analog Input: 1.6Vrms of full-scale input |
| Sense A | - | 13 | Jack Detect for Resistor Network | Connector {5.1K, 10K, 20K, 39.2K} with 1% accuracy |
| LINE2-L | IO | 14 | Analog Input and Output with Multiple Function (Left) | Analog I/O (PORT-E-L), default 2 nd line input. Recommended to be re-tasking port at front panel |
| LINE2-R | IO | 15 | Analog Input and Output with Multiple Function (Right) | Analog I/O (PORT-E-R), default 2 nd line input. Recommended to be re-tasking port at front panel |
| MIC2-L | IO | 16 | Analog Input and Output with Multiple Function (Left) | Analog I/O (PORT-F-L), default 2 nd mic input. Recommended to be re-tasking port at front panel |

| Name | Type | Pin | Description | Characteristic Definition |
|--------------|------|-----|--|---|
| MIC2-R | IO | 17 | Analog Input and Output with Multiple Function (Right) | Analog I/O (PORT-F-R), default 2 nd mic input. Recommended to be re-tasking port at front panel |
| CD-L | I | 18 | CD Input Left Channel | Analog Input: 1.6Vrms of full-scale input |
| CD-GND | I | 19 | CD Input Reference Ground | Analog Input: 1.6Vrms of full-scale input |
| CD-R | I | 20 | CD Input Right Channel | Analog Input: 1.6Vrms of full-scale input |
| MIC1-L | IO | 21 | Analog Input and Output with Multiple Function (Left) | Analog I/O (PORT-B-L), default 1 st mic input. Recommended to be microphone input at rear panel |
| MIC1-R | IO | 22 | Analog Input and Output with Multiple Function (Right) | Analog I/O (PORT-B-R), default 1 st mic input. Recommended to be microphone input at rear panel |
| LINE1-L | IO | 23 | Analog Input and Output with Multiple Function (Left) | Analog I/O (PORT-C-L), default 1 st line input. Recommended to be line level input at rear panel |
| LINE1-R | IO | 24 | Analog Input and Output with Multiple Function (Right) | Analog I/O (PORT-C-R), default 1 st line input. Recommended to be line level input at rear panel |
| LDO-OUT1 | - | 25 | Built-In LDO Output for Mixer & Amp | Needs 10 μ F capacitor to analog ground, and short to Pin38 |
| AVSS1 | G | 26 | Analog Ground for Mixer & Amp | Analog GND |
| VREF | - | 27 | 0.5 \times LDO-OUT1 Reference Voltage | 10 μ F capacitor to analog ground |
| MIC1-VREFO-L | O | 28 | Bias Voltage for MIC1 (Port-B) | Analog Output: 2.5V/3.2V/4.0V reference voltage |
| LDO-IN | P | 29 | Built-In LDO Input | VDD (5V) |
| MIC2-VREFO | O | 30 | Bias Voltage for MIC2 (Port-F) | Analog Output: 2.5V/3.2V/4.0V reference voltage |
| LINE2-VREFO | O | 31 | Bias Voltage for LINE2 (Port-E) | Analog Output: 2.5V/3.2V/4.0V reference voltage |
| MIC1-VREFO-R | O | 32 | Secondary Bias Voltage for MIC1 (Port-B) | Analog Output: 2.5V/3.2V/4.0V reference voltage |
| Sense C | - | 33 | Jack Detect for Resistor Network | Connector {5.1K, 10K, 20K, 39.2K} with 1% accuracy |
| Sense B | - | 34 | Jack Detect for Resistor Network | Connector {5.1K, 10K, 20K, 39.2K} with 1% accuracy |
| FRONT-L | IO | 35 | Analog Input and Output (Left) | Analog I/O (PORT-D-L), default front channel output |
| FRONT-R | IO | 36 | Analog Input and Output (Right) | Analog I/O (PORT-D-R), default front channel output |
| PIN37-VREFO | O | 37 | Bias Voltage | Analog Output: 2.5V/3.2V/4.0V reference voltage |
| LDO-OUT2 | - | 38 | Analog Power for DAC and ADC | Needs 10 μ F capacitor to analog ground, and short to Pin25 |
| SURR-L | IO | 39 | Analog Input and Output (Left) | Analog I/O (PORT-A-L), default surround channel |
| JDREF | - | 40 | Reference for Jack Detect | 20K, 1% resistor to AGND |
| SURR-R | IO | 41 | Analog Input and Output (Right) | Analog I/O (PORT-A-R), default surround channel |

| Name | Type | Pin | Description | Characteristic Definition |
|---------------|------|-----|---|---|
| AVSS2 | G | 42 | Analog Ground for DAC & ADC | Analog GND |
| CENTER | IO | 43 | Analog Input and Output (Left) | Analog I/O (PORT-G-L), default center channel |
| LFE | IO | 44 | Analog Input and Output (Right) | Analog I/O (PORT-G-R), default LFE channel |
| SIDE-L | IO | 45 | Analog Input and Output (Left) | Analog I/O (PORT-H-L), default side channel |
| SIDE-R | IO | 46 | Analog Input and Output (Right) | Analog I/O (PORT-H-R), default side channel |
| SPDIF-IN/EAPD | IO | 47 | SPDIF Input/ External Amplifier Power Down | Digital Input: Schmitt trigger (5V tolerance), $V_{IL} = 0.44 \times DVDD$, $V_{IH} = 0.56 \times DVDD$ Digital Output: $V_{OL} < 0.1 \times DVDD$, $V_{OH} > 0.9 \times DVDD$ |
| SPDIF-OUT | O | 48 | Primary SPDIF Out | Digital Output: $V_{OL} < 0.1 \times DVDD$, $V_{OH} > 0.9 \times DVDD$ 10mA@75Ω Output driving |
| | | | | Total: 48 Pins |

Note1: Pins 2 and 4 have multiple functions. Their default operation is as GPIOs. They function as digital MIC pins when the configuration register of the digital MIC pin widget (node ID12h) is enabled, and exclusively function as secondary SPDIF-OUT when the configuration register of the SPDIF-OUT2 pin widget (node ID 11h) is enabled.

6.2. Pin Differences: ALC888S-VD vs. ALC888S-VC

Table 2. Pin Differences: ALC888S-VD vs. ALC888S-VC

| Pin Number | ALC888S-VD | ALC888S-VC | Description for ALC888S-VD |
|------------|-------------------------------|----------------|---|
| Pin 2 | GPIO0/DMIC-CLK /SPDIF-OUT2 | SPDIFO2 | Pin 2 is re-designed as a share pin to support secondary SPDIF-OUT, GPIO, and digital microphone interface. |
| Pin 3(*) | REGREF | GPIO0/DMIC-CLK | Pin 3 is used as reference for the integrated regulator. |
| Pin 25 | LDO-OUT1 | AVDD1 | LDO output1; must be shorted to Pin38 |
| Pin 29(*) | LDO-IN | LINE1-VREFO | Pin 29 is used as VDD input for the built-in LDO. |
| Pin 38 | LDO-OUT2 | AVDD2 | LDO output2; must be shorted to Pin25 |

(*) Please notice external circuit connected to pin3/pin29 if ALC888S-VD is directly mounted on C version layout.

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

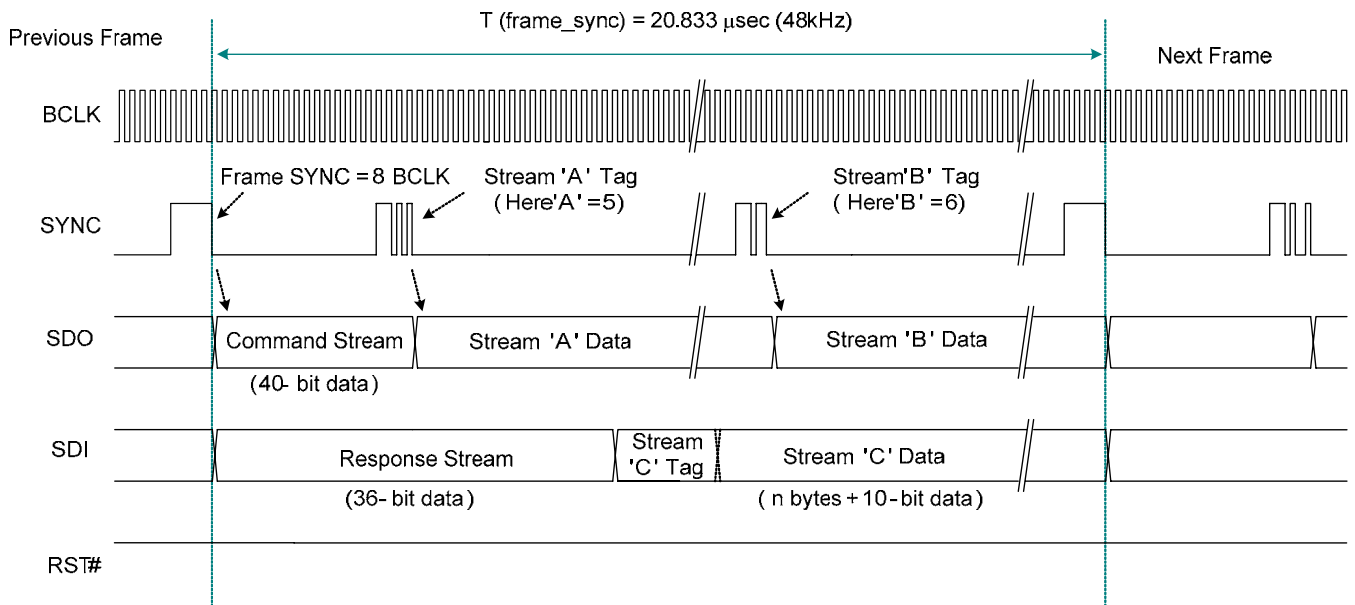


Figure 4. HDA Link Protocol

7.1.1. Link Signal Definitions

Table 3. Link Signal Definitions

| Item | Description |
|------|--|
| BCLK | 24.0MHz bit clock sourced from the HDA controller and connecting to all codecs |
| SYNC | 48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs |
| SDO | Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported |
| SDI | Serial data input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID |
| RST# | Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs |

Table 4. HDA Signal Definitions

| Signal Name | Source | Type for Controller | Description |
|-------------|------------------|---------------------|---|
| BCLK | Controller | Output | Global 24.0MHz Bit Clock |
| SYNC | Controller | Output | Global 48kHz Frame Sync and Outbound Tag Signal |
| SDO | Controller | Output | Serial Data Output from the Controller |
| SDI | Codec/Controller | Input/Output | Serial Data Input from Codec. Weakly pulled down by the controller |
| RST# | Controller | Output | Global Active Low Reset Signal |

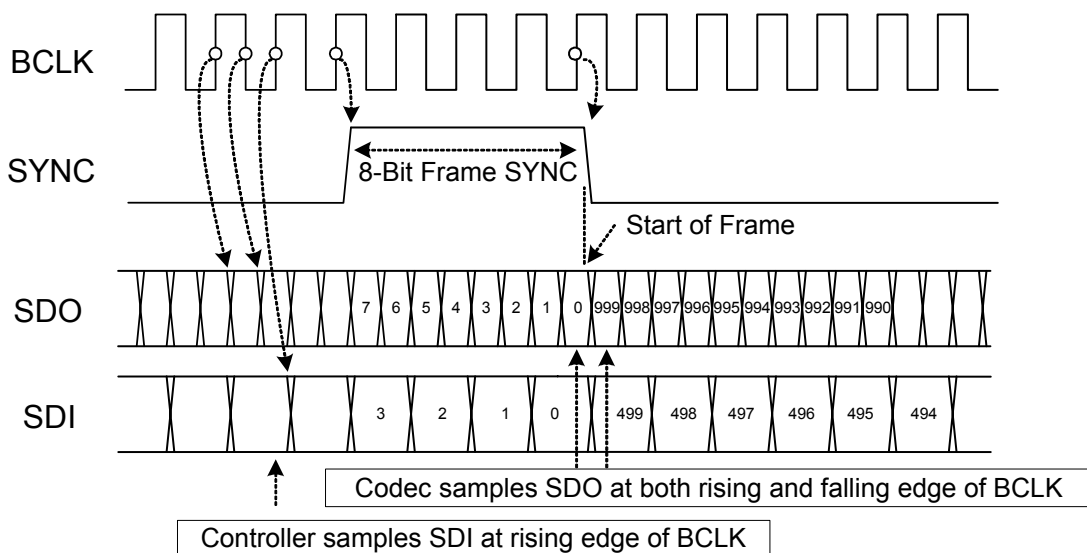


Figure 5. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0, and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 14 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC888S-VD is designed to receive a single SDO stream.

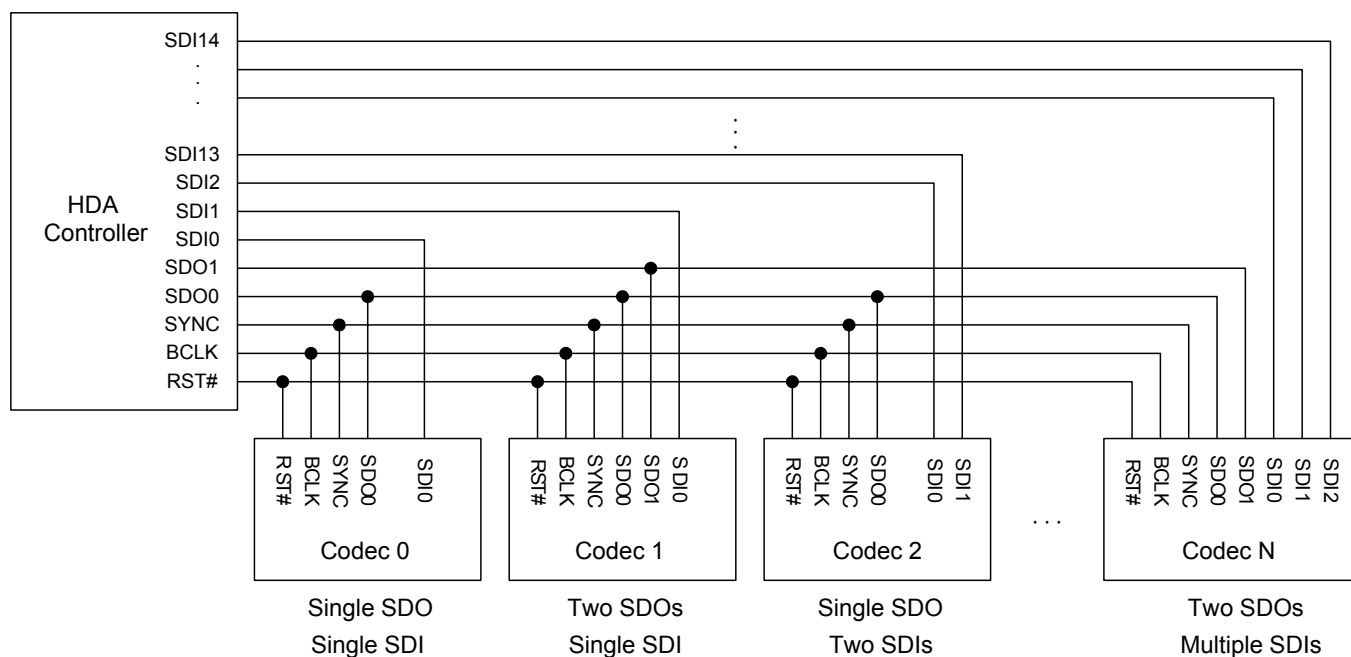


Figure 6. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be two blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

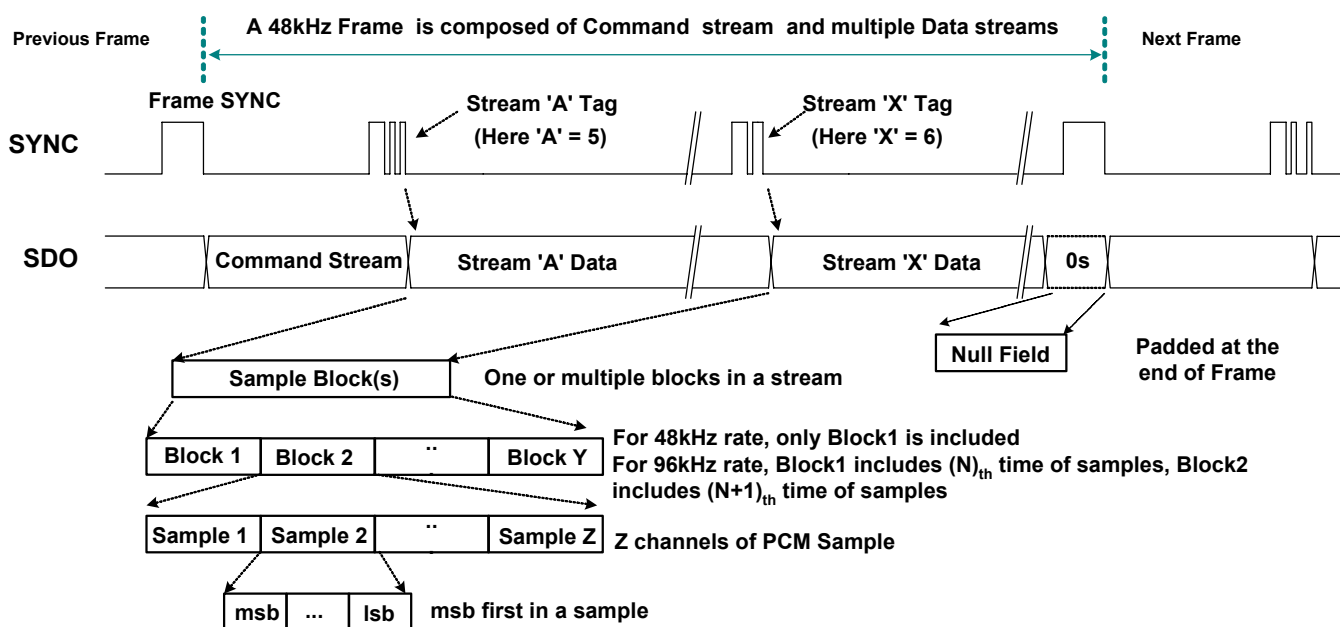


Figure 7. SDO Outbound Frame

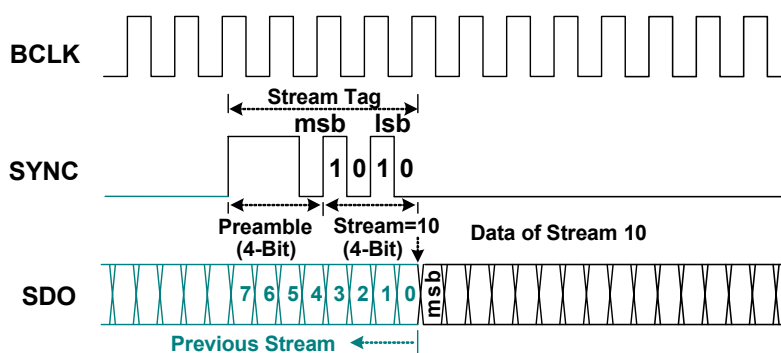


Figure 8. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the ‘Stripe Control’ bit in the controller’s Output Stream Control Register to initiate a specific stream (Stream ‘A’ in Figure 9) to be transmitted on multiple SDOs. In this case, the MSB of the data stream is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

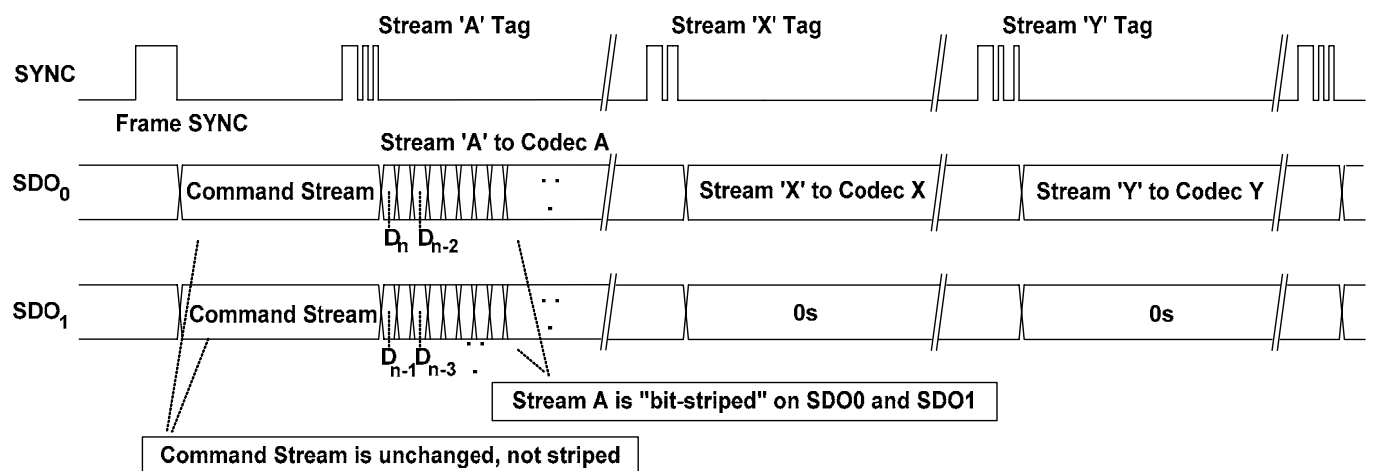


Figure 9. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), the SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK.

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 11).

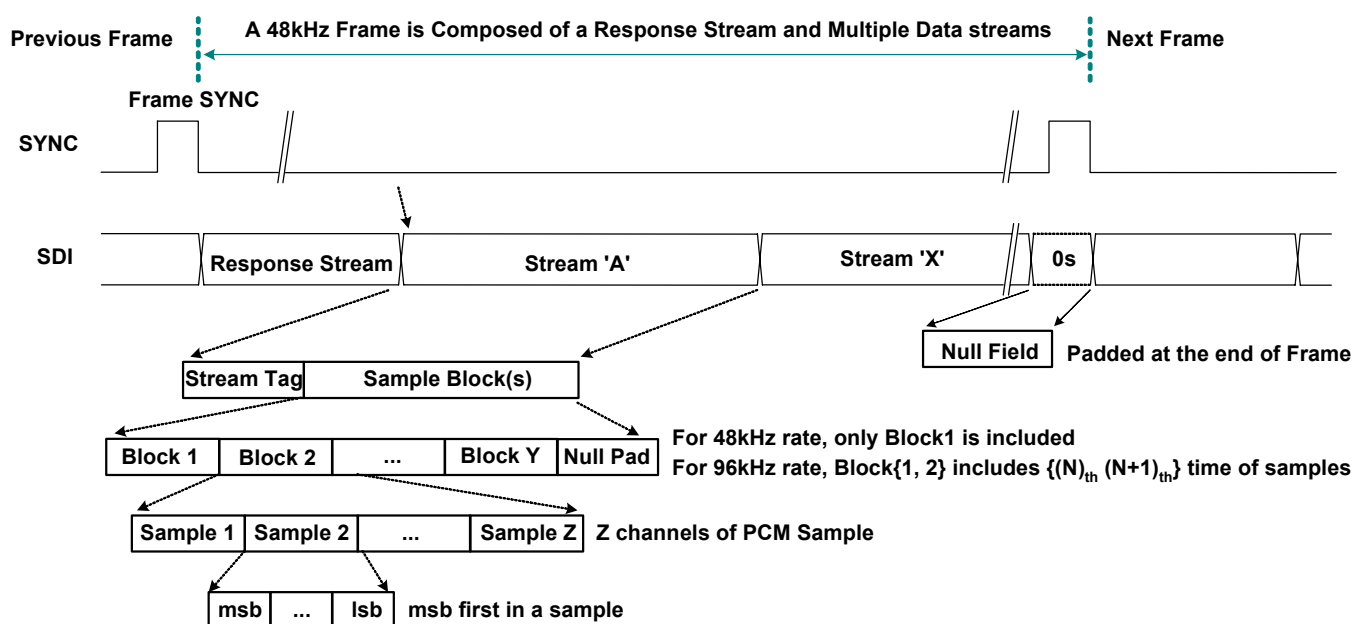


Figure 10. SDI Inbound Stream

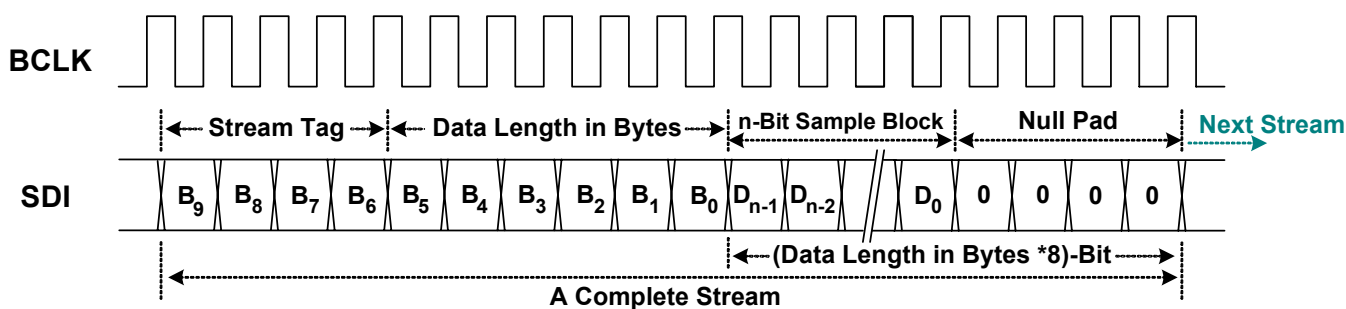


Figure 11. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data into separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

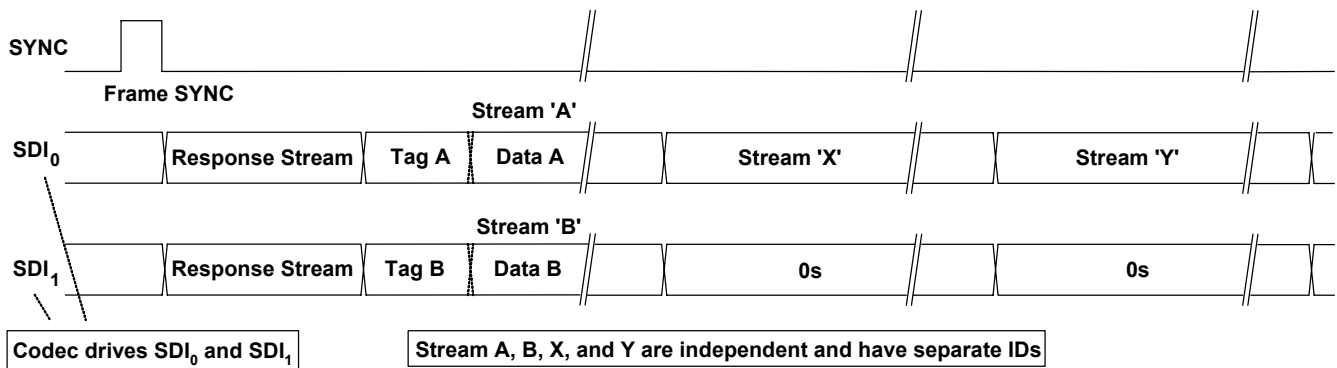


Figure 12. Codec Transmits Data Over Multiple SDIs

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 5, page 18, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 6, page 18, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence ‘12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)’ interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 7, page 19).

Table 5. Defined Sample Rate and Transmission Rate

| (Sub) Multiple | 48kHz Base | 44.1kHz Base |
|----------------|--|---|
| 1/6 | 8kHz (1 Sample Block Every 6 Frames) | - |
| 1/4 | 12kHz (1 Sample Block Every 4 Frames) | 11.025kHz (1 Sample Block Every 4 Frames) |
| 1/3 | 16kHz (1 Sample Block Every 3 Frames) | - |
| 1/2 | - | 22.05kHz (1 Sample Block Every 2 Frames) |
| 2/3 | 32kHz (2 Sample Blocks Every 3 Frames) | - |
| 1 | 48kHz (1 Sample Block per Frame) | 44.1kHz (1 Sample Block per Frame) |
| 2 | 96kHz (2 Sample Blocks per Frame) | 88.2kHz (2 Sample Blocks per Frame) |
| 4 | 192kHz (4 Sample Blocks per Frame) | 176.4kHz (4 Sample Blocks per Frame) |

Table 6. 48kHz Variable Rate of Delivery Timing

| Rate | Delivery Cadence | Description |
|--------|----------------------------|---|
| 8kHz | YNNNNN (Repeat) | One Sample Block is Transmitted in Every 6 Frames |
| 12kHz | YNNN (Repeat) | One Sample Block is Transmitted in Every 4 Frames |
| 16kHz | YNN (Repeat) | One Sample Block is Transmitted in Every 3 Frames |
| 32kHz | Y ² NN (Repeat) | Two Sample Blocks are Transmitted in Every 3 Frames |
| 48kHz | Y (Repeat) | One Sample Block is Transmitted in Every Frame |
| 96kHz | Y ² (Repeat) | Two Sample Blocks are Transmitted in Each Frame |
| 192kHz | Y ⁴ (Repeat) | Four Sample Blocks Are Transmitted In Each Frame |

N: No sample block in a frame.

Y: One sample block in a frame.

Y^x: X sample blocks in a frame.

Table 7. 44.1kHz Variable Rate of Delivery Timing

| Rate | Delivery Cadence |
|-----------|---|
| 11.025kHz | {12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-}{11}{-} |
| 22.05kHz | {12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-}{11}{-} |
| 44.1kHz | 12-11-11-12-11-11-12-11-11-12-11-11-11- (Repeat) |
| 88.2kHz | 12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² -12 ² -11 ² -11 ² - (Repeat) |
| 176.4kHz | 12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ -12 ⁴ -11 ⁴ -11 ⁴ - (Repeat) |

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNY
 {11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNY
 {-}=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYNYNYNYN
 {11}=YNYNYNYNYNYNYNYNYNYNYNYNYNYN
 {-}=NN

44.1kHz 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.
 88.2kHz 12²- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.
 176.4kHz 12⁴- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

- Link Reset
- Codec Reset
- Codec changes its power state (for example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the ‘CRST’ bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 13, shows the ‘Link Reset’ timing including the ‘Enter’ sequence (❶~❺) and ‘Exit’ sequence (❻~❾)

Enter ‘Link Reset’:

- ❶ Software writes a 0 to the ‘CRST’ bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ When the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RST# signal to low, and enters the ‘Link Reset’ state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from ‘Link Reset’:

- ⑥ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)
- ⑦ Software is responsible for de-asserting RST# after a minimum of 100µs BCLK running time (the 100µsec provides time for the codec PLL to stabilize)
- ⑧ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC
- ⑨ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

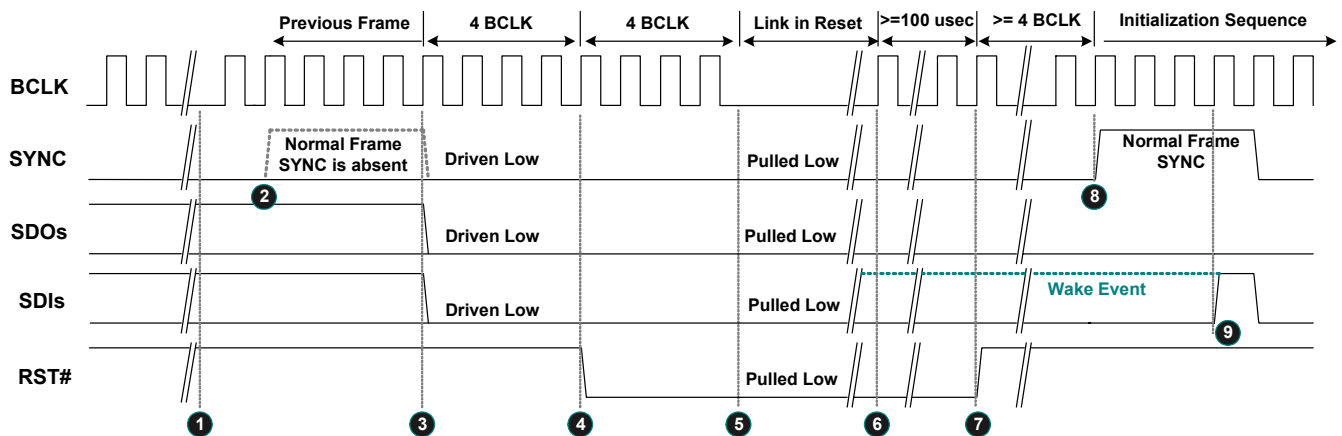


Figure 13. Link Reset Timing

7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec will stop driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operation state

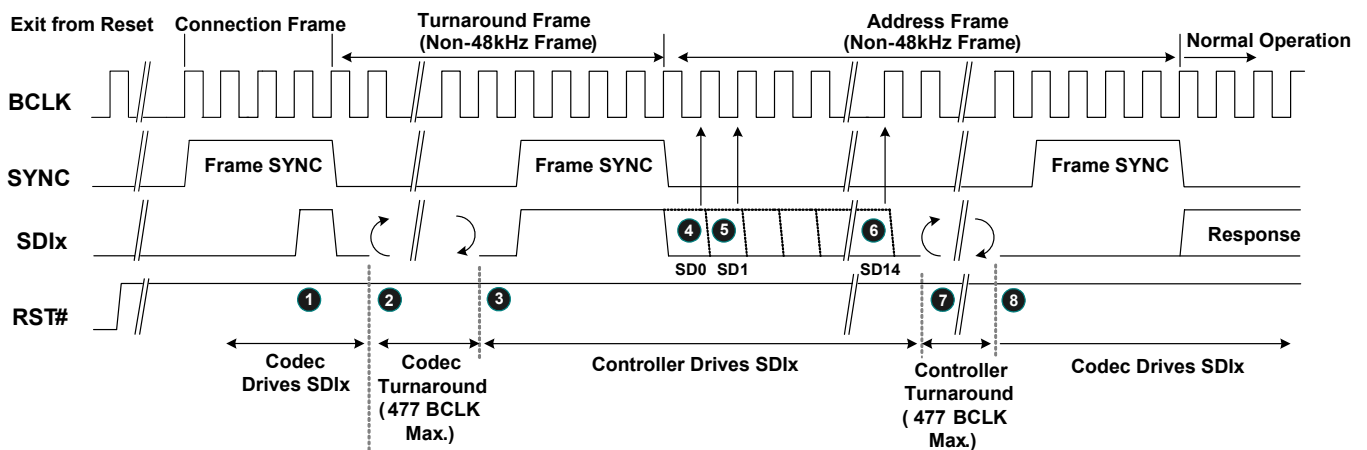


Figure 14. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 8 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 9 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 8. 40-Bit Commands in 4-Bit Verb Format

| Bit [39:32] | Bit [31:28] | Bit [27:20] | Bit [19:16] | Bit [15:0] |
|-------------|---------------|-------------|-------------|------------|
| Reserved | Codec Address | Node ID | Verb ID | Payload |

Table 9. 40-Bit Commands in 12-Bit Verb Format

| Bit [39:32] | Bit [31:28] | Bit [27:20] | Bit [19:8] | Bit [7:0] |
|-------------|---------------|-------------|------------|-----------|
| Reserved | Codec Address | Node ID | Verb ID | Payload |

Table 10. Verbs Supported by the ALC888S-VD (Y=Supported)

| Supported Verb | Get Verb | Set Verb | Root Node | Audio Function Group | Modem Function Group ^{*1} | HDMI Function Group ^{*1} | Vendor Defined Group ^{*1} | Audio Out Converter | Audio In Converter | Pin Widget | Sum Widget | Selector Widget | Power Widget ^{*1} | Volume Knob | Beep Generator | Vendor Defined Widget |
|---------------------------|-------------|-------------|-----------|----------------------|------------------------------------|-----------------------------------|------------------------------------|---------------------|--------------------|------------|------------|-----------------|----------------------------|-------------|----------------|-----------------------|
| Get Parameter | F00 | - | Y | Y | - | - | - | Y | Y | Y | Y | Y | - | Y | Y | Y |
| Connection Select | F01 | 701 | - | - | - | - | - | - | Y | Y | - | Y | - | - | - | - |
| Get Connection List Entry | F02 | - | - | - | - | - | - | - | Y | Y | Y | Y | - | - | - | - |
| Processing State | F03 | 703 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Coefficient Index | D- | 5- | - | - | - | - | - | - | - | - | - | - | - | - | - | Y |
| Processing Coefficient | C- | 4- | - | - | - | - | - | - | - | - | - | - | - | - | - | Y |
| Amplifier Gain/Mute | B- | 3- | - | - | - | - | - | - | Y | Y | Y | - | - | - | - | - |
| Stream Format | A- | 2- | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Digital Converter 1 | F0D | 70D | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Digital Converter 2 | F0D | 70E | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Digital Converter 3 | F3E | 73E | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Digital Converter 4 | F3F | 73F | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Power State | F05 | 705 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Channel/Stream ID | F06 | 706 | - | - | - | - | - | Y | Y | - | - | - | - | - | - | - |
| SDI Select | F04 | 704 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Pin Widget Control | F07 | 707 | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| Unsolicited Enable | F08 | 708 | - | - | - | - | - | - | - | Y | - | - | - | Y | - | - |
| Pin Sense | F09 | 709 | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| EAPD/BTL Enable | F0C | 70C | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| All GPIO Control | F15~ F19 | 715~ 719 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Beep Generator Control | F0A | 70A | - | - | - | - | - | - | - | - | - | - | - | - | Y | - |
| Volume Knob Control | F0F | 70F | - | - | - | - | - | - | - | - | - | - | - | Y | - | - |
| Subsystem ID, Byte 0 | F20 | 720 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Subsystem ID, Byte 1 | F20 | 721 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Subsystem ID, Byte 2 | F20 | 722 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Subsystem ID, Byte 3 | F20 | 723 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Config Default, Byte 0 | F1C | 71C | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| Config Default, Byte 1 | F1C | 71D | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| Config Default, Byte 2 | F1C | 71E | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| Config Default, Byte 3 | F1C | 71F | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| RESET | - | 7FF | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |

^{*1}: The ALC888S-VD does not support Modem Function, HDMI Function, Vendor Defined Groups, and Power Widgets.

Table 11. Parameters in the ALC888S-VD (Y=Supported)

| Supported Parameter | Parameter ID | Root Node | Audio Function Group | Modem Function Group ^{*1} | HDMI Function Group ^{*1} | Vendor Defined Group ^{*1} | Audio Out Converter | Audio In Converter | Pin Widget | Sum Widget | Selector Widget | Power Widget ^{*1} | Volume Knob | Beep Generator | Vendor Defined Widget |
|-----------------------------------|--------------|-----------|----------------------|------------------------------------|-----------------------------------|------------------------------------|---------------------|--------------------|------------|------------|-----------------|----------------------------|-------------|----------------|-----------------------|
| Vendor ID | 00 | Y | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Revision ID | 02 | Y | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Subordinate Node Count | 04 | Y | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Function Group Type | 05 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Audio Function Group Capabilities | 08 | - | Y | - | - | - | - | - | - | - | - | - | - | - | - |
| Audio Widget Capabilities | 09 | - | - | - | - | - | Y | Y | Y | Y | Y | - | Y | Y | Y |
| Sample Size, Rate | 0A | - | Y | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Stream Formats | 0B | - | Y | - | - | - | Y | Y | - | - | - | - | - | - | - |
| Pin Capabilities | 0C | - | - | - | - | - | - | - | Y | - | - | - | - | - | - |
| Input Amp Capabilities | 0D | - | - | - | - | - | - | Y | - | Y | Y | - | - | - | - |
| Output Amp Capabilities | 12 | - | - | - | - | - | - | - | Y | Y | - | - | - | - | - |
| Connection List Length | 0E | - | - | - | - | - | - | Y | Y | Y | Y | - | - | - | - |
| Supported Power States | 0F | - | Y | - | - | - | Y | Y | Y | Y | Y | - | - | - | Y |
| Processing Capabilities | 10 | - | - | - | - | - | - | - | - | - | - | - | - | - | Y |
| GPIO Count | 11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Volume Knob Capabilities | 13 | - | - | - | - | - | - | - | - | - | - | - | Y | - | - |

^{*1}: The ALC888S-VD does not support Modem Function, HDMI Function, Vendor Defined Groups, and Power Widgets.

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The ‘Tag’ in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:0] |
|----------|----------|-------------|------------|
| Valid | Unsol=0 | Reserved | Response |

Table 13. Unsolicited Response Format

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:28] | Bit [27:0] |
|----------|----------|-------------|-------------|------------|
| Valid | Unsol=1 | Reserved | Tag | Response |

Note: The response stream in the link protocol is 36-bit wide. The response is placed in the lower 32-bit field. Bit 35 is a ‘Valid’ bit to indicate the response is ‘Ready’. Bit 34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions. To simplify power management in the ALC888S-VD, only the Audio Function (NID=01h) supports power control. Output converters (DACs) and input converters (ADCs) have no individual power control. Software can configure whole codec power states through the audio function (NID=01h). Software may have various power states depending on system configuration.

Table 15 indicates those nodes that support power management.

7.5.1. System Power State Definitions

Table 14. System Power State Definitions

| Power States | Definitions |
|--------------|--|
| D0 | All Power On. Individual DACs and ADCs can be powered up or down as required. |
| D1 | All Converters (DACs and ADCs) are Powered Down. State maintained, analog reference stays up. |
| D2 | Power is Still Supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection and GPI are powered down. |
| D3 (Hot) | Power is Still Supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection/GPI work. |
| D3 (Cold) | Power is Still Supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection/GPI work when internal OSC powers up. |

7.5.2. Power Controls in NID 01h

Table 15. Power Controls in NID 01h

| Item | Description | D0 | D1 | D2 | D3 | Link Reset |
|-----------------------------|---|--------|--------|--------|--------|---------------------|
| Audio Function (NID=01h) | HD LINK State | Normal | Normal | Normal | Normal | PD |
| | Front DAC (NID-02h) | Normal | PD | PD | PD | PD |
| | Surr DAC (NID-03h) | Normal | PD | PD | PD | PD |
| | Cen/Lfe DAC (NID-04h) | Normal | PD | PD | PD | PD |
| | Side DAC (NID-05h) | Normal | PD | PD | PD | PD |
| | Fout DAC (NID-25h) | Normal | PD | PD | PD | PD |
| | LINE ADC (NID-08h) | Normal | PD | PD | PD | PD |
| | MIX ADC (NID-09h) | Normal | PD | PD | PD | PD |
| | All Headphone Drivers | Normal | Normal | PD | PD | PD |
| | All Mixers | Normal | Normal | PD | PD | PD |
| | All Reference | Normal | Normal | Normal | Normal | Normal |
| | Jack Detection with Unsolicited Response | Normal | Normal | PD | Normal | Normal ² |

Note 1: PD=Powered Down.

Note 2: Jack detection with unsolicited response is issued when a Link Reset occurs in D3 state.

7.5.3. Powered Down Conditions

Table 16. Powered Down Conditions

| Condition | Description |
|-------------------------------|---|
| LINK Response Powered Down | Internal Clock is Stopped. SDATA-IN and SPDIF-OUT are floated with internally pulled low 47K resistors. SPDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences is supported. All states are maintained if DVDD is supplied. |
| FRONT DAC Powered Down | Analog Block and Digital Filter are Powered Down. |
| SURR DAC Powered Down | Analog Block and Digital Filter are Powered Down. |
| CEN/LFE DAC Powered Down | Analog Block and Digital Filter are Powered Down. |
| SIDESURR DAC Powered Down | Analog Block and Digital Filter are Powered Down. |
| FOUT DAC Powered Down | Analog Block and Digital Filter are Powered Down. |
| LINE ADC Powered Down | Analog Block and Digital Filter are Powered Down. Data on SDATA-IN is quiet. |
| MIX ADC Powered Down | Analog Block and Digital Filter are Powered Down. Data on SDATA-IN is quiet. |
| Headphone Driver Powered Down | All Headphone Drivers are Powered Down. |
| Mixers Powered Down | All Internal Mixer Widgets are Powered Down. The DC reference and VREFOUTx at individual pin complexes are still alive. |
| Reference Power Down | All Internal References, DC Reference, and VREFOUTx at Individual Pin Complexes are Off. |

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC888S-VD. If a verb is not supported by the addressed widget, it will respond with 32 bits of ‘0’.

8.1. Verb – Get Parameters (Verb ID=F00h)

The ‘Get Parameters’ verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget. Some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, page 22, for detailed information about supported parameters.

Table 17. Verb – Get Parameters (Verb ID=F00h)

| Get Parameter Command Format | | | | Codec Response Format |
|------------------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=00h | Verb ID=F00h | Parameter ID[7:0] | 32-bit Response |

Note: If the parameter ID is not supported, the returned response is 32 bits of ‘0’.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

| Codec Response Format | |
|-----------------------|--|
| Bit | Description |
| 31:16 | Vendor ID=10ECh (Realtek’s PCI Vendor ID). |
| 15:0 | Device ID=0888h. |

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 19. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

| Codec Response Format | |
|-----------------------|---|
| Bit | Description |
| 31:24 | Reserved. Read as 0’s. |
| 23:20 | MajRev. The major version number (in decimal) of the HDA Spec to which the ALC888S-VD is fully compliant. Response=0x1. |
| 19:16 | MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC888S-VD is fully compliant. Response=0x0. |
| 15:8 | Revision ID. The vendor’s revision number. 00h is for the first silicon version (A version), 01h is for the second version (B version), etc. |
| 7:0 | Stepping ID. The vendor’s stepping number within the given Revision ID. |

Note: The Root Node (NID=00h in the ALC888S-VD) supports this parameter.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

Table 20. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31:24 | Reserved. Read as 0's. |
| 23:16 | Starting Node Number. The starting node number in the sequential widgets. |
| 15:8 | Reserved. Read as 0's. |
| 7:0 | Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group. |

| | Description | Reserved | Starting Node | Reserved | Total Fun/Widgets |
|----------------|-----------------------------------|-------------|---------------|------------|-------------------|
| | Bits → | Bit [31:24] | Bit [23:16] | Bit [15:8] | Bit [7:0] |
| Root Node | NID=00h | - | 01h | - | 01h |
| Audio Function | NID=01h | - | 02h | - | 25h |
| Others | Not Supported (Returns 00000000h) | | | | |

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 21. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

| Bit | Description |
|------|---|
| 31:9 | Reserved. Read as 0's. |
| 8 | UnSol Capable. Read as 1. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group |
| 7:0 | Function Group Type. Read as 01h. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function |

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 22. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31:17 | Reserved. Read as 0's. |
| 16 | Beep Generator. Read as 1. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group. |
| 15:12 | Reserved. Read as 0's. |
| 11:8 | Input Delay. Read as 0xF. |
| 7:4 | Reserved. Read as 0's. |
| 3:0 | Output Delay. Read as 0xF. |

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 23. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31:24 | Reserved. Read as 0's. |
| 23:20 | Widget Type. 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget |
| 19:16 | Delay. Samples delayed between the HDA link and widgets. |
| 15:11 | Reserved. Read as 0's. |
| 10 | Power Control. 0: Power state control is not supported on this widget 1: Power state is supported on this widget |
| 9 | Digital. 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (SPDIF, I ² S, etc.) |
| 8 | ConnList. Connection List. 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried |
| 7 | UnsolCap. Unsolicited Capable. 0: Unsolicited response is not supported 1: Unsolicited response is supported |
| 6 | ProcWidget. Processing Widget. 0: No processing control 1: Processing control is supported |
| 5 | Reserved. Read as 0. |
| 4 | Format Override. |
| 3 | AmpParOvr. AMP Param Override. |
| 2 | OutAmpPre. Out AMP Present. |
| 1 | InAmpPre. In AMP Present. |
| 0 | Stereo. 0: Mono Widget 1: Stereo Widget |

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameters here provide default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

Table 24. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

| Bit | Description |
|-------|--|
| 31:21 | Reserved. Read as 0's. |
| 20 | B32. 32-bit audio format support. 0: Not supported 1: Supported |
| 19 | B24. 24-bit audio format support. 0: Not supported 1: Supported |
| 18 | B20. 20-bit audio format support. 0: Not supported 1: Supported |
| 17 | B16. 16-bit audio format support. 0: Not supported 1: Supported |
| 16 | B8. 24-bit audio format support. 0: Not supported 1: Supported |
| 15:12 | Reserved. Read as 0's. |
| 11 | R12. 384kHz (=8×48kHz) rate support. 0: Not supported 1: Supported |
| 10 | R11. 192kHz (=4×48kHz) rate support. 0: Not supported 1: Supported |
| 9 | R10. 176.4kHz (=4×44.1kHz) rate support. 0: Not supported 1: Supported |
| 8 | R9. 96kHz (=2×48kHz) rate support. 0: Not supported 1: Supported |
| 7 | R8. 88.2kHz (=2×44.1kHz) rate support. 0: Not supported 1: Supported |
| 6 | R7. 48kHz rate support. 0: Not supported 1: Supported |
| 5 | R6. 44.1kHz rate support. 0: Not supported 1: Supported |
| 4 | R5. 32kHz (=2/3×48kHz) rate support. 0: Not supported 1: Supported |
| 3 | R4. 22.05kHz (=1/2×44.1kHz) rate support. 0: Not supported 1: Supported |
| 2 | R3. 16kHz (=1/3×48kHz) rate support. 0: Not supported 1: Supported |
| 1 | R2. 11.025kHz (=1/4×44.1kHz) rate support. 0: Not supported 1: Supported |
| 0 | R1. 8kHz (=1/6×48kHz) rate support. 0: Not supported 1: Supported |

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

Table 25. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

| Bit | Description |
|------|--|
| 31:3 | Reserved. Read as 0's. |
| 2 | AC3. 0: Not supported 1: Supported |
| 1 | Float32. 0: Not supported 1: Supported |
| 0 | PCM. 0: Not supported 1: Supported |

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 26. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

| Bit | Description | | | | | | | | | | | | | | |
|----------|--|-----|----------|--------|-----|------|---|---|----------|------|-----|----------|--------|-----|------|
| 31:16 | Reserved. Read as 0's | | | | | | | | | | | | | | |
| 15:8 | VREF Control Capability. ‘1’ in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of LDO-OUT1. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>7:6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Reserved</td> <td>100%</td> <td>80%</td> <td>Reserved</td> <td>Ground</td> <td>50%</td> <td>Hi-Z</td> </tr> </tbody> </table> | 7:6 | 5 | 4 | 3 | 2 | 1 | 0 | Reserved | 100% | 80% | Reserved | Ground | 50% | Hi-Z |
| 7:6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | |
| Reserved | 100% | 80% | Reserved | Ground | 50% | Hi-Z | | | | | | | | | |
| 7 | L-R Swap. Indicates the capability of swapping the left and right. | | | | | | | | | | | | | | |
| 6 | Balanced I/O Pin. ‘1’ indicates this pin complex has balanced pins. | | | | | | | | | | | | | | |
| 5 | Input Capable. ‘1’ indicates this pin complex supports input. | | | | | | | | | | | | | | |
| 4 | Output Capable. ‘1’ indicates this pin complex supports output. | | | | | | | | | | | | | | |
| 3 | Headphone Drive Capable. ‘1’ indicates this pin complex has an amplifier to drive a headphone. | | | | | | | | | | | | | | |
| 2 | Presence Detect Capable. ‘1’ indicates this pin complex can detect whether there is anything plugged in. | | | | | | | | | | | | | | |
| 1 | Trigger Required. ‘1’ indicates whether a software trigger is required for an impedance measurement. | | | | | | | | | | | | | | |
| 0 | Impedance Sense Capable. ‘1’ indicates this pin complex can perform analog sense on the attached device to determine its type. | | | | | | | | | | | | | | |

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 27. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

| Bit | Description |
|-------|--|
| 31 | (Input) Mute Capable. |
| 30:23 | Reserved. Read as 0. |
| 22:16 | Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB. |
| 15 | Reserved. Read as 0. |
| 14:8 | Number of Steps. Indicates the number of steps in the gain range. ‘0’ means the gain is fixed. |
| 7 | Reserved. Read as 0. |
| 6:0 | Offset. Indicates which step is 0dB. |

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

| Bit | Description |
|-------|--|
| 31 | (Output) Mute Capable. |
| 30:23 | Reserved. Read as 0. |
| 22:16 | Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB. |
| 15 | Reserved. Read as 0. |
| 14:8 | Number of Steps. Indicates the number of steps in the gain range. ‘0’ means the gain is fixed. |
| 7 | Reserved. Read as 0. |
| 6:0 | Offset. Indicates which step is 0dB. |

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 29. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0. |
| 7 | Short Form. 0: Short form 1: Long form |
| 6:0 | Connect List Length. Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (not a MUX widget). |

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 30. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

| Bit | Description |
|------|---|
| 31 | Extended Power States Supported (EPSS). 1: Extended power states EPSS is supported |
| 30 | CLKSTOP. 1: D3 mode operates even there is no BITCLK presents on the link |
| 29:4 | Reserved. Read as 0's. |
| 3 | D3Sup. 1: Power state D3 is supported |
| 2 | D2Sup. 1: Power state D2 is supported |
| 1 | D1Sup. 1: Power state D1 is supported |
| 0 | D0Sup. 1: Power state D0 is supported |

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 31. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31:16 | Reserved. Read as 0's. |
| 15:8 | NumCoeff. Number of Coefficient. |
| 7:1 | Reserved. Read as 0's. |
| 0 | Benign. 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant |

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 32. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

| Bit | Description |
|-------|---|
| 31 | GPIWake=0. The ALC888S-VD does not support GPIO wake up function. |
| 30 | GPIUnsol=1. The ALC888S-VD supports GPIO unsolicited response. |
| 29:24 | Reserved. Read as 0's. |
| 23:16 | NumGPIs=00h. No GPI pin is supported. |
| 15:8 | NumGPOs=00h. No GPO pin is supported. |
| 7:0 | NumGPIOs=02h. Two GPIO pins are supported. |

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 33. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

| Bit | Description |
|------|--|
| 31:8 | Reserved. Read as 0s. |
| 7 | Delta. Read as 0. 0: Software will not modify the volume in Volume Control Knob 1: Software can write a base volume to the Volume Control Knob |
| 6:0 | NumSteps. The total number of steps in the range of the Volume Control Knob (NID=21h) |

Note: The Volume Control knob (NID=21h) supports this parameter.

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 34. Verb – Get Connection Select Control (Verb ID=F01h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|-------------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F01h | 0's | Bit[7:0] are Connection Index |

Codec Response for Analog Port-B/C/E/F (NID=18h~1Bh)

| Bit | Description |
|------|---|
| 31:8 | 0's. |
| 7:0 | Connection Index Current Settings (Default Value is 00h). 00h: Sum Widget NID=0Ch 01h: Sum Widget NID=0Dh 02h: Sum Widget NID=0Eh 03h: Sum Widget NID=0Fh 04h: Sum Widget NID=26h Other: Reserved |

Codec Response for Digital Pin SPDIF-OUT (NID=1Eh)

| Bit | Description |
|------|--|
| 31:8 | 0's. |
| 7:0 | Connection Index Current Settings (Default Value is 00h). 00h: Digital Converter (SPDIF-OUT) NID=06h Other: Reserved |

Codec Response for Digital Pin SPDIF-OUT2 (NID=11h)

| Bit | Description |
|------|---|
| 31:8 | 0's. |
| 7:0 | Connection Index Current Settings (Default Value is 00h). 00h: Digital Converter (SPDIF-OUT2) NID=10h Other: Reserved |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 35. Verb – Set Connection Select (Verb ID=701h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=701h | Select Index [7:0] | 0's for All Nodes |

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 36. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-----------------------|
| CAd=X | Node ID=Xh | Verb ID=F02h | Offset Index - N[7:0] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=08h (LINE ADC)

| Bit | Description |
|------|---|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h. |
| 7:0 | Connection List Entry (N). Returns 23h (Sum Widget) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=09h (MIX ADC)

| Bit | Description |
|------|---|
| 15:8 | Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h. |
| 7:0 | Connection List Entry (N). Returns 22h (Sum Widget) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=0Ah (SPDIF-IN Converter)

| Bit | Description |
|------|--|
| 31:8 | Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h. |
| 7:0 | Connection List Entry (N). Returns 1Fh (SPDIF-IN Pin Widget) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=0Bh (Mixer)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 1Bh (Pin Complex – LINE2) for N=0~3. Returns 15h (Pin Complex-SURR) for N=4~7. Returns 00h for N>7. |
| 23:16 | Connection List Entry (N+2). Returns 1Ah (Pin Complex – LINE1) for N=0~3. Returns 14h (Pin Complex – FRONT) for N=4~7. Returns 00h for N>7. |
| 15:8 | Connection List Entry (N+1). Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7. Returns 17h (Pin Complex – SIDESURR) for N=8~11. Returns 00h for N>11. |
| 7:0 | Connection List Entry (N). Returns 18h (Pin Complex – MIC1) for N=0~3. Returns 1Ch (Pin Complex – CD) for N=4~7. Returns 16h (Pin Complex – CEN/LFE) for N=8~11. Returns 00h for N>11. |

Codec Response for NID=0Ch (Front Sum)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 02h (Front DAC) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=0Dh (Surround Sum)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 03h (Surround DAC) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=0Eh (Cen/LFE Sum)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 04h (Cen/LFE DAC) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=0Fh (Side-Surr Sum)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 05h (Front DAC) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=26h (Fout Sum)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 25h (Fout1 DAC) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=14h (Port-D)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 0Ch (Sum Widget NID=0Ch) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=15h (Port-A)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 0Dh (Sum Widget NID=0Dh) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=16h (Port-G)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 0Eh (Sum Widget NID=0Eh) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=17h (Port-H)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 00h. |
| 23:16 | Connection List Entry (N+2). Returns 00h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 0Fh (Sum Widget NID=0Fh) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=18h~1Bh (Port-B/C/E/F)

| Bit | Description |
|------------|--|
| 31:24 | Connection List Entry (N+3). Returns 0Fh (Sum Widget NID=0Fh) for N=0~3. Returns 00h for n>3. |
| 23:16 | Connection List Entry (N+2). Returns 0Eh (Sum Widget NID=0Eh) for N=0~3. Returns 00h for N>3. |
| 15:8 | Connection List Entry (N+1). Returns 0Dh (Sum Widget NID=0Dh) for N=0~3. Returns 00h for N>3. |
| 7:0 | Connection List Entry (N). Returns 0Ch (Sum Widget NID=0Ch) for N=0~3. Returns 26h (Sum Widget NID=26h) for N=4~7. Returns 00h for N>7. |

Codec Response for NID=1Eh (Pin Widget: SPDIF-OUT)

| Bit | Description |
|------------|--|
| 31:16 | Connection List Entry (N+3) and (N+2). Returns 0000h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 06h (SPDIF-OUT converter) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=11h (Pin Widget: SPDIF-OUT2)

| Bit | Description |
|------------|---|
| 31:16 | Connection List Entry (N+3) and (N+2). Returns 0000h. |
| 15:8 | Connection List Entry (N+1). Returns 00h. |
| 7:0 | Connection List Entry (N). Returns 10h (SPDIF-OUT2 converter) for N=0~3. Returns 00h for N>3. |

Codec Response for NID=22h (Sum Widget before ADC 09h)

| Bit | Description |
|------------|---|
| 31:24 | Connection List Entry (N+3). Returns 1Bh (Pin Complex – LINE2) for N=0~3. Returns 15h (Pin Complex-SURR) for N=4~7. Returns 12h for N=8~11. Returns 00h for N>11. |
| 23:16 | Connection List Entry (N+2). Returns 1Ah (Pin Complex – LINE1) for N=0~3. Returns 14h (Pin Complex – FRONT) for N=4~7. Returns 0Bh (Sum Widget) for N=8~11. Returns 00h for N>11. |
| 15:8 | Connection List Entry (N+1). Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7. Returns 17h (Pin Complex – SIDESURR) for N=8~11. Returns 00h for N>11. |
| 7:0 | Connection List Entry (N). Returns 18h (Pin Complex – MIC1) for N=0~3. Returns 1Ch (Pin Complex – CD) for N=4~7. Returns 16h (Pin Complex – CEN/LFE) for N=8~11. Returns 00h for N>11. |

Codec Response for NID=23h (Sum Widget before ADC 08h)

| Bit | Description |
|-------|---|
| 31:24 | Connection List Entry (N+3). Returns 1Bh (Pin Complex – LINE2) for N=0~3. Returns 15h (Pin Complex-SURR) for N=4~7. Returns 00h for N>7. |
| 23:16 | Connection List Entry (N+2). Returns 1Ah (Pin Complex – LINE1) for N=0~3. Returns 14h (Pin Complex – FRONT) for N=4~7. Returns 0Bh (Sum Widget) for N=8~11. Returns 00h for N>11. |
| 15:8 | Connection List Entry (N+1). Returns 19h (Pin Complex – MIC2) for N=0~3. Returns 1Dh (Pin Complex – PCBEEP) for N=4~7. Returns 17h (Pin Complex – SIDESURR) for N=8~11. Returns 00h for N>11. |
| 7:0 | Connection List Entry (N). Returns 18h (Pin Complex – MIC1) for N=0~3. Returns 1Ch (Pin Complex – CD) for N=4~7. Returns 16h (Pin Complex – CEN/LFE) for N=8~11. Returns 00h for N>11. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 37. Verb – Get Processing State (Verb ID=F03h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=F03h | 0's |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for All NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.6. Verb – Set Processing State (Verb ID=703h)

Table 38. Verb – Set Processing State (Verb ID=703h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|------------------------|
| CAd=X | Node ID=Xh | Verb ID=703h | Processing State [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 39. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=20h | Verb ID=Dh | 0's |

Codec Response Format

| Response [31:0] |
|----------------------------------|
| Bit [15:0] are Coefficient Index |

Codec Response for NID=20h (Realtek Defined Registers)

| Bit | Description |
|-------|------------------------|
| 31:16 | Reserved. Read as 0's. |
| 15:0 | Coefficient Index. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 40. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------------|
| CAd=X | Node ID=Xh | Verb ID=5h | Coefficient Index [15:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 41. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=20h | Verb ID=Ch | 0's |

Codec Response Format

| Response [31:0] |
|-------------------------------|
| Processing Coefficient [15:0] |

Codec Response for NID=20h (Realtek Defined Registers)

| Bit | Description |
|-------|-------------------------|
| 31:16 | Reserved. Read as 0's. |
| 15:0 | Processing Coefficient. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 42. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=Xh | Verb ID=4h | Coefficient [15:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 43. Verb – Get Amplifier Gain (Verb ID=Bh)

| Get Command Format | | | | Codec Response Format | |
|--------------------|--------------------|--------------------|---------------------------|------------------------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] | Response [31:0] | |
| CAd=X | Node ID=Xh | Verb ID=Bh | ‘Get’ Payload [15:0] | Bit[7:0] are Responsible for ‘Get’ | |

‘Get’ Payload in Command Bit[15:0]

| Bit | Description |
|------|--|
| 15 | Get Input/Output. 0: Input amplifier gain is requested 1: Output amplifier gain is requested |
| 14 | Reserved. Read as 0. |
| 13 | Get Left/Right. 0: Right amplifier gain is requested 1: Left amplifier gain is requested |
| 12:4 | Reserved. Read as 0’s. |
| 3:0 | Index[3:0] for Input Source. Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored. |

Codec Response for 08h (LINE ADC) and 09h (MIX ADC)

| Bit | Description |
|------|--|
| 31:8 | 0’s. |
| 7 | Bit 15 is 0 in ‘Get Amplifier Gain’. Input Amplifier Mute. 0: Unmute 1: Mute Bit 15 is 1 in ‘Get Amplifier Gain’. Read as 0 (No Output Amplifier Mute). |
| 6:0 | Bit 15 is 0 in ‘Get Amplifier Gain’. Input Amplifier Gain [6:0]. 7-bit step value (0~46) specifying the volume from –16dB~+30dB in 1.0dB steps. Bit 15 is 1 in ‘Get Amplifier Gain’. Read as 0’s (No Output Amplifier Mute). |

Codec Response for NID=0Bh (MIXER Sum Widget)

| Bit | Description |
|------|--|
| 31:8 | 0’s. |
| 7 | Bit 15 is 0 in ‘Get Amplifier Gain’. Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index) Bit 15 is 1 in ‘Get Amplifier Gain’. Read as 0 (No Output Amplifier Mute). |
| 6:0 | Bit 15 is 0 in ‘Get Amplifier Gain’. Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –34.5dB~+12dB in 1.5dB steps. Bit 15 is 1 in ‘Get Amplifier Gain’. Read as 0’s (No Output Amplifier Mute). |

Codec Response for NID=0Ch~0Fh and 26h (Sum Widget: Front, Surr, Cen/LFE, SIDESURR Sum, Fout)

| Bit | Description |
|------|--|
| 31:8 | 0's. |
| 7 | Bit 15 is 0 in 'Get Amplifier Gain'. Input Amplifier Mute. 0: Unmute 1: Mute Bit 15 is 1 in 'Get Amplifier Gain'. Read as 0 (No Output Amplifier Mute). |
| 6:0 | Bit 15 is 0 in 'Get Amplifier Gain'. Read as 0 (No Input Amplifier Gain). Bit 15 is 1 in 'Get Amplifier Gain'. Output Amplifier Gain [6:0]. 7-bit step value (0~64) specifying the volume from -64dB~0dB in 1.0dB steps. |

Codec Response for NID=02h ~ 05h and 25h (DAC Widget: Front, Surr, Cen/LFE, SIDESURR, Fout DAC)

| Bit | Description |
|------|--|
| 31:8 | 0's. |
| 7 | Bit 15 is 0 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Mute). Bit 15 is 1 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Mute). |
| 6:0 | Bit 15 is 0 in 'Get Amplifier Gain. Read as 0's (No Output Amplifier Mute). Bit 15 is 1 in 'Get Amplifier Gain. Output Amplifier Gain [6:0]. 7-bit step value (0~64) specifying the volume from -64dB~0dB in 1dB steps. |

Codec Response for NID=14h~17h (Pin Complex: Front/Surr/CenLFE/SIDESURR)

| Bit | Description |
|------|---|
| 31:8 | 0's. |
| 7 | Bit 15 is 0 in 'Get Amplifier Gain'. Read as 0. Bit 15 is 1 in 'Get Amplifier Gain'. Output Amplifier Mute. 0: Unmute 1: Mute (NID=14h~17h, Default=1) |
| 6:0 | Bit 15 is 0 in 'Get Amplifier Gain'. Read as 0's. Bit 15 is 1 in 'Get Amplifier Gain'. Read as 0 (No Output Amplifier Gain). |

Codec Response for NID=18h~1Bh (Pin Complex: MIC1/MIC2/LINE1/LINE2)

| Bit | Description |
|------|--|
| 31:8 | 0's. |
| 7 | Bit 15 is 0 in 'Get Amplifier Gain. Read as 0. Bit 15 is 1 in 'Get Amplifier Gain. Output Amplifier Mute: 0: Unmute 1: Mute (NID=18h~1Bh, Default=1) |
| 6:0 | Bit 15 is 0 in 'Get Amplifier Gain. Input Amplifier Gain [6:0]. 7-bit step value (0~3) specifying the volume from 0dB~30dB in 10dB steps. Bit 15 is 1 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Gain). |

Codec Response for NID=22h and 23h (Sum Widget)

| Bit | Description |
|------|---|
| 31:8 | 0's. |
| 7 | Bit 15 is 0 in 'Get Amplifier Gain. Input Amplifier Mute: 0: Unmute; 1: Mute Bit 15 is 1 in 'Get Amplifier Gain. Read as 0 (No Output Amplifier Mute). |
| 6:0 | Bit 15 is 0 in 'Get Amplifier Gain. Read as 0 (No Input Amplifier Gain). Bit 15 is 1 in 'Get Amplifier Gain. Read as 0 (No Input Amplifier Gain). |

Codec Response to Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 44. Verb – Set Amplifier Gain (Verb ID=3h)
Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|------------|---------------------|
| CAd=X | Node ID=Xh | Verb ID=3h | 'Set' Payload [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

'Set' Payload in Command Bit[15:0]

| Bit | Description |
|------|---|
| 15 | Set Output Amp. '1' indicates output amplifier gain will be set. |
| 14 | Set Input Amp. '1' indicates input amplifier gain will be set. |
| 13 | Set Left Amp. '1' indicates left amplifier gain will be set. |
| 12 | Set Right Amp. '1' indicates right amplifier gain will be set. |
| 11:8 | Index Offset (for Input Amplifiers on Sum Widgets and Selector Widgets). 5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the 'Set Input Amp' bit is not set. |
| 7 | Mute. 0: Unmute 1: Mute ($-\infty$ gain) |
| 6:0 | Gain[6:0]. A 7-bit step value specifying the amplifier gain. |

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 45. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=Xh | Verb ID=Ah | 0's |

Codec Response Format

| Response [31:0] |
|--------------------------------|
| Bit[15:0] are Converter Format |

Codec Response for NID=02h~06h, 10h, 25h (Output Converters: Front, Surr, Cen/LFE, Side-Surr, Fout DAC, SPDIF-OUT, SPDIF-OUT2).

Codec Response for NID=08h~0Ah (Input Converters: LINE, MIX DAC, and SPDIF-IN)

| Bit | Description |
|-------|---|
| 31:16 | Reserved. Read as 0. |
| 15 | Stream Type (TYPE). 0: PCM 1: Non-PCM |
| 14 | Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz |
| 13:11 | Sample Base Rate Multiple (MULT). 000b: ×1 001b: ×2 010b: ×3 011b: ×4 100b~111b: Reserved |
| 10:8 | Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 |
| 7 | Reserved. Read as 0. |
| 6:4 | Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved |
| 3:0 | Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels |

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 46. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X | Node ID=Xh | Verb ID=2h | Set Format [15:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

'Set' Payload in Command Bit[15:0]

| Bit | Description |
|-------|---|
| 31:16 | Reserved. Read as 0. |
| 15 | Stream Type (TYPE). 0: PCM 1: Non-PCM |
| 14 | Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz |
| 13:11 | Sample Base Rate Multiple (MULT). 000b: ×1 001b: ×2 010b: ×3 011b: ×4 100b~111b: Reserved |
| 10:8 | Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 |
| 7 | Reserved. Read as 0. |
| 6:4 | Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved |
| 3:0 | Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels 15: 16 channels |

8.15. Verb – Get Power State (Verb ID=F05h)

Table 47. Verb – Get Power State (Verb ID=F05h)

| Get Command Format | | | | Codec Response Format | |
|--------------------|--------------------|-------------------|--------------------------|------------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAd=X | Node ID=01h | Verb ID=Ah | 0's | Power State [7:0] | |

Codec Response for NID=01h (Audio Function Group)

Codec Response for NID=02h~05h, 25h, 08h, 09h (Audio Input/Output Converter)

Codec Response for NID=11h, 12h, 14h~1Fh (Pin Widget)

Codec Response for NID=06h, 10h, 0Ah (Audio Input/Output Converter)

| Bit | Description |
|------|--|
| 31:6 | Reserved. Read as 0's. |
| 5:4 | PS-Act. Actual Power State [1:0]. 00: Power state is D0 10: Power state is D2 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set. |
| 3:2 | Reserved. Read as 0's. |
| 1:0 | PS-Set. Set Power State [1:0]. 00: Power state is D0 10: Power state is D2 PS-Set controls the current power setting of the referenced node. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.16. Verb – Set Power State (Verb ID=705h)

Table 48. Verb – Set Power State (Verb ID=705h)

| Set Command Format | | | | Codec Response Format | |
|--------------------|--------------------|-------------------|--------------------------|------------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAd=X | Node ID=01h | Verb ID=705h | Power State [7:0] | 0's for All Nodes | |

'Power State' in Command Bit[7:0]

| Bit | Description |
|-----|--|
| 7:6 | Reserved. Read as 0's. |
| 5:4 | PS-Act. Actual Power State [1:0]. 00: Power state is D0 10: Power state is D2 PS-Act indicates the actual power state of the referenced node. |
| 3:2 | Reserved. Read as 0's. |
| 1:0 | PS-Set. Set Power State [1:0]. 00: Power state is D0 10: Power state is D2 |

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F06h | 0's | Stream & Channel [7:0] |

Codec Response for NID=02h~05h,25h, 06h, 10h (Output Converters: Front, Surr, Cen/LFE, Side-Surr, Fout DAC, SPDIF-OUT, SPDIF-OUT2)

Codec Response for NID=08h~0Ah (Input Converters: LINE ADC, MIX DAC, and SPDIF-IN)

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's. |
| 7:4 | Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc. |
| 3:0 | Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 50. Verb – Set Converter Stream, Channel (Verb ID=706h)

| Set Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=706h | Stream & Channel [7:0] | 0's for All Nodes |

'Stream and Channel' in Command Bit[7:0]

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's. |
| 7:4 | Set Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc. |
| 1:0 | Set Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel. |

Note: This verb assigns stream and channel for output converters (NID=02h~06h, 25h, 10h) and input converters (NID=08h~0Ah). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 51. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=F07h | 0's |

Codec Response Format

| Response [31:0] |
|-------------------|
| Pin Control [7:0] |

Codec Response for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 11h, 1Fh, (Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, SPDIF-OUT, SPDIF-OUT2, and SPDIF-IN)

| Bit | Description |
|------|---|
| 31:1 | Reserved. Read as 0's. |
| 7 | H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O Unit). 0: Disabled 1: Enabled |
| 6 | Out Enable (Output Buffet Enable, EN_OBUF for an I/O Unit). 0: Disabled 1: Enabled |
| 5 | In Enable (Input Buffer Enable, EN_IBUF for an I/O Unit). 0: Disabled 1: Enabled |
| 4:3 | Reserved. |
| 2:0 | VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of LDO-OUT1 010b: Ground 0V 011b: Reserved 100b: 80% of LDO-OUT1 101b: 100% of LDO-OUT1 110b~111b: Reserved |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 52. Verb – Set Pin Widget Control (Verb ID=707h)

| Set Command Format | | | | Codec Response Format | |
|--------------------|-------------|--------------|-------------------|-----------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAAd=X | Node ID=Xh | Verb ID=707h | Pin Control [7:0] | 0's for All Nodes | |

'Pin Control' in command [7:0] for NID=14h~1Bh, 1Ch, 1Dh, 1Eh, 11h, 1Fh (Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, LINE2, CD-IN, PCBEEP, SPDIF-OUT, SPDIF-OUT2, and SPDIF-IN)

| Bit | Description | | | |
|------|--|--|--|--|
| 31:1 | Reserved. Read as 0's. | | | |
| 7 | H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O Unit). 0: Disabled 1: Enabled | | | |
| 6 | Out Enable (Output Buffet Enable, EN_OBUF for an I/O Unit). 0: Disabled 1: Enabled | | | |
| 5 | In Enable (Input Buffer Enable, EN_IBUF for an I/O Unit). 0: Disabled 1: Enabled | | | |
| 4:3 | Reserved. | | | |
| 2:0 | VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of LDO-OUT1 010b: Ground 0V 011b: Reserved 100b: 80% of LDO-OUT1 101b: 100% of LDO-OUT1 110b~111b: Reserved | | | |

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

Table 53. Verb – Get Unsolicited Response Control (Verb ID=F08h)

| Get Command Format | | | | Codec Response Format | |
|--------------------|-------------|---------------|-------------------|-----------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] | |
| CAAd=X | Node ID=Xh | Verb ID= F08h | 0's | 32-bit Response | |

Codec Response for NID=01h (GPIO in Audio Function Group), 14h~1Ch, 1Eh, 11h, 1Fh (Port A to H, CD-IN, SPDIF-OUT, SPDIF-OUT2 and SPDIF-IN)

| Bit | Description |
|------|---|
| 31:8 | Reserved. Read as 0's. |
| 7 | Unsolicited Response is Enabled. 0: Disabled 1: Enabled |
| 6:4 | Reserved. Read as 0's. |
| 3:0 | Assigned Tag for Unsolicited Response. The tag[3:0] is assigned by software to determine which widget generates unsolicited responses. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enables a widget to generate an unsolicited response.

Table 54. Verb – Set Unsolicited Response Control (Verb ID=708h)

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=708h | EnableUnsol [7:0] | 0's for All Nodes |

'EnableUnsol' in Command Bit[7:0] for NID=01h (GPIO in Audio Function Group), 14h~1Ch, 1Eh, 11h, 1Fh (Port A to H, CD-IN, SPDIF-OUT, SPDIF-OUT2 and SPDIF-IN)

| Bit | Description |
|------|--|
| 31:8 | Reserved. Read as 0's. |
| 7 | Enable Unsolicited Response. 0: Disable 1: Enable |
| 6:4 | Reserved. Read as 0's. |
| 3:0 | Tag for Unsolicited Response. Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses. |

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 55. Verb – Get Pin Sense (Verb ID=F09h)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|---------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= F09h | 0's | 32-bit Response |

Codec Response for NID = 14h~1Bh, 11h, 1Eh, 1Fh

| Bit | Description |
|------|--|
| 31 | Presence Detect Status. 0: No device is attached to the pin 1: Device is attached to the pin |
| 30:0 | Measured Impedance. The ALC888S-VD does not support hardware impedance detection. This field is read as 0s. |

Codec Response for Other NID

| Bit | Description |
|------|------------------------------------|
| 31:0 | Not Supported (Returns 00000000h). |

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 56. Verb – Execute Pin Sense (Verb ID=709h)

Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID= 709h | Right Channel[0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

'Payload' in Command Bit[7:0]

| Bit | Description |
|-----|--|
| 7:1 | Reserved. Read as 0's. |
| 0 | Right (Ring) Channel Select. 0: Sense Left channel (Tip) 1: Sense Right channel (Ring) The ALC888S-VD does not support hardware impedance sensing and will ignore this control. |

8.25. Verb – Get Volume Knob Widget (Verb ID=F0Fh)

Table 57. Verb – Get Volume Knob (Verb ID=F0Fh)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X | Node ID=21h | Verb ID= F0Fh | 0's |

Codec Response Format

| Response [31:0] |
|----------------------------------|
| Bit[31:8]=0s, Bit[7:0] is Volume |

Codec Response for NID = 21h (Volume Knob Widget)

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7 | Direct. 0: The volume generated by external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by external HW volume control will directly affect the volume of the amplifier. |
| 6:0 | Volume in Steps. |

Note: The ALC888S-VD does not support Volume Knob Widget and will ignore this verb and respond with 0's.

8.26. Verb – Set Volume Knob Widget (Verb ID=70Fh)

Table 58. Verb – Set Volume Knob (Verb ID=70Fh)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|---------------|----------------------------|
| CAd=X | Node ID=21h | Verb ID= 70Fh | Bit[7] is 'Direct' Control |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's |

'Payload' in Command Bit[7:0]

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7 | Direct. 0: The volume generated by external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by external HW volume control will directly affect the volume of the amplifier. |
| 6:0 | Reserved. |

Note: The ALC888S-VD does not support Volume Knob Widget and will ignore this verb and respond with 0's.

8.27. Verb – Get Configuration Default (Verb ID=F1Ch)

Reads the 32-bit sticky register for each Pin Widget configured by software.

Table 59. Verb – Get Configuration Default (Verb ID=F1Ch)

| Get Command Format | | | | Codec Response Format |
|--------------------|--------------------|-------------------|--------------------------|------------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= F1Ch | 0's | 32-bit Response |

Codec Response for NID=14h~1Bh (Port-A~Port-H), 1Ch (CD-IN), 1Dh (BEEP-IN), 1Eh (SPDIF-OUT), 1Fh (SPDIF-IN), 11h (SPDIF-OUT2), and 12h (Digital MIC)

| Bit | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|--|-----------|-----------|-----------|-----------|---------|---------|-----------|-----------|-----------|-----------|-----------|-----------|---------|---------|---------|---------|---------|---------|-----------|-----------|-----------|-----------|-----------|-----------|---------|---------|-----------|-----------|
| 31:0 | <p>32-Bit Configuration Information for Each Pin Widget. Default value for each pin widget. [31:30]: Port Connectivity (0h: Port; 2h: Header; 1h: Not Connected) [29:24]: Location [23:20]: Default Device [19:16]: Connection Type [15:12]: Color [11:08]: Misc [07:04]: Default Association [03:00]: Sequence</p> <table border="1" data-bbox="320 1070 1337 1144"> <thead> <tr> <th>NID 14h</th> <th>NID 15h</th> <th>NID 16h</th> <th>NID 17h</th> <th>NID 18h</th> <th>NID 19h</th> </tr> </thead> <tbody> <tr> <td>01014030h</td> <td>01011031h</td> <td>01016032h</td> <td>01012033h</td> <td>01A19850h</td> <td>02A19C80h</td> </tr> </tbody> </table> <table border="1" data-bbox="320 1182 1337 1256"> <thead> <tr> <th>NID 1Ah</th> <th>NID 1Bh</th> <th>NID 1Ch</th> <th>NID 1Dh</th> <th>NID 1Eh</th> <th>NID 1Fh</th> </tr> </thead> <tbody> <tr> <td>01813051h</td> <td>02214C40h</td> <td>9993105Fh</td> <td>00000100h</td> <td>01441070h</td> <td>41C46060h</td> </tr> </tbody> </table> <table border="1" data-bbox="320 1294 660 1368"> <thead> <tr> <th>NID 11h</th> <th>NID 12h</th> </tr> </thead> <tbody> <tr> <td>411110F0h</td> <td>411111F0h</td> </tr> </tbody> </table> | NID 14h | NID 15h | NID 16h | NID 17h | NID 18h | NID 19h | 01014030h | 01011031h | 01016032h | 01012033h | 01A19850h | 02A19C80h | NID 1Ah | NID 1Bh | NID 1Ch | NID 1Dh | NID 1Eh | NID 1Fh | 01813051h | 02214C40h | 9993105Fh | 00000100h | 01441070h | 41C46060h | NID 11h | NID 12h | 411110F0h | 411111F0h |
| NID 14h | NID 15h | NID 16h | NID 17h | NID 18h | NID 19h | | | | | | | | | | | | | | | | | | | | | | | | |
| 01014030h | 01011031h | 01016032h | 01012033h | 01A19850h | 02A19C80h | | | | | | | | | | | | | | | | | | | | | | | | |
| NID 1Ah | NID 1Bh | NID 1Ch | NID 1Dh | NID 1Eh | NID 1Fh | | | | | | | | | | | | | | | | | | | | | | | | |
| 01813051h | 02214C40h | 9993105Fh | 00000100h | 01441070h | 41C46060h | | | | | | | | | | | | | | | | | | | | | | | | |
| NID 11h | NID 12h | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 411110F0h | 411111F0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

Table 60. Default Configuration in Chip (14h~1Ch)

| NID= | 14h | 15h | 16h | 17h | 18h | 19h | 1Ah | 1Bh | 1Ch |
|-------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| Name | FRONT | SURR | CEN/LFE | SIDE | MIC1 | MIC2 | LINE1 | LINE2 | CD-IN |
| Port | Jack | Jack | Jack | Jack | Jack | Jack | Jack | Jack | Header |
| Location | Rear | Rear | Rear | Rear | Rear | Front | Rear | Front | Inside |
| Device | Line Out | Line Out | Line Out | Line Out | Mic In | Mic In | Line In | HP Out | AUX |
| Con Type | 1/8" Jack | 1/8" Jack | 1/8" Jack | 1/8" Jack | 1/8" Jack | 1/8" Jack | 1/8" Jack | 1/8" Jack | ATAPI |
| Color | Green | Black | Orange | Grey | Pink | Pink | Blue | Green | Black |
| Misc | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | ✓Vrefo *Retask *Sensing ✓JD | ✓Vrefo ✓Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | ✓Vrefo ✓Retask *Sensing ✓JD | *Vrefo *Retask *Sensing *JD |
| Association | 3h | 3h | 3h | 3h | 5h | 8h | 5h | 4h | 5h |
| Sequence | 0h | 1h | 2h | 3h | 0h | 0h | 1h | 0h | Fh |

Table 61. Default Configuration in Chip (1Dh~12h)

| NID= | 1Dh | 1Eh | 1Fh | 11h | 12h |
|-------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| Name | BEEP-IN | SPDIF-OUT | SPDIF-IN | SPDIF-OUT2 | Digital MIC |
| Port | Internal | Jack | NC | NC | NC |
| Location | Unknown | Rear | Rear | Rear | Rear |
| Device | Other | SPDIF Out | SPDIF-In | Speaker | Speaker |
| Con Type | Other | RCA | RCA | 1/8" Jack | 1/8" Jack |
| Color | Other | Black | Orange | Black | Black |
| Misc | *Vrefo *Retask *Sensing *JD | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing ✓JD | *Vrefo *Retask *Sensing *JD |
| Association | 0h | 7h | 6h | Fh | Fh |
| Sequence | 0h | 0h | 0h | 0h | 0h |

8.28. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh, 11h, 12h, 1Eh, and 1Fh, e.g., placement and expected default device.

Table 62. Verb – Set Configuration Default Bytes 0, 1, 2, 3

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|-----------------------------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=71Ch, 71Dh, 71Eh, 71Fh | Label [7:0] | 0's for All Nodes |

Note: Supported by Pin Widget NID=14h~1Bh (Port-A~Port-H), 1Ch (CD-IN), 1Dh (BEEP-IN), 1Eh (SPDIF-OUT), 1Fh (SPDIF-IN), 11h (SPDIF-OUT2), and 12h (Digital MIC). Other widgets will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.29. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 63. Verb – Get BEEP Generator (Verb ID= F0Ah)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|---------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID= F0Ah | 0's | Divider [7:0] |

'Response' for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7:0 | Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255×4)=47Hz. The highest tone is 48kHz/(1×4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input. |

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.30. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 64. Verb – Set BEEP Generator (Verb ID= 70Ah)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=70Ah | Divider [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

'Divider' in Set Command

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7:0 | Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is $48\text{kHz}/(255 \times 4) = 47\text{Hz}$. The highest tone is $48\text{kHz}/(1 \times 4) = 12\text{kHz}$. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input. |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.31. Verb – Get GPIO Data (Verb ID=F15h)

Table 65. Verb – Get GPIO Data (Verb ID= F15h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=F15h | 0's |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Data. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Data. The value written (output) or sensed (input) on the corresponding pin if it is enabled. |

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.32. Verb – Set GPIO Data (Verb ID=715h)

Table 66. Verb – Set GPIO Data (Verb ID= 715h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=715h | Data [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

'Data' in Set command for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Output Data. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Output Data. The value written determines the value driven on a pin that is configured as an output pin. |

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.33. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 67. Verb – Get GPIO Enable Mask (Verb ID= F16h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=F16h | 0's |

Codec Response Format

| Response [31:0] |
|------------------|
| EnableMask [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:3 | Reserved. |
| 2:0 | GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.34. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 68. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=716h | Enable Mask [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Enable Mask. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.35. Verb – Get GPIO Direction (Verb ID=F17h)

Table 69. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=F17h | 0's |

Codec Response Format

| Response [31:0] |
|-----------------|
| Direction [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Direction Control. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.36. Verb – Set GPIO Direction (Verb ID=717h)

Table 70. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=717h | Direction [7:0] |

Codec Response Format

| Response [31:0] |
|-------------------|
| 0's for All Nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|---|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Direction Control. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.37. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 71. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=01h | Verb ID=F19h | 0's |

Codec Response Format

| Response [31:0] |
|-------------------|
| UnsolEnable [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.38. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 72. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=01h | Verb ID=719h | UnsolEnable [7:0] | 0's for All Nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit | Description |
|------|--|
| 31:8 | Reserved. |
| 7:3 | GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC888S-VD. |
| 2:0 | GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.39. Verb – Function Reset (Verb ID=7FFh)

Table 73. Verb – Function Reset (Verb ID=7FFh)

| Command Format (NID=01h) | | | | Codec Response Format |
|--------------------------|-------------|--------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=01h | Verb ID=7FFh | 0's | 0's |

Codec Response

| Bit | Description |
|------|------------------------|
| 31:0 | Reserved. Read as 0's. |

Note: The Function Reset command causes all widgets in the ALC888S-VD to return to their power on default state.

8.40. Verb – Get Digital Converter Control 1, 2, 3, 4 (Verb ID=F0Dh, F0Eh, F3Eh, F3Fh)

Table 74. Verb – Get Digital Converter Control 1, 2, 3, 4 (Verb ID=F0Dh, F0Eh, F3Eh, F3Fh)

| Get Command Format | | | | Codec Response Format |
|--------------------|-------------|---------------------------------|-------------------|--|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd=X | Node ID=Xh | Verb ID=F0Dh/F0Eh/ F3Eh/F3Fh | 0's | Bit[31:16]=0's, Bit[15:0] are SIC Bit |

NID=06h (SPDIF-OUT) Response to 'Get verb' – F0Dh/F0Eh/F3Eh/F3Fh
 NID=10h (SPDIF-OUT2) Response to 'Get verb' – F0Dh/F0Eh/F3Eh/F3Fh

| Bit | Description – SIC (SPDIF IEC Control) Bit[15:0] |
|-------|--|
| 31:24 | Read as 0's. |
| 23 | Keep Alive Enable. 0: Disable (SPDIF output is disabled in D2/D3 mode) 1: Enable (SPDIF output is enabled in D2/D3 mode) |
| 22:20 | Reserved. Read as 0's. |
| 19:16 | IEC Coding Type. Not supported in ALC888S-VD, read as 0's. |
| 15 | Reserved. Read as 0's. |
| 14:8 | CC[6:0] (Category Code). |
| 7 | LEVEL (Generation Level). |
| 6 | PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format |
| 5 | /AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright). 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | VCFG for Validity Control (Control V Bit and Data in Sub-Frame). |
| 1 | V for Validity Control (Control V Bit and Data in Sub-Frame). |
| 0 | Digital Enable (DigEn). 0: OFF 1: ON |

NID=0Ah (SPDIF-IN) Response to 'Get verb' - F0Dh/F0Eh

| Bit | Description (part of SPDIF-IN Channel Status) |
|-------|---|
| 31:15 | Reserved. Read as 0's. |
| 14:8 | CC[6:0] (Category Code). |

NID=0Ah (SPDIF-IN) Response to 'Get verb' - F0Dh/F0Eh

| Bit | Description (part of SPDIF-IN Channel Status) |
|------------|--|
| 7 | LEVEL (Generation Level). |
| 6 | PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format |
| 5 | /AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright). 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | Reserved. |
| 1 | Invalid. V Bit in Sub-Frame of SPDIF-IN. 0: Data X and Y are valid, or SPDIF-IN is not locked 1: At least one of data X and Y is invalid |
| 0 | Digital Enable (DigEn). 0: OFF 1: ON |

Codec Response for Other NID

| Bit | Description |
|------------|--------------------|
| 31:0 | 0's. |

8.41. Verb – Set Digital Converter Control 1, 2, 3, 4 (Verb ID=70Dh, 70Eh, 73Eh, 73Fh)

Table 75. Verb – Set Digital Converter Control 1, 2, 3, 4 (Verb ID=70Dh, 70Eh, 73Eh, 73Fh)

Set Command Format (Verb ID=70Dh, Set Control 1)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=70Dh | SIC [7:0] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's |

Set Command Format (Verb ID=70Eh, Set Control 2)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=70Eh | SIC [15:8] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's |

Set Command Format (Verb ID=73Eh, Set Control 3)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=73Eh | SIC [23:16] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's |

Set Command Format (Verb ID=73Fh, Set Control 4)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X | Node ID=Xh | Verb ID=73Fh | SIC [31:24] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's |

'Payload' in Set Control 1 for NID=06h and 10h (SPDIF-OUT and SPDIF-OUT2)

| Bit | Description – SIC (SPDIF IEC Control) Bit[7:0] |
|-----|--|
| 7 | LEVEL (Generation Level). |
| 6 | PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format |
| 5 | /AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data |
| 4 | COPY (Copyright). 0: Asserted 1: Not asserted |
| 3 | PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds |
| 2 | VCFG for Validity Control (Control V Bit and Data in Sub-Frame). |
| 1 | V for Validity Control (Control V Bit and Data in Sub-Frame). |
| 0 | Digital Enable (DigEn). 0: OFF 1: ON |

'Payload' in Set Control 2 for NID=06h and 10h (SPDIF-OUT and SPDIF-OUT2)

| Bit | Description – SIC (SPDIF IEC Control) Bit[7:0] |
|-----|--|
| 7 | Reserved. Read as 0's. |
| 6:0 | CC[6:0] (Category Code). |

'Payload' in Set Control 3 for NID=06h and 10h (SPDIF-OUT and SPDIF-OUT2)

| Bit | Description – SIC (SPDIF IEC Control) Bit[23:16] |
|-----|--|
| 7 | Keep Alive Enable. 0: Disable (SPDIF output would be disabled in D2/D3 mode) 1: Enable (SPDIF output would be enabled in D2/D3 mode) |
| 6:0 | Reserved. |

'Payload' in Set Control 4 for NID=06h and 10h (SPDIF-OUT and SPDIF-OUT2)

| Bit | Description – SIC (SPDIF IEC Control) Bit[31:24] |
|-----|--|
| 7:0 | Reserved. |

'Payload' in Set Control 1 for NID=0Ah (SPDIF-IN)

| Bit | Description – SIC (SPDIF IEC Control) Bit[7:0] |
|-----|--|
| 7:1 | Reserved. |
| 0 | Digital Enable (DigEn). 0: OFF 1: ON |

'Payload' in Set Control 2 for NID=0Ah (SPDIF-IN)

| Bit | Description – SIC (SPDIF IEC Control) Bit[7:0] |
|-----|--|
| 7:0 | Reserved. Read as 0's. |

Note: Other widgets will ignore this verb.

8.42. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

32-bit Read/Write register for Audio Function Group (NID=01h)

Table 76. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd = X | Node ID=01h | Verb ID=F20h | 0s |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=01h

| Bit | Description |
|-------|-------------------------------------|
| 31:16 | Subsystem ID[23:8] (Default=10ECh). |
| 15:8 | Subsystem ID[7:0] (Default=08h). |
| 7:0 | Assembly ID[7:0] (Default=88h). |

8.43. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Table 77. Verb – Set Subsystem ID [31:0]
(Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

| Set Command Format | | | | Codec Response Format |
|--------------------|-------------|-----------------------------------|-------------------|-----------------------|
| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
| CAd = X | Node ID=01h | Verb ID=723h, 722h, 721h, 720h | Label [7:0] | 0s for All Nodes |

Codec Response for all NID

| Bit | Description |
|------|-------------|
| 31:0 | 0s. |

8.44. Verb – Get EAPD Control (Verb ID=F0Ch for Get)

Table 78. Verb – Get EAPD Control (Verb ID=F0Ch)

Get Command Format (NID=14h and 15h)

Codec Response Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] | Response [31:0] |
|-------------|-----------------|--------------|-------------------|------------------------|
| CAd=X | Node ID=14h/1Bh | Verb ID=F0Ch | 0s | Bit[1] is EAPD Control |

Codec Response for NID=14h (FRONT, port-D) and 1Bh (LINE2, port-E)

| Bit | Description |
|------|--|
| 31:3 | Reserved. |
| 2 | L-R Swap. The ALC888S-VD does not support swapping left and right channels. Read as 0. |
| 1 | EAPD Value. 0: EAPD pin state is low 1: EAPD pin state is high |
| 0 | Bridge Tied Load (BTL) Enable. The ALC888S-VD does not support BTL output. Read as 0. |

Codec Response in for Other NID

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

8.45. Verb – Set EAPD Control (Verb ID=70Ch for Set)

Table 79. Verb – Set EAPD Control (Verb ID=70Ch for Set)

Set Command Format (NID=14h and 15h)

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-----------------|--------------|------------------------|
| CAd=X | Node ID=14h/1Bh | Verb ID=70Ch | Bit[1] is EAPD Control |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0s |

Payload in Set Command for NID=14h (FRONT, port-D) and 1Bh (LINE2, port-E)

| Bit | Description |
|-----|--|
| 7:3 | Reserved. Written Data is Ignored. |
| 2 | L-R Swap. The ALC888S-VD does not support swapping left and right channels, written data is ignored. |
| 1 | EAPD Value. 0: EAPD pin state is low 1: EAPD pin state is high |
| 0 | Bridge Tied Load (BTL) Enable. The ALC888S-VD does not support BTL output. Written data is ignored. |

Note: Pin 47 is shared by the EPAD and SPDIF-IN functions. Pin 47 will act as EAPD and reflect the set EAPD state in payload bit[1] when pin widget SPDIF-IN is not connected via the programming configuration register. Other widgets will ignore this verb

Codec Response

| Bit | Description |
|------|-------------|
| 31:0 | 0's. |

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 80. Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--------------------------------------|----------|---------|---------|---------|-------|
| Power Supply | | | | | |
| Digital Power for Core | DVDD | 3.0 | 3.3 | 3.6 | V |
| Digital Power for HDA Link | DVDD-IO* | 1.5 | 3.3 | 3.6 | V |
| Analog | LDO-IN** | 4.5 | 5.0 | 5.5 | V |
| | LDO-OUT1 | 4.05 | 4.5 | 4.95 | V |
| Ambient Operating Temperature | Ta | 0 | - | +70 | °C |
| Storage Temperature | Ts | - | - | +125 | °C |
| ESD (Electrostatic Discharge) | | | | | |
| Susceptibility Voltage | | | | | |
| All Pins | | 4000 | | | |

*: The digital link power DVDD-IO must be lower than the digital core power DVDD.

**.: The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Realtek technical support representatives for special testing support.

9.1.2. Threshold Voltage

DVDD-IO= 1.5V±5%/3.3V±5%, DVDD= 3.3V±5%, T_{ambient}=25°C, with 50pF external load.

Table 81. Threshold Voltage

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|-----------------|------------------|---------|------------------|-------|
| Input Voltage Range | V _{in} | -0.30 | - | DVDD+0.30 | V |
| Low Level Input Voltage (HDA link) | V _{IL} | - | - | 0.4×DVDD-IO | V |
| High Level Input Voltage (HDA link) | V _{IH} | 0.6×DVDD-IO | - | - | V |
| High Level Output Voltage (HDA link) | V _{OH} | 0.9×DVDD-IO | - | - | V |
| Low Level Output Voltage (HDA link) | V _{OL} | - | - | 0.1×DVDD-IO | V |
| Low Level Input Voltage (SPDIF-IN, GPIOs) | V _{IL} | - | - | 0.44×DVDD (1.45) | V |
| High Level Input Voltage (SPDIF-IN, GPIOs) | V _{IH} | 0.56×DVDD (1.85) | - | - | V |
| High Level Output Voltage (SPDIF-OUT, GPIOs) | V _{OH} | 0.9×DVDD | - | - | V |
| Low Level Output Voltage (SPDIF-OUT, GPIOs) | V _{OL} | - | - | 0.1×DVDD | V |
| Input Leakage Current | - | -10 | - | 10 | μA |
| Output Leakage Current (Hi-Z) | - | -10 | - | 10 | μA |
| Output Buffer Drive Current | - | - | 5 | - | mA |
| Internal Pull Up Resistance | - | - | 50k | - | Ω |

9.1.3. Digital Filter Characteristics

Table 82. Digital Filter Characteristics

| Filter | Description | Minimum | Typical | Maximum | Units |
|---------------------|--|----------|-----------|---------|-------|
| ADC Filter | Passband (Upper Band < -0.030dB) | - | 0.4350×Fs | - | KHz |
| | Passband (Upper Band < -1.0dB) | - | 0.4571×Fs | - | KHz |
| | Passband Ripple | - | - | ±0.030 | dB |
| | Stopband | 0.565×Fs | - | - | KHz |
| | Stopband Attenuation | 80 | - | - | dB |
| ADC Highpass Filter | Passband Frequency Response: -0.15dB (Fs=192000) | - | 20 | - | Hz |
| DAC Lowpass Filter | Passband Frequency Response: -0.03dB | - | 0.441×Fs | - | KHz |
| | Stopband | 0.559×Fs | - | 1.5×Fs | KHz |
| | Stopband Rejection | 90 | - | - | dB |
| | Passband Ripple | - | - | ±0.030 | dB |
| DAC Highpass Filter | Passband Frequency Response: -0.15dB (Fs=192000) | - | 20 | - | Hz |

Note: Fs=Sample rate.

9.1.4. SPDIF Input/Output Characteristics

DVDD=3.3V, T_{ambient}=25°C, with 75Ω external load.

Table 83. SPDIF Input/Output Characteristics

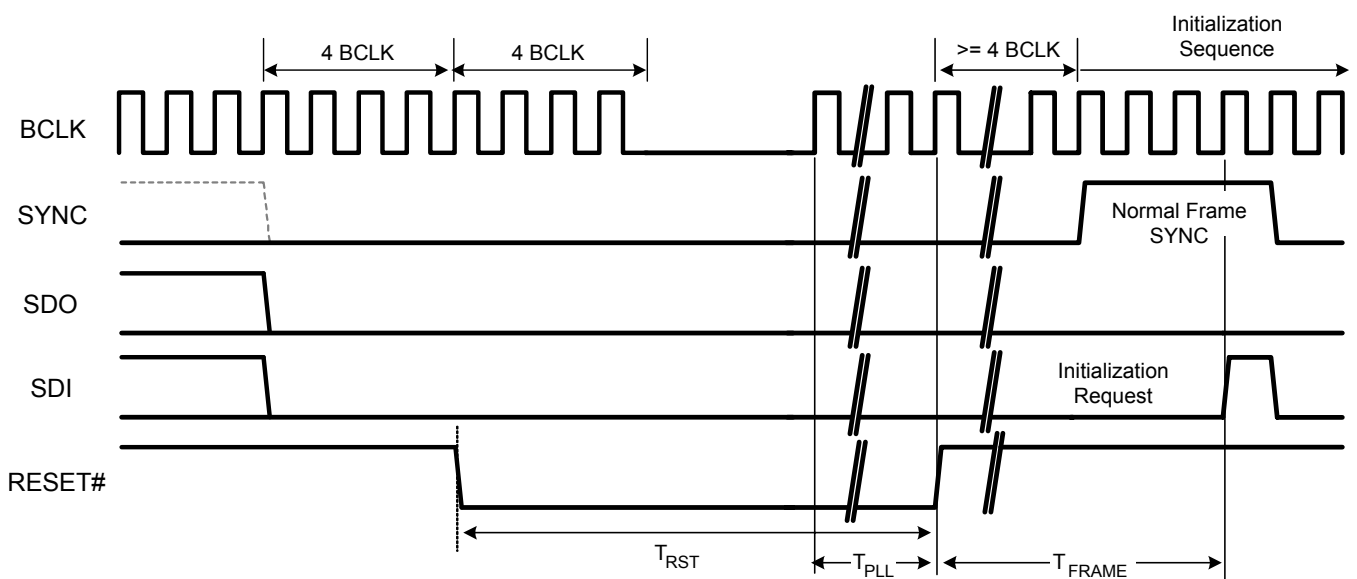
| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|-----------------------------|-----------------|---------|---------|---------|-------|
| SPDIF-OUT High Level Output | V _{OH} | 3.0 | 3.3 | - | V |
| SPDIF-OUT Low Level Output | V _{OL} | - | 0 | 0.3 | V |
| SPDIF-IN High Level Input | V _{IH} | 1.85 | - | - | V |
| SPDIF-IN Low Level Input | V _{IL} | - | - | 1.45 | V |
| SPDIF-IN Bias Level | V _t | - | 1.65 | - | V |

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 84. Link Reset and Initialization Timing

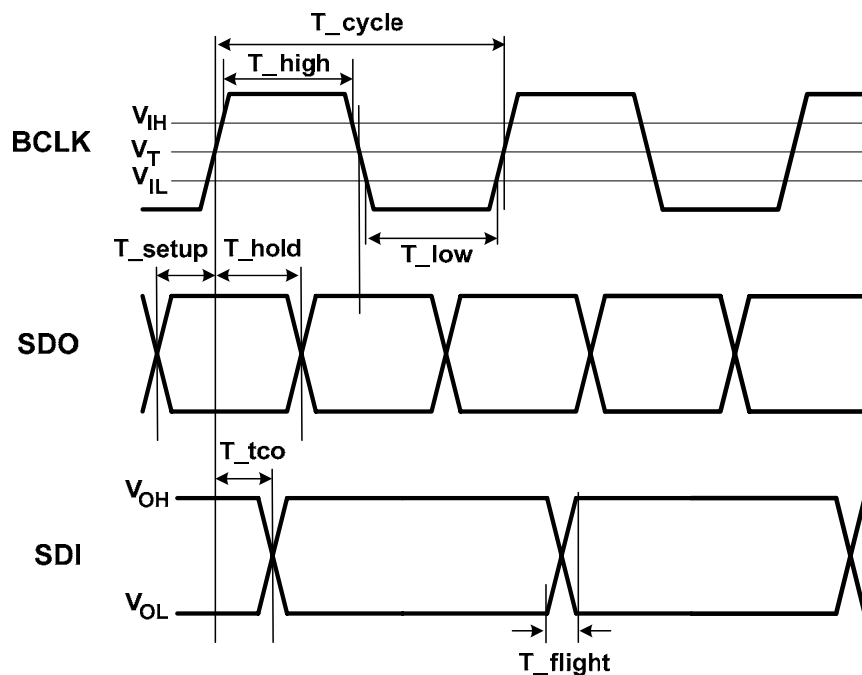
| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|--|-------------|---------|---------|---------|------------|
| RESET# Active Low Pulse Width | T_{RST} | 100.167 | - | - | μs |
| RESET# Inactive to BCLK Startup Delay for PLL Ready Time | T_{PLL} | 100 | - | - | μs |
| SDI Initialization Request | T_{FRAME} | - | - | 25 | Frame Time |


Figure 15. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 85. Link Timing Parameters at the Codec

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---------------------|---------|---------|---------|-------|
| BCLK Frequency | - | 23.9976 | 24.0 | 24.0024 | MHz |
| BCLK Period | T_{cycle} | 41.163 | 41.67 | 42.171 | ns |
| BCLK Jitter | T_{jitter} | - | 150 | 500 | ns |
| BCLK High Pulse Width | T_{high} | 17.5 | - | 24.16 | ns |
| BCLK Low Pulse Width | T_{low} | 17.5 | - | 24.16 | ns |
| SDO Setup Time at Both Rising and Falling Edge of BCLK | T_{setup} | 5 | - | - | ns |
| SDO Hold Time at Both Rising and Falling Edge of BCLK | T_{hold} | 5 | - | - | ns |
| SDI Valid Time After Rising Edge of BCLK (1:50pF External Load) | T_{tco} | 3 | - | 11.0 | ns |
| SDI Flight Time | T_{flight} | 0 | - | 7 | ns |


Figure 16. Link Signals Timing

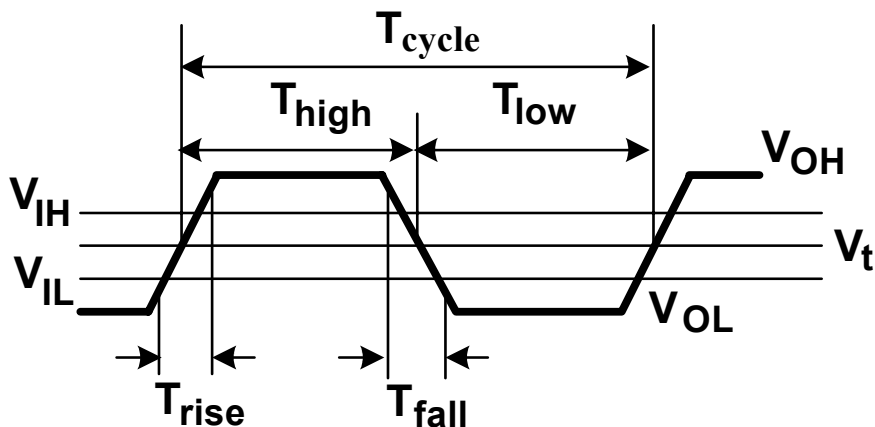
9.2.3. SPDIF Output and Input Timing

Table 86. SPDIF Output and Input Timing

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|-------------------------------|---------------------|-------------|-------------|-------------|--------|
| SPDIF-OUT Frequency | - | - | 3.072 | - | MHz |
| SPDIF-OUT Period ¹ | T_{cycle} | - | 325.6 | - | ns |
| SPDIF-OUT Jitter | T_{jitter} | - | - | 4 | ns |
| SPDIF-OUT High Level Width | T_{High} | 156.2 (48%) | 162.8 (50%) | 169.2 (52%) | ns (%) |
| SPDIF-OUT Low Level Width | T_{Low} | 156.2 (48%) | 162.8 (50%) | 169.2 (52%) | ns (%) |
| SPDIF-OUT Rising Time | T_{rise} | - | 2.0 | - | ns |
| SPDIF-OUT Falling Time | T_{fall} | - | 2.0 | - | ns |
| SPDIF-IN Period ² | T_{cycle} | - | 325.6 | - | ns |
| SPDIF-IN Jitter | T_{jitter} | - | - | 10 | ns |
| SPDIF-IN High Level Width | T_{High} | 146.4 (45%) | 162.8 (50%) | 179 (55%) | ns (%) |
| SPDIF-IN Low Level Width | T_{Low} | 146.4 (45%) | 162.8 (50%) | 179 (55%) | ns (%) |

Note 1: Bit parameters for 48kHz sample rate of SPDIF-OUT.

Note 2: Bit parameters for 48kHz sample rate of SPDIF-IN.


Figure 17. Output and Input Timing

9.2.4. Test Mode

The ALC888S-VD does not support test mode or Automatic Test Equipment (ATE) mode.

9.3. Analog Performance

Standard Test Conditions

- $T_{\text{ambient}}=25^{\circ}\text{C}$, DVDD=3.3V±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz

Table 87. Analog Performance

| Parameter | Min | Typical | Max | Units |
|--|-----|--------------|--------------|--------|
| Full-Scale Input Voltage All Inputs (Gain=0dB) to ADC | - | 1.5 | - | Vrms |
| Full-Scale Output Voltage (Gain=0dB) | | | | |
| DAC | - | 1.2 | - | Vrms |
| Headphone Amplifier Output@32Ω Load | - | 1.1 | - | Vrms |
| Dynamic Range with -60dB Signal (A-Weight) | | | | |
| ADC | - | 92 | - | dB FSA |
| DAC | - | 97 | - | dB FSA |
| Headphone Amplifier Output@32Ω Load | - | 97 | - | dB FSA |
| THD+N with -3dB Signal (No A-Weight) | | | | |
| ADC from Port-C and Port-F | - | -84 | - | dB FS |
| ADC from Other Port Except Port-C and Port-F | - | -85 | - | dB FS |
| DAC to All Port | - | -84 | - | dB FS |
| Headphone Amplifier Output@32Ω Load | - | -75 | - | dB FS |
| Magnitude Response (10KΩ Load) | | | | |
| All DAC @Fs=48KHz (FR=±0.05dB) | 0 | - | 21,792 | Hz |
| All DAC @Fs=96KHz (FR=±0.05dB) | 0 | - | 43,584 | Hz |
| All DAC @Fs=192KHz (FR=±0.05dB) | 0 | - | 87,168 | Hz |
| All ADC @Fs=48KHz (FR=±0.04dB) | 0 | - | 19,200 | Hz |
| All ADC @Fs=96KHz (FR=±0.04dB) | 0 | - | 38,400 | Hz |
| All ADC @Fs=192KHz (FR=±0.04dB) | 0 | - | 76,800 | Hz |
| Power Supply Rejection (Measured at 1kHz Point) | - | -72 | - | dB |
| Amplifier Gain Step | - | 1.0 | - | dB |
| Channel Separation (Crosstalk) | - | -80 | - | dB |
| Input Impedance (Gain=0dB) | - | 64 | - | KΩ |
| Output Impedance | | | | |
| Amplified Output | - | 2 | - | Ω |
| Non-Amplified Output | - | 200 | - | Ω |
| Digital Power Supply Current (Normal/DVD-Audio) DVDD=3.3V | - | 12/28 | - | mA |
| Digital Power Supply Current (D2) DVDD=3.3V | - | - | 1100 | μA |
| Analog Power Supply Current (Normal Operation) AVDD=5.0V | - | 48 | - | mA |
| Analog Power Supply Current (D2) AVDD=5.0V | - | 530 | - | μA |
| VREFOUTx Output Voltage | - | 0.5×LDO-OUT1 | 0.8×LOD-OUT1 | V |
| VREFOUTx Output Current | - | 5 | - | mA |

10. Application Circuits

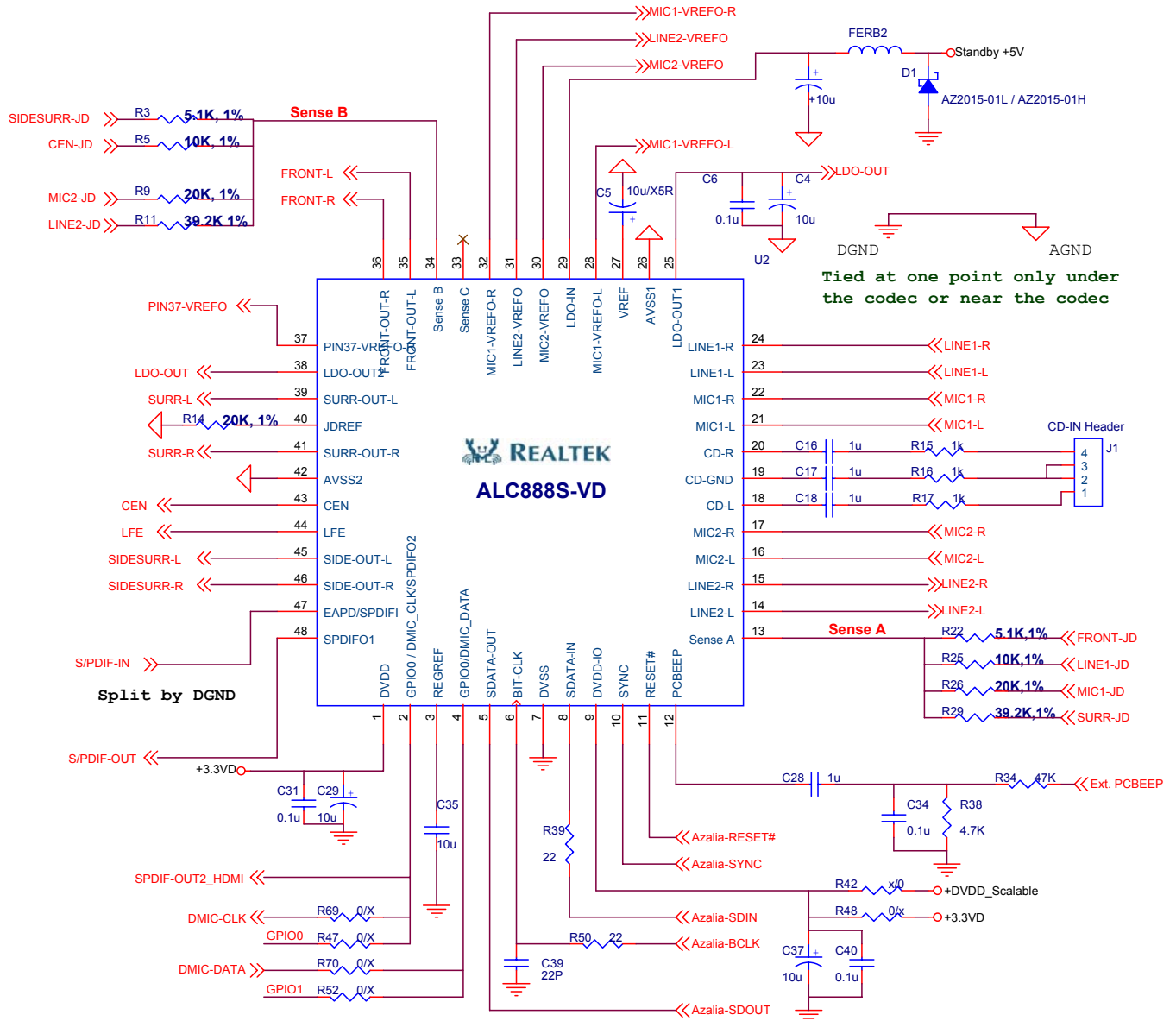
To get the best compatibility in hardware design and software driver, any modification should be confirmed with Realtek. Realtek may update the latest application circuits onto our web site (www.realtek.com) without modifying this datasheet.

10.1. Desktop System

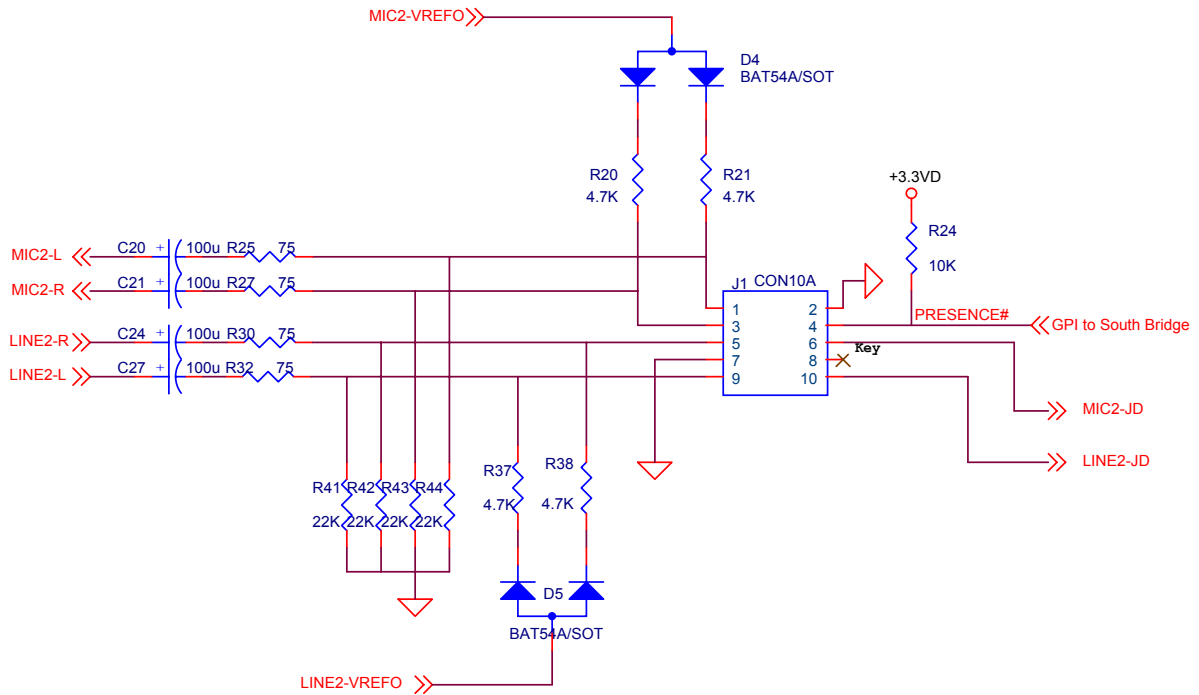
This following pages show an example of a 7.1 channel output desktop system with three analog jacks on the rear panel, and with two re-tasking analog jacks on the front panel.

Table 88. Desktop System

| Analog Port | Pin | Location | Function Description |
|---------------------|--------|-------------|--|
| FRONT (Port-D) | 35, 36 | Rear Panel | Front Channel Line Output and Amplified Output. |
| SURR (Port-A) | 39, 41 | Rear Panel | Surround Channel Line Output. |
| CENTER/LFE (Port-G) | 43, 44 | Rear Panel | Center and Low Frequency (Sub-Woofers) Channel Line Output. |
| SIDE (Port-H) | 45, 46 | Rear Panel | Side Surround Channel Line Output. |
| MIC1 (Port-B) | 21, 22 | Rear Panel | Analog Microphone Input. |
| LINE1 (Port-C) | 23, 24 | Rear Panel | Analog Line Input. |
| LINE2 (Port-E) | 14, 15 | Front Panel | Re-Tasking Jack Supports Headphone Out (Default), Microphone Input, and Line Input. |
| MIC2 (Port-F) | 16, 17 | Front Panel | Re-Tasking Jack Supports Microphone Input (Default), Line Input, and Headphone Output. |



AUDIO FRONT HEADER



HD Audio Front Panel I/O Module

PORT-E (LINE2) and PORT-F (MIC2) are front panel I/O

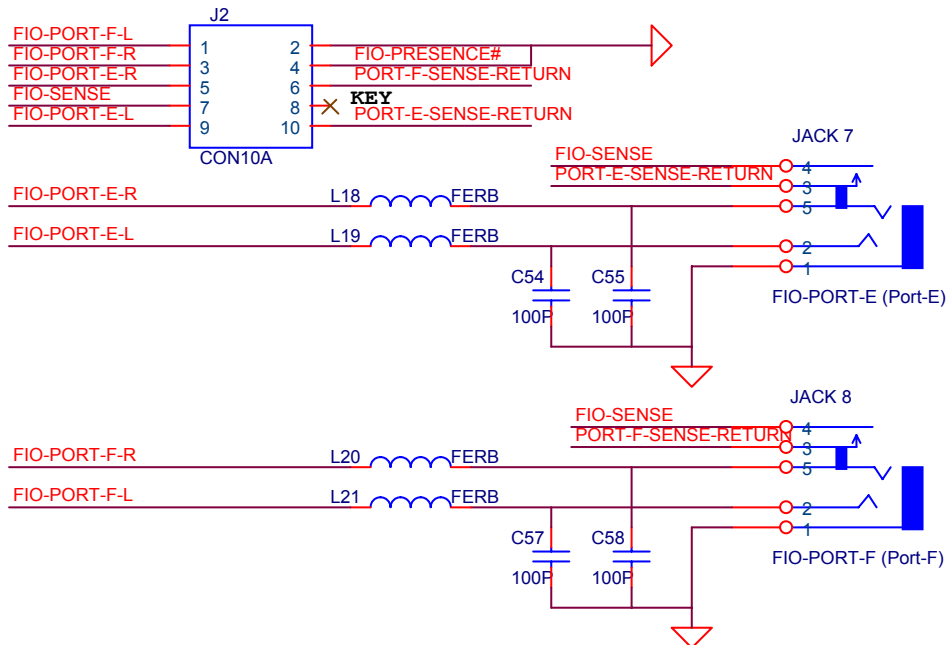
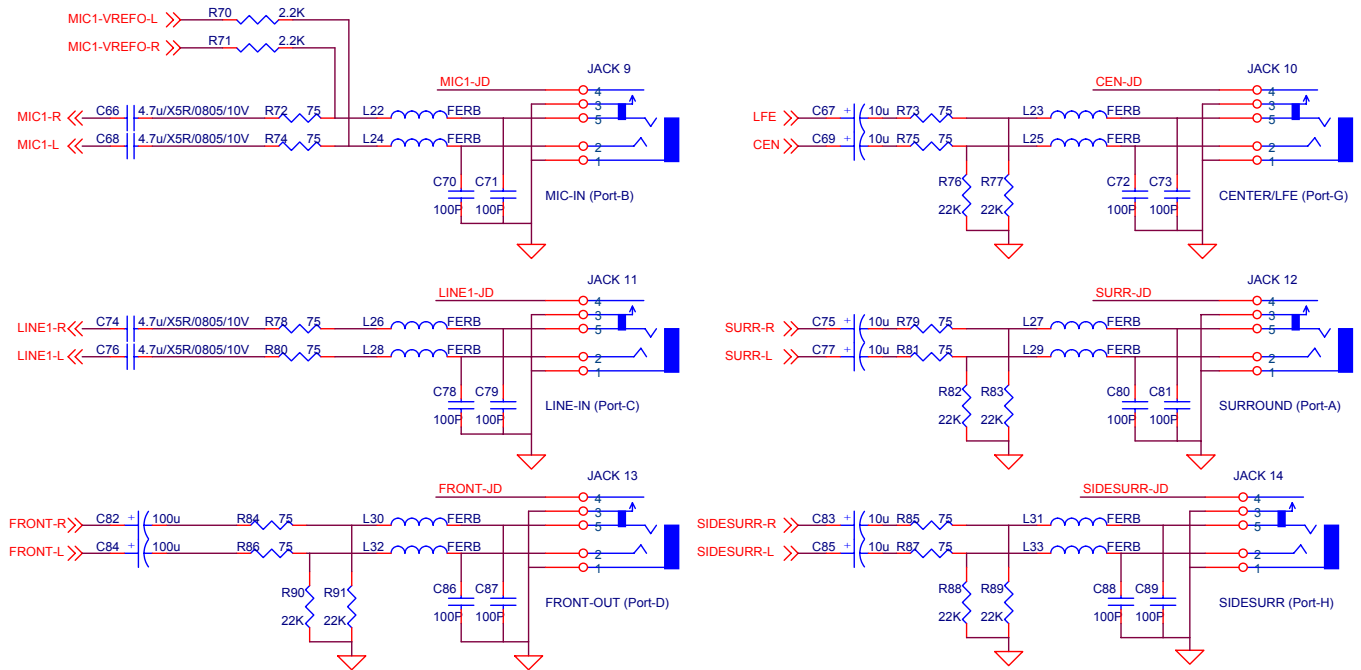
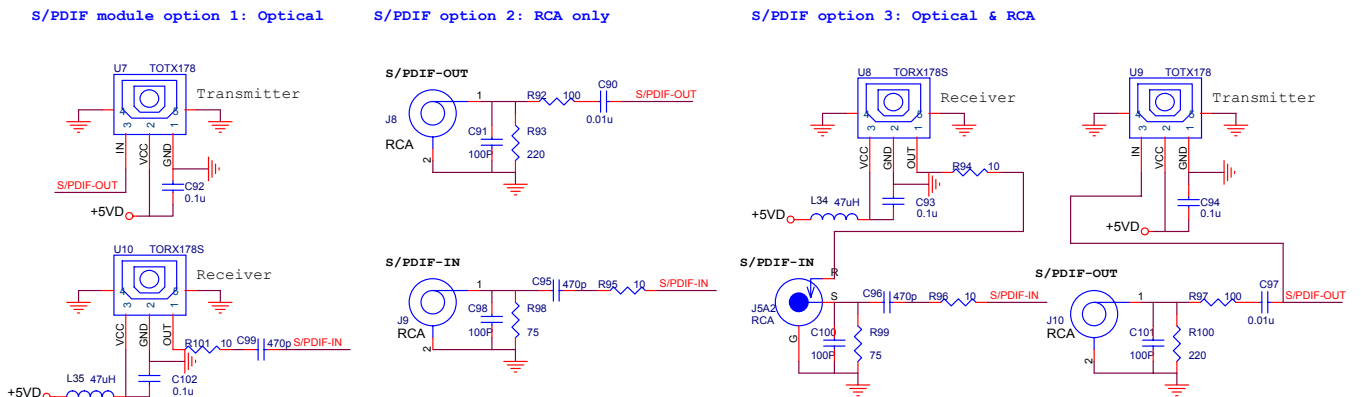


Figure 19. Front Panel Header and Front Panel Module Connection

ANALOG I/O CONNECTOR

Figure 20. Jack Connection at Rear Panel

Figure 21. SPDIF Input/Output Connection

11. Application Supplements

11.1. Standby Mode

In standby mode the ALC888S-VD turns on DC bias on all analog input and output ports (NID=14h~1Bh). This is a special application to avoid ‘Pop’ noise while the system is in power on and power off transition stages.

Table 89 shows the DC bias state when Standby mode is enabled.

Table 89. Standby Mode

| +3.3V on DVDD (Pin-1) | +5VA on AVDD | Operation Mode |
|------------------------------|---------------------|-----------------------|
| No (<2.0V) | No | Shut Down |
| No (<2.0V) | Yes | Standby Mode |
| Yes (>2.0V) | No | Normal |
| Yes (>2.0V) | Yes | Normal |

11.2. Digital Microphone Implementation

This section describes the ALC888S-VD digital microphone implementation. There is one Clock output pin and 1 Data input pin in the ALC888S-VD. The ALC888S-VD provides the clock signal to the digital microphone. When the digital microphone receives the external sound input, it converts the analog signals to digital in a 1-bit format. The 1-bit data is delivered to the codec through the data input pin. The Digital Filter in the audio codec converts the 1-bit data stream into Pulse Code Modulation (PCM) data. The PCM data is sent to the HDA controller through the HDA link.

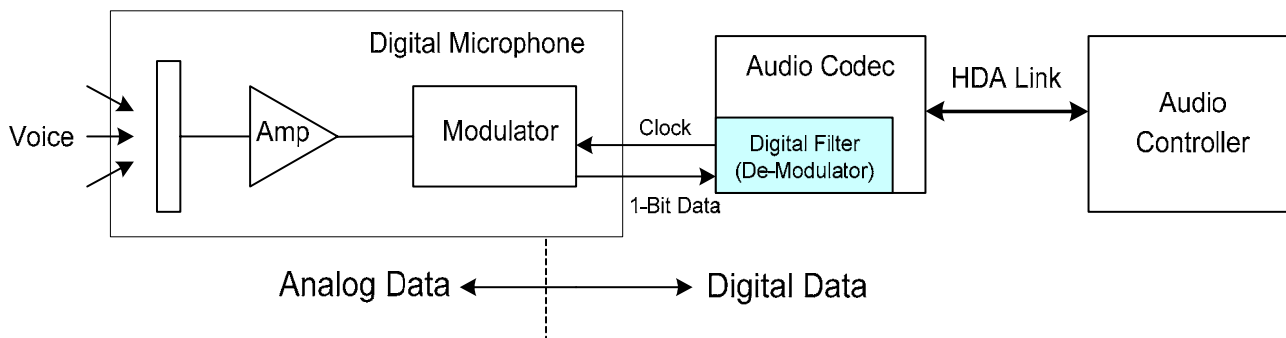


Figure 22. Digital Microphone Implementation

The ALC888S-VD supports a two-wire interface for the digital microphone and operates in single-channel (mono type) or stereo-channel mode. One pin is clock output to the digital microphone, and the other is a serial pin. The default clock output is 2.048MHz.

The ALC888S-VD uses one data pin to support stereo inputs from various digital microphones and microphone module. Popular digital microphones provided from Fortemedia, Akustica, Knowles, and Hosiden are supported. Please contact Realtek and your digital microphone vendor to get the best compatibility between the ALC888S-VD and various digital microphones.

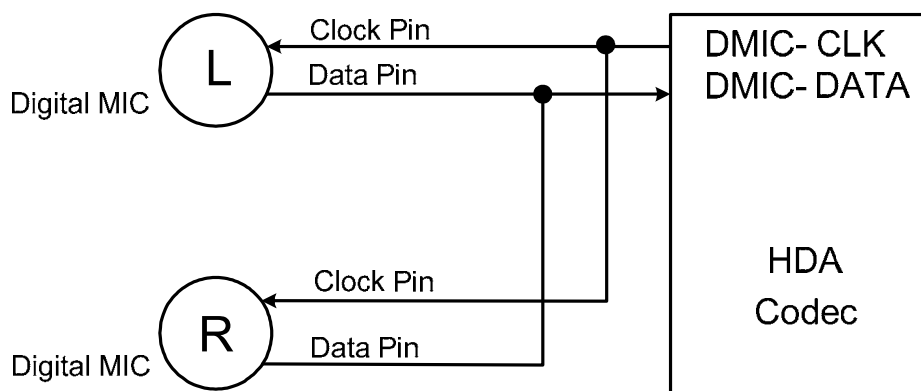
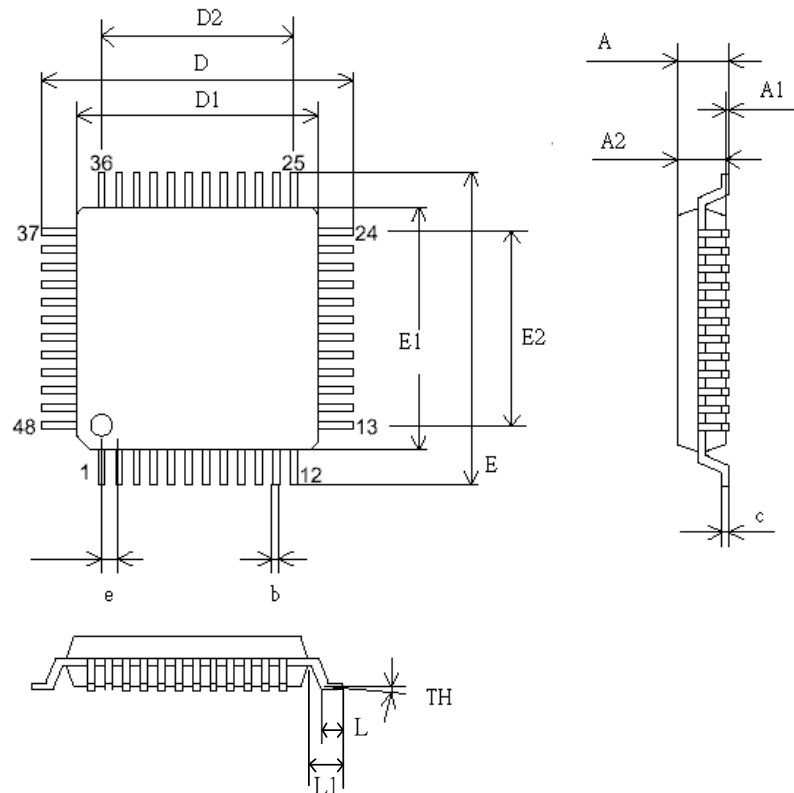


Figure 23. Stereo Digital Microphone Connection

12. Mechanical Dimensions



| SYMBOL | MILLIMETER | | | INCH | | |
|--------|------------|------|------|------------|--------|-------|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| A | - | - | 1.60 | - | - | 0.063 |
| A1 | 0.05 | - | 0.15 | 0.002 | - | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| c | 0.09 | - | 0.20 | 0.004 | - | 0.008 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 7.00 BSC | | | 0.276 BSC | | |
| D2 | 5.50 | | | 0.217 | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 7.00BSC | | | 0.276 BSC | | |
| E2 | 5.50 | | | 0.217 | | |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC | | | 0.0196 BSC | | |
| TH | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.0236 | 0.030 |
| L1 | - | 1.00 | - | - | 0.0393 | - |

| | | | |
|--------------------------------|--|----------|----------|
| TITLE: LQFP-48 (7.0x7.0x1.6mm) | | | |
| PACKAGE OUTLINE DRAWING, | | | |
| FOOTPRINT 2.0mm | | | |
| LEADFRAME MATERIAL | | | |
| APPROVE | | DOC. NO. | |
| | | VERSION | 02 |
| CHECK | | DWG NO. | PKGC-065 |
| | | DATE | |
| REALTEK SEMICONDUCTOR CORP. | | | |

13. Ordering Information

Table 90. Ordering Information

| Part Number | Description | Status |
|----------------|------------------------------|------------|
| ALC888S-VD2-GR | LQFP-48 with 'Green' Package | Production |

Note: See page 7 for 'Green' package and version identification.

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