RTL8100C(L) Series

SINGLE-CHIP FAST ETHERNET CONTROLLER WITH POWER MANAGEMENT

LAYOUT GUIDE

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the Realtek RTL8100C or RTL8100CL Single-Chip Fast Ethernet Controller with Power Management.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/12/17	First release.

Table of Contents

List of Tables

List of Figures

1. Introduction

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration and Power Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System-Directed Power Management (OSPM) to achieve the most efficient power management possible.

In order to achieve maximum performance using the RTL8100C(L), good design attention is required throughout the design and layout process. Following these rules will contribute greatly to a proper functioning hardware system. All information provided in this guide has been tested by Realtek System Engineers to be accurate and directly applicable to the system design

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8100C(L). Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8100C(L).

(3) Simplify the task of routing signal traces.

In order to achieve maximum performance using the RTL8100C(L), good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8100C(L), good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify that critical components such as the clock source and transformer meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (10µF-22µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8100C(L) chip.

- Provide termination on all high-speed switching signals.
- Route the signal trace as short as possible.
- Use a smaller package for the capacitor to reduce the package inductance.

Use the following signal integrity techniques to reduce crosstalk.

- Shorter parallel route
- Wider ground plane spacing between signal wires
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane

2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane if possible.
- 50-ohm impedance match resisters and 0.1uF common mode noise filter capacitors should be placed near the RTL8100C(L) chip.
- Avoid right angle signal traces. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

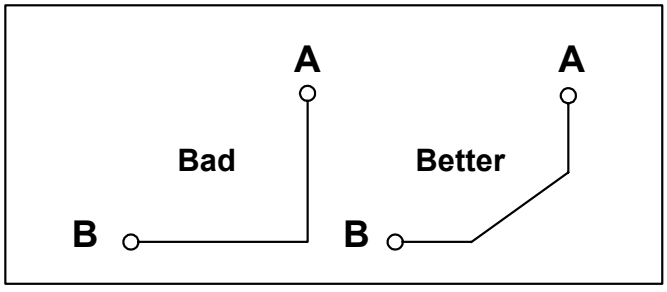

Figure 1. Signal Trace Angles

3. Major Components Placement

Components placement should be carefully considered in order to optimize and shorten the routing traces.

3.1. RTL8100C(L)

- The RTL8100C(L) should be placed as close as possible to the 10/100M magnetic (Less than 12cm recommended).
- The RTSET (Pin 127) resistor should be placed near to the RTL8100C(L) but away from signal traces (i.e. TX+/-; RX+/-) and Clock signals as far as possible.

3.2. Magnetics

- The 10/100M magnetics should be placed as close as possible to the RJ-45 connector.
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other

3.3. Crystal

- The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx, power), magnetics, and board edges.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI.
- The retaining straps of the OSC, if any, need good grounding.

3.4. Termination Resistors & Capacitors

The transmitting resistors and capacitors (Figure 2, page 4) should normally be placed close to the RTL8100C(L) chip. The receiving resistors and capacitors (Figure 2, page 4) should be placed close to the 10/100M magnetics. However, these resistors & capacitors should be chosen carefully for impedance matching compatibility.

In certain cases, the placing of transmitting resistors and capacitors (Figure 2, page 4) should be consistent with trace layout. For example, signal trace layouts in the interior layer with width/spacing 4/8/4, based on simulation results (Table 1) show that the longer the traces, the more necessary to place termination resistors close to the magnetics.

Table 1. Signal Trace Layout Simulation

Trace Width/Spacing (4/8/4)	Rise Time	
	Block A Close to RTL8100C(L)	Block A Close to Magnetics
Length=1000mil	3.2229ns	3.2085ns
Length=1600mil	3.2389ns	3.1453ns
Length=2000mil	3.2497ns	3.1054ns

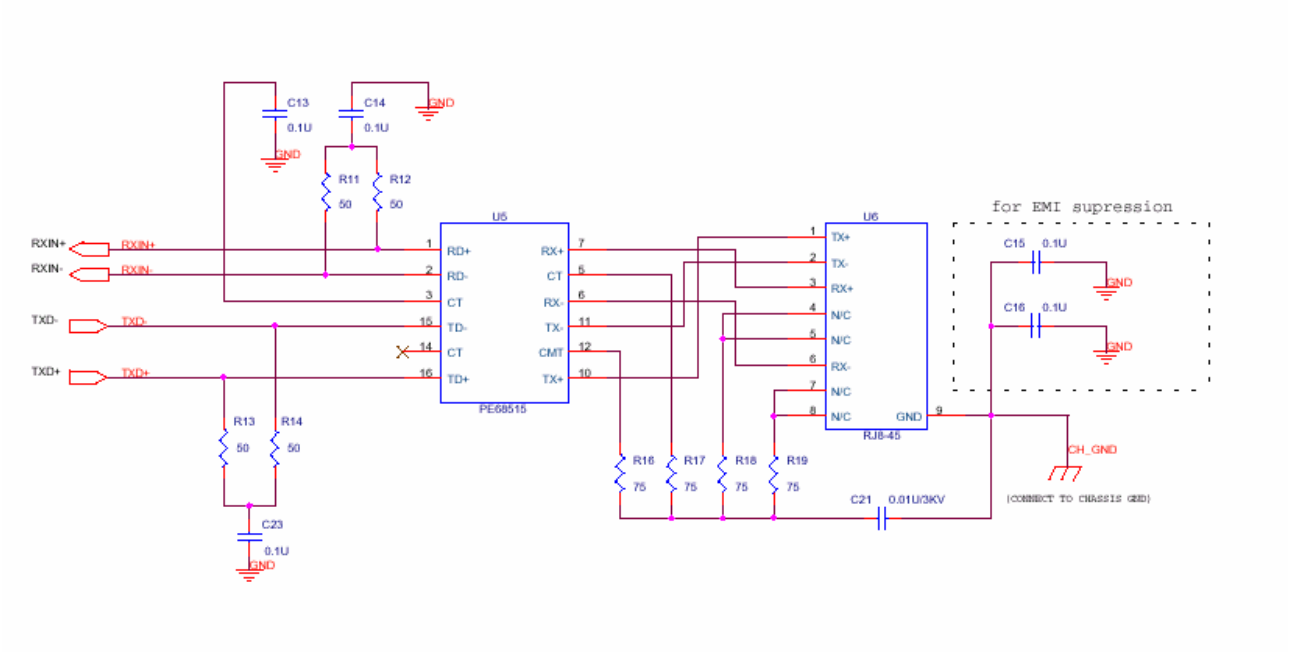

Figure 2. Layout

3.5. Ferrite Beads and De-Coupling Capacitors

- Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors (Z5U, Y5V types are recommended) should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

4. Signal and Trace Routing

Noise, ringing, and data lines have to be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, cross-talk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Traces routed from the RTL8100C(L) to the 10/100 magnetics, and to the RJ-45 connector, should be as short as possible. It is also very important to keep both differential pair signal traces (TX+/- & RX+/-) equal in length. The traces should be placed close to each other (D1 in Figure 3) as they provide a strong canceling effect on noise. However, it is very important to keep TX and RX signal pair traces apart (D2 in Figure 3).

Note: D1 <2mm and D2 >3mm.

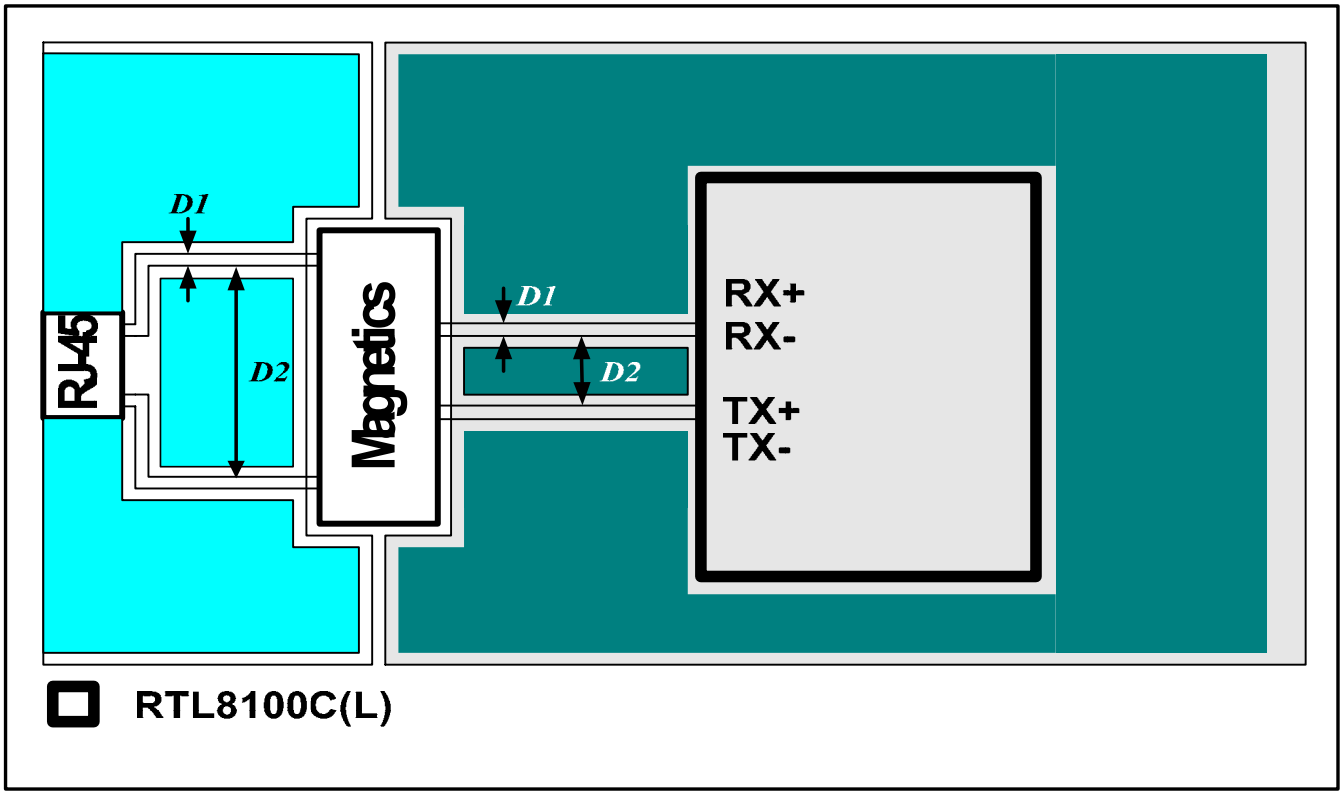

Figure 3. Signal and Trace Routing

- Ground Plane shielding can be used to separate both pairs. A good layout should avoid intersection of pairs of signal traces. A good layout should also avoid the following:

  a. Intersection of TX+/- and RX+/- Signal Traces

  b. Intersection of TX+ and TX- Signal Traces

  c. Intersection of RX+ and RX- Signal Traces

- RX +/- signal traces should not use vias. It is better to keep RX+/- traces on the component side.

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them.
- The Length of a signal trace should not exceed 1/20 of the highest harmonic (about one 10th) wavelength. For example, the 25MHz clock trace should not exceed 20cm and the 125MHz signal traces (TX+/-; RX+/-) should not exceed 12cm.
- It is important to separate Digital Signals (e. g., BROM, Flash, CLK) from Analog Signals (e. g., TX+/-, RX+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles.
- The power into the RTL8100C(L) digital power pins can be improved with de-coupling capacitors. The Power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8100C(L) need to be de-coupled with a capacitor. The de-coupling capacitors should be placed as close to the IC as possible and the traces should be kept short.
- The traces between the transistor for supplying DVDD25 (i.e., Transistor to VCTRL & DVDD25 pins) should be kept as short and wide as possible to provide a cleaner digital and analog 2.5V power supply. Also, keeping the 22µF and 0.1µF capacitor close to the transistor is very important. We recommend the use of tantalum capacitors.

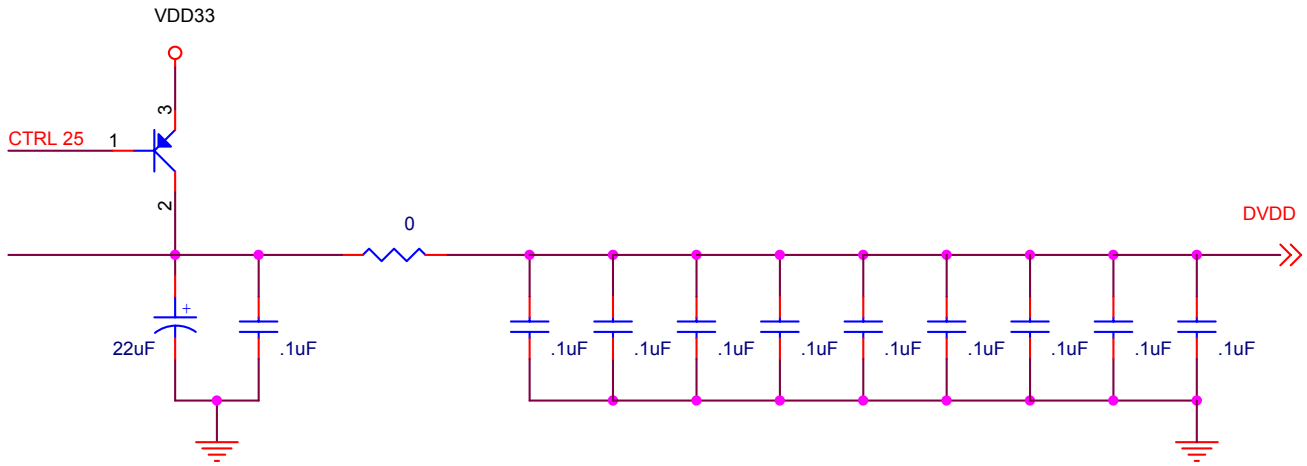

Figure 4. Power Transistor Traces

5. Power Supply and Ground Plane

5.1. Power Plane Partition

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. Analog circuitry on the same plane as the digital power area will experience energy fluctuation due to the fast switching time of digital components. This phenomenon could improperly bias the transistors, and cause the circuits to malfunction. It is recommended to use at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8100C(L). If it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

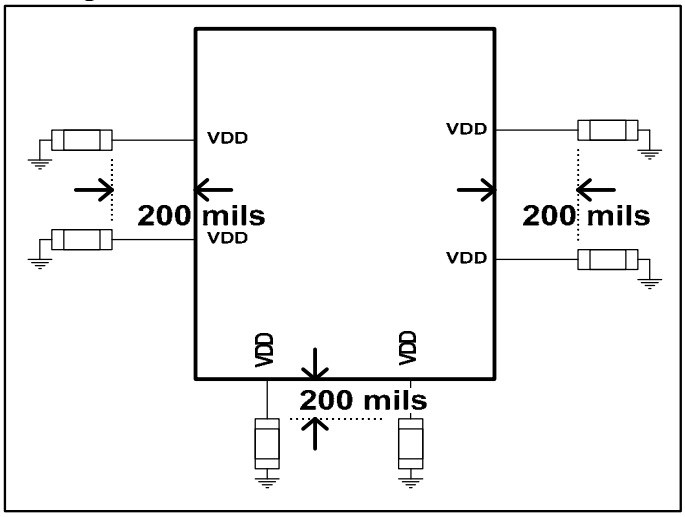

Figure 5. Decoupled Capacitor Example

(b) Use a Ferrite Bead to Connect Digital and Analog Power

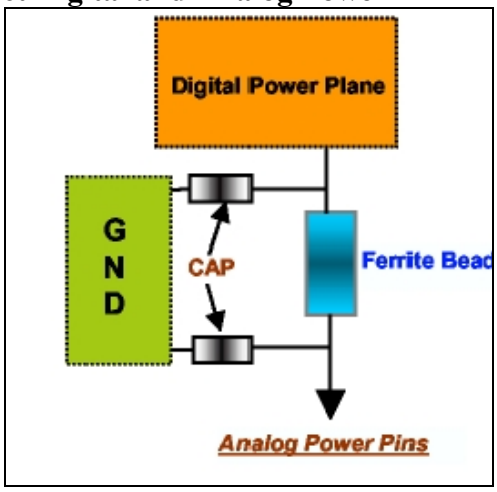

Figure 6. Ferrite Bead

To further improve the performance of the power plane, try to keep the contact area between the RTL8100C(L) VDD pins and power plane as large as possible rather than using small narrow traces (Figure 7).

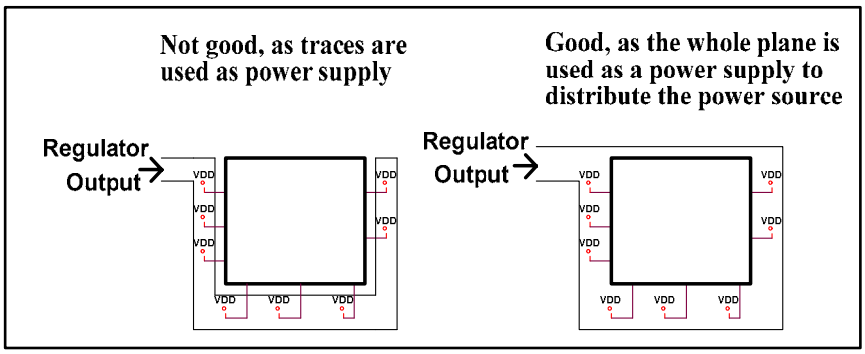

Figure 7. Power Source Distribution

5.2. Ground Plane Layout

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

To achieve better GND plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 8 illustrates a not so good (left) and a good ground plane layout (right).

Figure 8. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer induced noise away from the power and system ground planes (Figure 9).

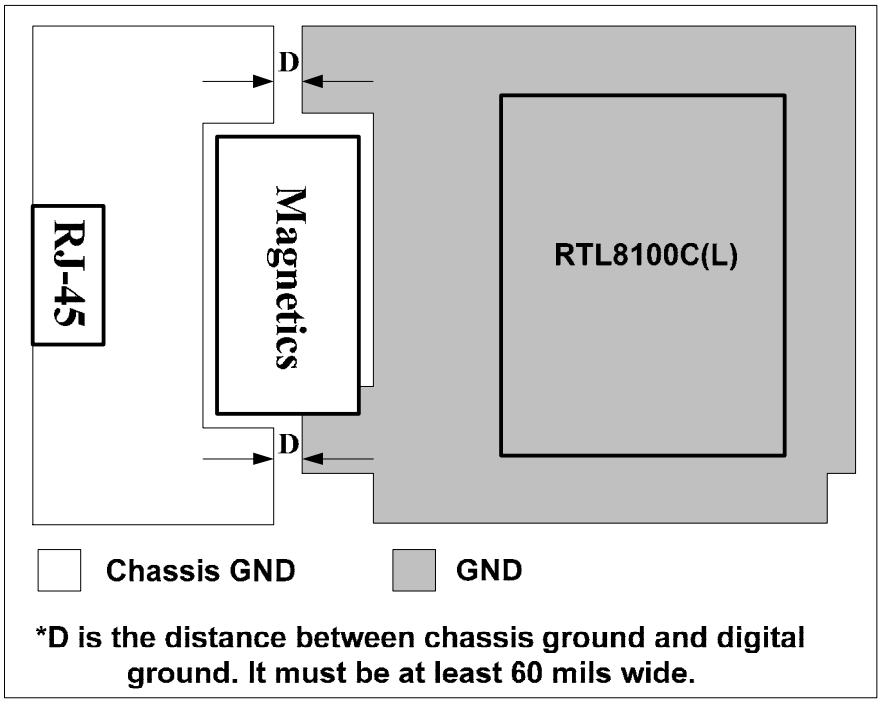

Figure 9. Ground Plane Separation

The Chassis Ground as shown in Figure 9 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is also important to keep the gap (D in Figure 9) between Chassis GND and System GND wider than 60 mils for better isolation.

6. Parts Recommendations

6.1. 10/100M Magnetics

Table 2. 10/100M Magnetics

Turn Ratio Tx/Rx:	1:1
Primary Inductance:	350µH OCL with 8mA bias
Insertion Loss:	-1.0dB Max, 1 ~ 100MHz
Return Loss:	-18dB Min @ 100Ω, 1 ~ 30MHz -14dB Min @ 100Ω, 30 ~ 60MHz -12dB Min @ 100Ω, 60 ~ 80MHz
Differential to Common Mode Rejection:	-40dB Min @ 1 ~ 60MHz -30dB Min @ 60 ~ 100MHz
Hi-Pot:	1500Vrms @ 60sec
Operating Temperature:	0°C to 70°C

6.2. Recommended Magnetics

Table 3. Recommended Magnetics

Manufacturer	Part Number
Pulse Engineering	H1267, H1281 (Gigabit Pin-Compatible)
Belfuse	S558-5999-46
Delta	LF8527
Both Hand	BH16ST8515
YCL	20PMT04

6.3. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to X1 (Pin121, XTAL1) and X2 (Pin122, XTAL2), and shunt each crystal lead to ground with a 27pF capacitor.

Table 4. Reference Clock

Parameter	Conditions
Nominal Frequency	25.000MHz
Oscillation Mode	Base wave
Frequency Tolerance at 25℃	±50ppm
Temperature Stability	±50ppm
Operating Temperature Range	-10℃～+70℃
Equivalent Series Resistance	30Ohm Max.
Drive Level	0.1mV
Load Capacitance	20pf
Shunt Capacitance	7pf Max.

Parameter	Conditions
Insulation Resistance	Mega Ohm Min./DC 100V
Test Impedance Meter	Saunders 250A
Aging Rate Per Year	±0.0003%

6.4. Resistors

Resistors that have tolerance requirements within 1%, are strongly recommended. Refer to the BOM for suggested schematics.

6.5. Capacitors

- Use Electrolytic capacitors for large value and low frequency de-coupling
- Use X7R and C0G capacitors for small value and high frequency de-coupling and use Y5V capacitors for critical temperature requirements
- For power filtering, low ESR Tantalum capacitors are recommended for the power circuit and use X7R dielectric capacitors of several uF correspondingly to reduce the power ripple significantly. Refer to the provided BOM for suggested schematics.

6.6. Ferrite Bead

The ferrite bead used should be of at least 100Ω@100MHz impedance with a rated current of 300mA or over.

6.7. Power Transistors

The RTL8100C(L) works with current rates of around 150mA. We recommended using components that have a current rate 2 to 3 times greater than this value. It is important to select a transistor that has sufficient current rate for this particular circuit. The beta (β) value should be as large as possible (i.e., $\beta > 150$)

6.8. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

7. Special Notes

- The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for 2-layer layouts.
- If a 5v EEPROM is used, the layout should include Power Down & Power Source traces. If a 3.3V EEPROM is used, ensure the Power Pin of the EEPROM is connected to the RTL8100C(L)'s 3.3v pin
- If it is found that there is a serious EMI issue during read/write operations from the PCI 33/66 MHz interface, some de-coupling capacitors (0.047uF, 22uF) can be added between the system GND and power planes.
- For legacy WOL applications, please note the WOL connector specification for the system. The WOL connector specification must match the WOL connector of the motherboard where the system will be used.
- When using the oscillator as the clock source for 25MHz, avoid connecting any capacitors to the clock circuitry.
- The digital bus traces for PCI, BOOTROM, and EEPROM should have lengths as equal as possible to achieve proper skew rate requirements, especially for PCI 66MHz/64-bit application.
- Routing the PCI clock trace longer than bus traces in order to gain some setup time is not recommended (though it can be done). The digital functionality of the IC is robust enough that there is no need to route the PCI clock in this manner.
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions.
- Applying a bead on a 2.5v power trace may cause serious power ripple to analog power, and effect performance.
- Applying a 0.1µF to TCT (Tx Center Tap) may cause unanticipated interoperability issues.

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