RTL8102E-GR
RTL8102EL-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

EEPROM-Less APPLICATION NOTES

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/11/01	First release.
1.1	2008/04/28	Added section 3, Enabling EEPROM-Less Operation, page 1.

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1. Introduction

This application note helps board designers to implement an EEPROM-less Realtek PCI-E RTL8102E(L)-GR Fast Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single chip PCI-E RTL8102E(L)-GR Fast Ethernet controller. Those points are listed below and are detailed in the following sections.

- LAN MAC Address Programming
- SDID/SVID Programming (If necessary)
- LED Mode Configuration
- Serial Number
- PXE Driver

3. Enabling EEPROM-Less Operation

For the RTL8102E(L)-GR to operate properly without EEPROM or eFUSE auto-load, the following steps must be followed:

A. Isolate disable LAN: Write 14h to I/O register offset 55h via byte access

B. CLKREQ:

Step1: Write I/O register offset 53h Bit_7 to 1'b

Step2: Write I/O register offset 55h Bit_2 & Bit_4 to 1'b

Step3: Write I/O register offset D1h Bit_4 to 1'b

Step4: Enable LAN Active State Power Management (ASPM) capability in PCI Configuration register offset 80h Bit_0 & Bit_1 to 1'b

Step5: Enable CLKREQ capability in PCI Configuration register offset 81h Bit_0 to 1'b

4. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM or eFUSE memory and stored in the RTL8102E(L)-GR. The BIOS must provide the MAC address to the RTL8102E(L)-GR each boot time. The RTL8102E(L)-GR will hold the MAC address until AC power off (pulling PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable 'register protection'.

Step2: Write 33221100h to I/O register offset 0x00 via double word access.

Step3: Write 00005544h to I/O register offset 0x04 via double word access.

Step4: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'.

5. SID/SVID Programming (If Necessary)

The default RTL8102E(L)-GR SID/SVID value is 8136/10EC. If the board layer designer wants to change the value, please follow the steps below:

If SID=8136h, SVID=10ECh:

Step1: Write 813610ECh to I/O register offset 0x64 via double word access.

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Note: When the RTL8102E(L)-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

6. LED Mode Configuration

The RTL8102E(L)-GR supports three LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK10/100. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists. The LEDS1-0 are I/O register 0x52 bit7:6.

Table 1. LEDs

Symbol	Type	64-Pin	48-Pin	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the 93C46.
If there is no 93C46, the default value of the (LEDS1, LEDS0)=(0, 0).

6.2. Rx LED

In 10/100Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

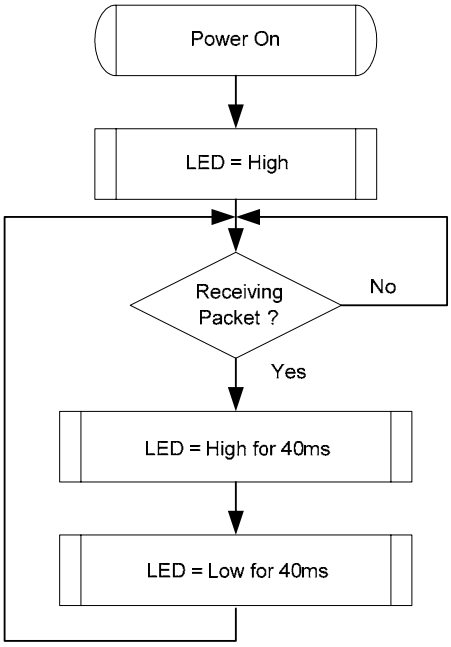

Figure 1. Rx LED

6.3. Tx LED

In 10/100Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

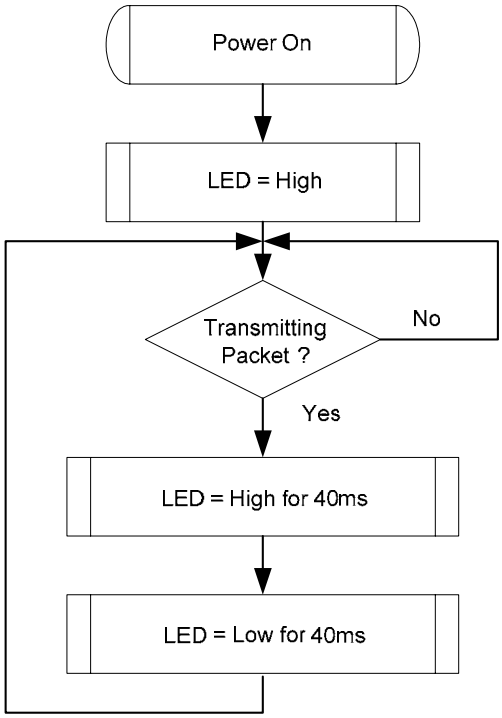

Figure 2. Tx LED

6.4. LINK LED

In 10/100Mbps mode, blinking of the LINK LED indicates that the RTL8102E(L)-GR is linked properly. When this LED is high for extended periods, it indicates that a link problem exists.

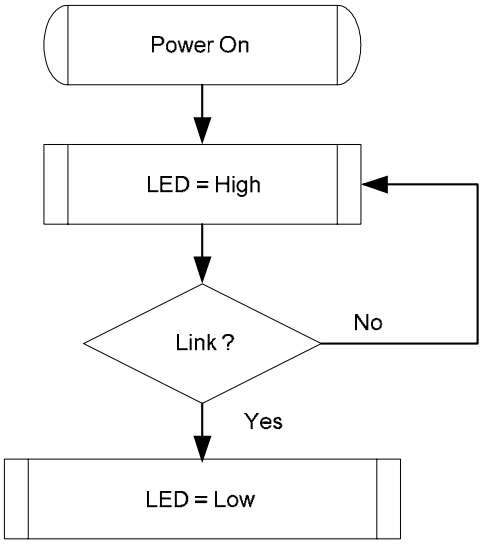

Figure 3. LINK LED

6.5. Tx/Rx LED

In 10/100Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

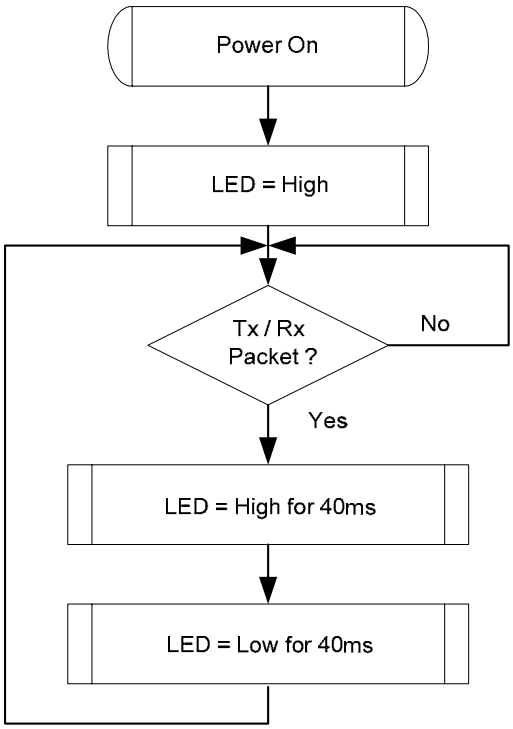

Figure 4. Tx/Rx LED

6.6. LED Mode Configuration

The default value of the RTL8102E(L)-GR LEDS1-0 is 00b. If the board layer designer wishes to change the value, please follow the steps below:

Step1: Write C0h to I/O register offset 0x50 via byte access to disable 'register protection'.

Step2: Write xx001111b to I/O register offset 0x52 via byte access (bit7 is LEDS1 and bit6 is LEDS0; refer to the datasheet to find which mode you need).

Step3: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'.

7. Serial Number

Due to the EEPROM-less design goal, the serial number cannot be loaded from EEPROM and stored in the RTL8102E(L)-GR. The BIOS must provide the serial number to the RTL8102E(L)-GR each boot time.

If the serial number is 00E04C3612345678h:

Step1: Write 364CE000h to I/O register offset 0x64 via double word access.

Step2: Write 8000F164h to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Step4: Write 78563412h to I/O register offset 0x64 via double word access.

Step5: Write 8000F168h to I/O register offset 0x68 via double word access.

Step6: Wait for 1ms.

Note: When the RTL8102E(L)-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

8. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below:

Table 2. PXE Parameters

Bit	Symbol	RW	Description	
7:6	Boot Protocol	RW	00: PXE protocol	01: RPL protocol
5:4	Boot order	RW	00: ROM disable 10: Int 19h	01: Int 18h 11: PnP/BEV(BBS)
3:0	-	-	Reserved	

Note1: When the EEPROM-less feature is implemented, the RTL8102E(L)-GR cannot WOL from '1st AC power-on'.
Note2: When the RTL8102E(L)-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

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