RTL8103E(L)-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

EEPROM-Less APPLICATION NOTES

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed application information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/11/10	First release.

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1. Introduction

This application note will help board designers to implement an EEPROM-less Realtek PCI-E RTL8103E(L)-GR Fast Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single-chip PCI-E RTL8103E(L)-GR Fast Ethernet controller. Those points have been categorized as below and are detailed in the following chapters.

- LAN MAC Address Programming
- DID/VID Programming (if necessary)
- SDID/SVID Programming (if necessary)
- LED Mode Configuration
- PXE Driver

3. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8103E(L)-GR. The BIOS must provide the MAC address to the RTL8103E(L)-GR each boot time. The RTL8103E(L)-GR will hold the MAC address until AC power off (pulling PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write the C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write the 33221100h to I/O register offset 0x00 via double word access

Step3: Write the 00005544h to I/O register offset 0x04 via double word access

Step4: Write the 00h to I/O register offset 0x50 via byte access to enable 'register protection'

4. DID/VID Programming (If Necessary)

The default DID/VID value of the RTL8103E(L)-GR is 8136/10EC. If the board layer designer wants to change the value, please follow the steps below:

If VID=10ECh, DID=8136h:

Step1: Write the 813610EC h to I/O register offset 0x64 via double word access

Step2: Write the 8000F000h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

5. SID/SVID Programming (If Necessary)

The default SID/SVID value of the RTL8103E(L)-GR is 8136/10EC. If the board layer designer wants to change the value, please follow the steps below:

If SVID=10ECh, SID=8136h

Step1: Write the 813610ECh to I/O register offset 0x64 via double word access.

Step2: Write the 8000F02Ch to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

6. LED Mode Configuration

The RTL8103E(L)-GR supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.1. Link Monitor

The Link Monitor senses link integrity (LINK10, LINK100, LINK10/100, LINK10/ACT, LINK100/ACT). Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists. The LEDS1-0 are I/O register 0x52 bit7-6.

Table 1. LEDs

Symbol	Type	Pin No	Description				
LED0	O	40	LEDS1-0	00	01	10	11
LED1	O	39	LED0	Tx/Rx	LINK10/ACT	Tx	LINK10/ACT
LED2	O	36	LED1	LINK100	LINK100/ACT	LINK	LINK100/ACT
LED3	O	35	LED2	LINK10	FULL	Rx	FULL
			LED3	NA	NA	FULL	NA

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the 93C46. If there is no 93C46, the default value of the (LEDS1, LEDS0) = (1, 1).

6.2. Rx LED

In 10/100Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

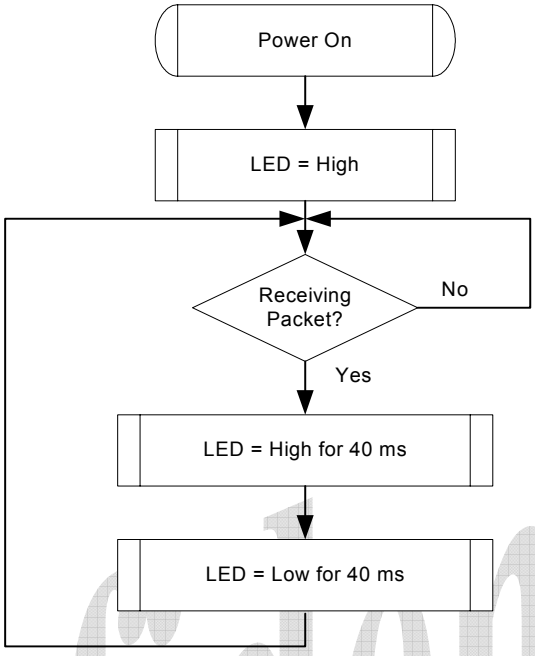

Figure 1. Rx LED

6.3. Tx LED

In 10/100Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

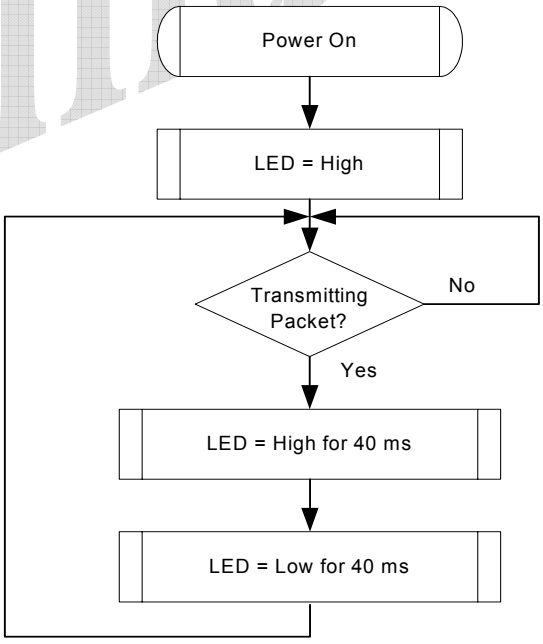

Figure 2. Tx LED

6.4. LINK/ACT LED

In 10/100Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8103E(L)-GR is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

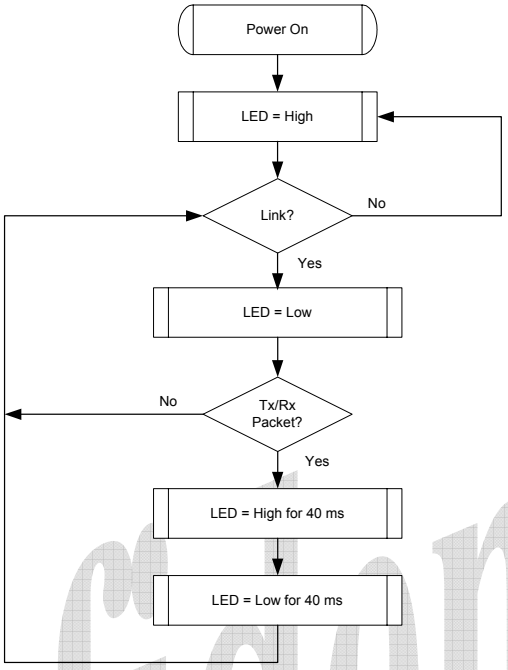

Figure 3. LINK/ACT LED

6.5. Tx/Rx LED

In 10/100Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

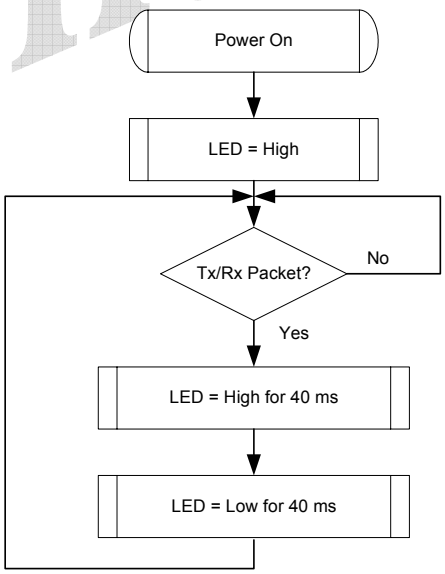

Figure 4. Tx/Rx LED

6.6. LED Mode Configuration

The default value of the RTL8103E(L)-GR LEDS1-0 is 11b. If the board layer designer wishes to change the value, please follow the steps below:

Step1: Write C0h to I/O register offset 0x50 via byte access to disable 'register protection'

Step2: Write xx001111b to I/O register offset 0x52 via byte access (bit7 is LEDS1 and bit6 is LEDS0; refer to the datasheet to find which mode you need)

Step3: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'

7. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below:

Table 2. PXE Parameters

Bit	Symbol	RW	Description
7-6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5-4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3	Show Config Message	RW	0: Enable 1: Disable
2	Shift+F10 Menu Entry	RW	0: Enable 1: Disable
1-0	Show Config Time	RW	00: 3 Seconds 01: 5 Seconds 10: 1 Seconds 11: 0 Seconds

Note: When the EEPROM-less feature is implemented, the RTL8103E(L)-GR cannot WOL from '1st AC power-on'.

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