

REALTEK

RTL8103T-GR

INTEGRATED FAST ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

EEPROM-Less APPLICATION NOTES

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware engineer’s reference and provides detailed application information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/12/22	First release.

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1. Introduction

This application note will help board designers to implement an EEPROM-less Realtek PCI-E RTL8103T-GR Fast Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single-chip PCI-E RTL8103T-GR Fast Ethernet controller. Those points have been listed below and are detailed in the following sections.

- LAN MAC Address Programming
- DID/VID Programming (if necessary)
- SDID/SVID Programming (if necessary)
- LED Mode Configuration
- PXE Driver

3. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8103T-GR. The BIOS must provide the MAC address to the RTL8103T-GR each boot time. The RTL8103T-GR will hold the MAC address until AC power off (pulling PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write the C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write the 33221100h to I/O register offset 0x00 via double word access

Step3: Write the 00005544h to I/O register offset 0x04 via double word access

Step4: Write the 00h to I/O register offset 0x50 via byte access to enable 'register protection'

4. DID/VID Programming (If Necessary)

The default DID/VID value of the RTL8103T-GR is 8136/10EC. If the board layer designer wants to change the value, please follow the steps below:

Example: Where VID=10ECh, DID=8136h:

Step1: Write 813610EC h to I/O register offset 0x64 via double word access

Step2: Write 8000F000h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

5. SID/SVID Programming (If Necessary)

The default SID/SVID value of the RTL8103T-GR is 8136/10EC. If the board layer designer wants to change the value, please follow the steps below:

Example: Where SVID=10ECh, SID=8136h

Step1: Write 813610ECh to I/O register offset 0x64 via double word access.

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

6. LED Mode Configuration

The RTL8103T-GR supports customer-defined LED operation modes. This section describe the various LED configuration options.

6.1. Link Monitor

The Link Monitor senses link integrity (LINK10, LINK100, LINK10/100, LINK10/ACT, LINK100/ACT). Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists. The customized LED enable register is located at I/O register 0x55 bit 6 (1'b indicates 'customized LED enabled'). The mode configuration register is located at I/O register 0x17~0x18.

Table 1. Customized LEDs

	LINK			ACT
Speed	Link 10M	Link100M	Not Defined	-
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 2	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

6.2. ACT LED

In 10/100Mbps mode, blinking of the ACT LED indicates that the RTL8103T-GR is operating properly.

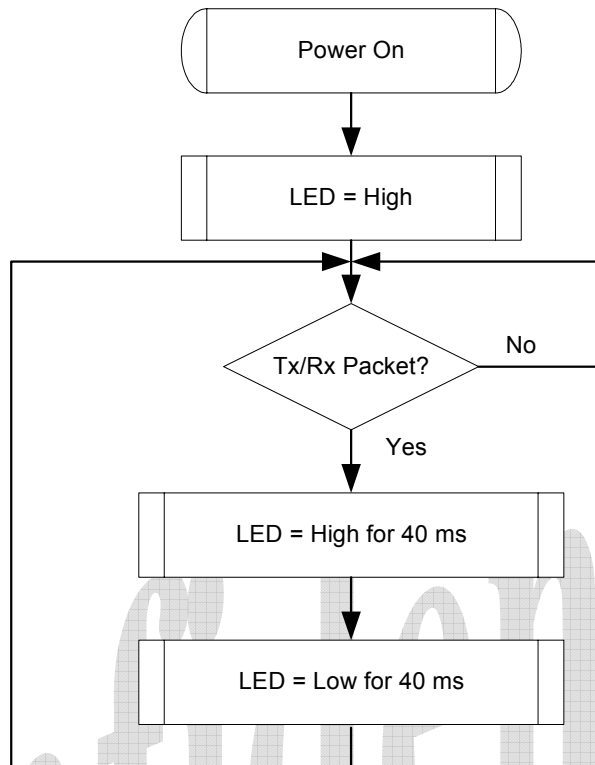


Figure 1. ACT LED

7. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below:

Table 2. PXE Parameters

Bit	Symbol	RW	Description
7-6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5-4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3	Show Config Message	RW	0: Enable 1: Disable
2	Shift+F10 Menu Entry	RW	0: Enable 1: Disable
1-0	Show Config Time	RW	00: 3 Seconds 01: 5 Seconds 10: 1 Seconds 11: 0 Seconds

Note: When the EEPROM-less feature is implemented, the RTL8103T-GR cannot WOL from '1st AC power-on'.

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