RTL8111B-GR
RTL8168B-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

EEPROM DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's register information on the Realtek RTL8111B and RTL8168B chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/11/14	First release.

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1. EEPROM (93C46/93C56) Contents

The RTL8111B/RTL8168B requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM, and the 93C56 is a 2K-bit EEPROM. The EEPROM interface provides the ability for the RTL8111B/RTL8168B to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following an internal power on reset, PCI reset, and software EEPROM autoload command. The RTL8111B/RTL8168B autoloads values from the EEPROM to these fields in configuration space and I/O space. If the EEPROM is not present, the RTL8111B/RTL8168B initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using 'bit-bang' accesses via the 9346CR Register, or using PCI VPD.

Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the initial power on reset, PCI reset, and software EEPROM autoload command in the 9346CR, the RTL8111B/RTL8168B performs a series of EEPROM read operations from the 93C46 (93C56) Address 00h to 3Fh.

We recommend you obtain Realtek approval before changing the default settings of the EEPROM.

Table 1. EEPROM (93C46/93C56) Contents

Bytes	Contents	Description
00h	29h	These 2 Bytes Contain ID Code Words for the RTL8111B/RTL8168B The RTL8111B/RTL8168B will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are '10ECh' and '8129h'.
01h	81h	
02h-03h	VID	PCI Vendor ID. PCI Configuration Space Offset 00h-01h
04h-05h	DID	PCI Device ID. PCI Configuration Space Offset 02h-03h
06h-07h	SVID	PCI Subsystem Vendor ID. PCI Configuration Space Offset 2Ch-2Dh
08h-09h	SMID	PCI Subsystem ID. PCI Configuration Space Offset 2Eh-2Fh
0Ah	BAR2	PCI BAR2[7:0] PCI Configuration Space Offset 18h. 04h for 64-bit MEM, 00h for 32-bit MEM
0Bh	BAR0	PCI BAR0[7:0] PCI Configuration Space Offset 10h. 01h for IO
0Ch	CONFIGx	Reserved
0Dh	CONFIG3	RTL8111B/RTL8168B Configuration Register 3 Operational register offset 54h
0Eh-13h	Ethernet ID	Ethernet ID After auto-load command or hardware reset, the RTL8111B/RTL8168B loads Ethernet ID to IDR0-IDR5 of the RTL8111B/RTL8168B's I/O registers.
14h	CONFIG0	RTL8111B/RTL8168B Configuration Register 0 Operational registers offset 51h
15h	CONFIG1	RTL8111B/RTL8168B Configuration Register 1 Operational registers offset 52h
16h-17h	PMC	Reserved. Do not change this field without Realtek approval Power Management Capabilities PCI configuration space addresses 42h and 43h

Bytes	Contents	Description
18h	Express Cap	[7:5]: Reserved [4]: Configuration space offset 62h bit[4] [3:0]: Offset 6D bit [3:0] of the RTL8111B/RTL8168B's I/O registers
19h	CONFIG4	Reserved. Do not change this field without Realtek approval RTL8111B/RTL8168B Configuration Register 4 Operational registers offset 55h
1Ah	Express Device Capability	PCIE Configuration Space Offset 64h
1Bh		PCIE Configuration Space Offset 65h
1Ch	Link Control / Status	PCIE Configuration Space Offset 70h
1Dh		PCIE Configuration Space Offset 73h
1Eh	PCIE Link Cap	[3:2]: PCIE Configuration Space Offset 6Dh bit[3:2]
1Fh	CONFIG_5	Realtek Internal Use. Do not change this field without Realtek approval
20h-27h	Serial Number	PCIE Configuration Space Offset 14Ch-153h
28h	PM Exit Control	PCIE Configuration Space Offset B4h
29h		PCIE Configuration Space Offset B5h
2Ah		PCIE Configuration Space Offset B6h
2Bh		PCIE Configuration Space Offset B7h
2Ch	Active PM Timer	PCIE Configuration Space Offset B8h
2Dh		PCIE Configuration Space Offset B9h
2Eh	EPHY2	Realtek Internal Use. Do not change this field without Realtek approval
2Fh	ROMBAR	PCI Configuration Space Offset 30h
30h	VSR P Credit	PCIE Configuration Space Offset 96h
31h	EPHY0	Realtek Internal Use. Do not change this field without Realtek approval
32h-33h	CheckSum	Reserved. Do not change this field without Realtek approval Checksum of the EEPROM content
34h	VSR P Credit	PCIE Configuration Space Offset 94h
35h		PCIE Configuration Space Offset 95h
36h	VSR NP Credit	PCIE Configuration Space Offset 99h
37h		PCIE Configuration Space Offset 9Ah
38h	VSR CPL Credit	PCIE Configuration Space Offset 9Ch
39h		PCIE Configuration Space Offset 9Dh
3Ah	VSR Link Timer	PCIE Configuration Space Offset B2h
3Bh		PCIE Configuration Space Offset B3h
3Ch	EPHY1	Realtek Internal Use. Do not change this field without Realtek approval
3Dh	VSR Link Timer	PCIE Configuration Space Offset B1h
3Eh		PCIE Configuration Space Offset B0h
3Fh	PXE_Para	Reserved. Do not change this field without Realtek approval PXE ROM code parameter
40h-7Fh	VPD_Data	VPD Data Field Offset 40h is the start address of the VPD data

2. EEPROM Related Ethernet MAC Registers

Table 2. EEPROM Related Ethernet MAC Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	RW*	-	-	-	-	-	-	-	-
51h	CONFIG0	R	-	-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	-	-
		W*	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	-	-
53h	CONFIG2	R	-	-	-	-	-	-	-	-
		W*	-	-	-	-	-	-	-	-
54h	CONFIG3	R	-	-	Magic	LinkUp	-	-	-	-
		W*	-	-	Magic	LinkUp	-	-	-	-
55h	CONFIG4	RW*	-	-	-	LWPME	-	LWPTN	-	-
56h	CONFIG5	RW*	-	-	-	-	-	-	-	-

Note: Registers marked with type = 'W' can be written only if bits EEM1=EEM0=1.*

2.1. CONFIG 0 (Offset 0051h, RW)

Note: Only the RTL8168B provides this function. The RTL8111B does not support SPI.

Table 3. CONFIG 0 (Offset 0051h, RW)

Bit	Symbol	RW	Description
7	Bootrom_pgact	RW	When set to 1, the SPI flash can be directly accessed via bit6~3, which will reflect the states of SPICSB, SPISK, SPIDI, and SPIDO pins respectively.
6	P_SPICS	RW	These bits reflect the state of the SPICSB, SPISK, SPIDI and SPIDO pins when bootrom_pgact is set to 1.
5	P_SPISCK	RW	
4	P_SPISI	RW	
3	P_SPISO	R	
2:0	BS2, BS1, BS0	R	Select Boot ROM Size

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	Reserved
1	1	1	Reserved

2.2. CONFIG 1 (Offset 0052h, RW)

Table 4. CONFIG 1 (Offset 0052h, RW)

Bit	Symbol	RW	Description
7:6	LEDS1-0	RW	Refer to the RTL8111B/8168B Datasheet for a Detailed LED Pin Description The initial value of these bits comes from the 93C46/93C56
5	-	-	Reserved
4	Speed_down	RW	Speed Down Enable 0: Link speed will stay at 1000Mbps when the isolateb pin is low 1: Link speed changes from 1000Mbps to 100Mbps when the isolateb pin is low
3	MEMMAP	R	Memory Mapping The operational registers are mapped into PCI memory space Always 1
2	IOMAP	R	I/O Mapping The operational registers are mapped into PCI I/O space Always 1
1	VPD	R	Vital Product Data: Set to enable Vital Product Data Always 1
0	PMEn	R	Power Management Enable Always 1

2.3. CONFIG 2 (Offset 0053h, RW)

Table 5. CONFIG 2 (Offset 0053h, RW)

Bit	Symbol	RW	Description
7-5	-	-	Reserved
4	Aux_Status	R	Auxiliary Power Present Status 1: Aux. Power is present 0: Aux. Power is absent The value of this bit is fixed after each PCI reset.
3-0	-	-	Reserved

2.4. CONFIG 3 (Offset 0054h, RW)

Table 6. CONFIG 3 (Offset 0054h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	VPDSel	RW	VPD Offset Select 1'b0 (default): VPD address start point = 40h 1'b1: VPD address start point = 00h
5	Magic	RW	Magic Packet This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8111B/RTL8168B will assert the PMEB signal to wakeup the operating system when a Magic Packet is received. Once the RTL8111B/RTL8168B has been enabled for Magic Packet wakeup, it scans all incoming packets addressed to the node for a specific data sequence that indicates to the controller that this is a Magic Packet. A Magic Packet must also meet the basic requirements of: Destination address + Source address + data + CRC. The destination address may be the node ID of the receiving station or a multicast address, which includes a broadcast address. The specific sequence consists of 16 duplications of a 6-byte ID register, with no breaks nor interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE MAC address match the address of the ID register. If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the Magic frame looks like the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4-0	-	-	Reserved

2.5. CONFIG 4 (Offset 0055h, RW)

Table 7. CONFIG 4 (Offset 0055h, RW)

Bit	Symbol	RW	Description
7-0	-	-	Reserved

2.6. CONFIG 5 (Offset 0056h, RW)

Table 8. CONFIG 5 (Offset 0056h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	BWF	RW	Broadcast Wakeup Frame 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF 0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF The power-on default value of this bit is 0
5	MWF	RW	Multicast Wakeup Frame 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address The power-on default value of this bit is 0
4	UWF	RW	Unicast Wakeup Frame 1: Enable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address The power-on default value of this bit is 0
3-0	-	-	Reserved

3. EEPROM Related Power Management Registers

Table 9. EEPROM Related Power Management Registers

Configuration Space Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

3.1. PCI Configuration Space Table

Table 10. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	IntDisable	0	SERREN
		W	-	-	-	-	-	IntDisable	-	SERREN
06h	Status	R	0	0	0	1	IntSt	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	0	0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	1
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	CLS7	CLS6	CLS5	CLS4	CLS3	CLS2	CLS1	CLS0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		RW	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		RW	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		RW	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h-17h	Reserved									
18h	MEM 64 BAR	R	MEM7	0	0	0	MEMPF	MEMLOC	MEMLOC	MEMIN
19h		RW	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
1Ah		RW	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
1Bh		RW	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
1Ch		RW	MEM39	MEM38	MEM37	MEM36	MEM35	MEM34	MEM33	MEM32
1Dh		RW	MEM47	MEM46	MEM45	MEM44	MEM43	MEM42	MEM41	MEM40
1Eh		RW	MEM55	MEM54	MEM53	MEM52	MEM51	MEM50	MEM49	MEM48
1Fh		RW	MEM63	MEM62	MEM61	MEM60	MEM59	MEM58	MEM57	MEM56

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h-27h	Reserved									
28h-2Bh	CISPtr	CardBus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		RW	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h-3Bh	Reserved									
3Ch	ILR	RW	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	0	1	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_$D3_{cold}$	PME_$D3_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
45h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
46h-47h	Reserved									
48h	VPDID	R	0	0	0	0	0	0	1	1
49h	NextPtr	R	0	1	0	1	0	0	0	0
4Ah	Flag VPD Address	RW	VPD ADDR7	VPD ADDR6	VPD ADDR5	VPD ADDR4	VPD ADDR3	VPD ADDR2	VPD ADDR1	VPD ADDR0
4Bh		RW	Flag	VPD ADDR14	VPD ADDR13	VPD ADDR12	VPD ADDR11	VPD ADDR10	VPD ADDR9	VPD ADDR8
4Ch	VPD Data	RW	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
4Dh		RW	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
4Eh		RW	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
4Fh		RW	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	Message Control	R	64-bit Address Capable	Multiple Message Enable			0	0	1	MSI Enable
		W	-	Multiple Message Enable			-	-	1	MSI Enable
53h		Reserved. Always return 0								
54h-57h	Message Address Low	RW	64-bit Interrupt Message Address Low							
58h-5Bh	Message Address High	RW	64-bit Interrupt Message Address High							
5Ch-5Dh	Message Data	RW	16-bit Message Data							
5E-5Fh	Reserved									
60h	PCIEID	R	0	0	0	1	0	0	0	0
61h	NextPtr	R	1	0	0	0	0	1	0	0
62h-63h	PCIE Cap.	R	0	0	0	Legacy	0	0	0	1
		R	0	0	0	0	0	0	0	0
64h-67h	Device Capability Register	R	L0s_acpt_ latency[1]	L0s_acpt_ latency[0]	Entend_ tag_ support	0	0	Max_payload_size_support		
		R	0	Pwr_ind_ present	Attn_ind_ present	Attn_ button_ present	L1s_acpt_ latency[2]	L1s_acpt_ latency[1]	L1s_acpt_ latency[0]	L0s_acpt_ latency[2]
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
68h-69h	Device Control Register	RW	Max_payload_size			Relaxed_ ordering_ en	Unsupport _rqst_rpt_ en	Fatal_err _rpt_en	Non_fatal _err_rpt_ en	Correct-able_err_ rpt_en
		RW	0	Max_read_request_size			No_snoop _en	Auxpwr _PM_en	0	Entend _tag_en
6Ah	Device Status Register	R	0	0	Transact _ion_ pending	AuxPwr _det	Upsupport _rqst_det	Fatal_err _det	Non_fatal _err_det	Correct-able_err_ det
		W	0	0	-	-	Upsupport _rqst_det	Fatal_err _det	Non_fatal _err_det	Correct-able_err_ det
6Bh		R	0	0	0	0	0	0	0	0
6Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
6Dh		R	L1_exit _lat[0]	L0s_exit _lat[2]	L0s_exit _lat[1]	L0s_exit _lat[0]	ASPM_support		0	0
6Eh		R	0	0	0	0	0	0	L1_exit _lat[2]	L1_exit _lat[1]0
6Fh		R	0	0	0	0	0	0	0	0
70h	Link Control Register	R	Extended _sync	Common _clock	0	0	0	0	ASPM_control	
		W	Extended _sync	Common _clock	0	0	0	0	ASPM_control	
71h		R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72h	Link Status Register	R	0	0	0	1	0	0	0	1
73h		R	0	0	0	Slot_clock_cfg	0	0	0	0
74h-83h	Reserved									
84h	SpecificID	R	0	0	0	0	1	0	0	1
85h	NextPtr	R	0	0	0	0	0	0	0	0
86h	Byte_Len	R	0	1	0	0	1	1	0	0
87h	Version	R	0	0	0	0	0	0	0	1
88h	Receive Capability	R	0	0	0	0	0	0	0	1
89h		R	0	0	0	1	1	1	0	0
8Ah	Receive Control	R	0	0	0	0	0	0	0	0
8Bh		R	0	0	0	0	0	0	0	0
8Ch-8Eh	Error Mask register	RW	RX_Error_mask							
8Fh	ROM BAR Mask	R	0	0	ROM_BAR_MASK					
90h	BAR MASK Register	R	0	0	0	0	1	0	0	0
91h		R	0	0	1	0	0	0	0	0
92h		R	1	0	0	0	0	0	0	0
93h		R	0	0	0	0	0	0	0	0
94h	Allocated Posted Credit	R	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
95h		R	PH[3]	PH[2]	PH[1]	PH[0]	PD[11]	PD[10]	PD[9]	PD[8]
96h		R	0	0	0	0	PH[7]	PH[6]	PH[5]	PH[4]
97h		R	0	0	0	0	0	0	0	0
98h	Allocated Nonposted Credit	R	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]
99h		R	NH[3]	NH[2]	NH[1]	NH[0]	ND[11]	ND[10]	ND[9]	ND[8]
9Ah		R	0	0	0	0	NH[7]	NH[6]	NH[5]	NH[4]
9Bh		R	0	0	0	0	0	0	0	0
9Ch	Allocated Completion Credit	R	CPLD[7]	CPLD[6]	CPLD[5]	CPLD[4]	CPLD[3]	CPLD[2]	CPLD[1]	CPLD[0]
9Dh		R	0	0	0	0	CPLD[11]	CPLD[10]	CPLD[9]	CPLD[8]
9Eh		R	0	0	0	0	0	0	0	0
9Fh		R	0	0	0	0	0	0	0	0
A0h-A1h	Transmit Capability	R	0	0	0	0	0	0	1	0
		R	0	0	1	0	1	0	0	0
A2h-A3h	Transmit Control	R	1	1	1	1	1	1	1	1
		R	0	0	0	0	0	0	0	1
A4h	Transmit First Error Report	R	Tag[7]	Tag[6]	Tag[5]	Tag[4]	Tag[3]	Tag[2]	Tag[1]	Tag[0]
A5h		R	0	0	Class[2]	Class[1]	Class[0]	Tag[10]	Tag[9]	Tag[8]
A6h		R	0	0	0	0	0	0	0	0
A7h		R	Txer_flag	Txer[4]	Txer[3]	Txer[2]	Txer[1]	Txer[0]	0	0
		W	Txer_flag	Txer[4]	Txer[3]	Txer[2]	Txer[1]	Txer[0]	0	0
A8h-A9h	Transmit Buffer Top	R	TX_buffer_address							
AAh-ABh	Reserved									
ACh	Aux Capability	R	0	0	0	0	0	0	1	1
ADh		R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AEh	Aux Control	R	0	0	0	0	0	0	1	1
AFh		R	0	0	0	0	0	0	0	0
B0h	Link Timer	RW	Replay[7]	Replay[6]	Replay[5]	Replay[4]	Replay[3]	Replay[2]	Replay[1]	Replay[0]
B1h		RW	Ack_Nack [5]	Ack_Nack [4]	Ack_Nack [3]	Ack_Nack [2]	Ack_Nack [1]	Ack_Nack [0]	Repaly[9]	Replay[8]
B2h		RW	Flow_ctrl [3]	Flow_ctrl [2]	Flow_ctrl [1]	Flow_ctrl [0]	Ack_ Nack[9]	Ack_ Nack[8]	Ack_ Nack[7]	Ack_ Nack[6]
B3h		RW	Receive_ flow_ctrl [1]	Receive_ flow_ctrl [0]	Flow_ctrl [9]	Flow_ctrl [8]	Flow_ctrl [7]	Flow_ctrl [6]	Flow_ctrl [5]	Flow_ctrl [4]
B4h	PM Exit Control	R	Common_N_FTS							
B5h		R	0	0	Common_L1_exit			Common_L0s_exit		
B6h		R	Non_common_N_FTS							
B7h		R	0	0	Non_common_L1_exit			Non_common_L0s_exit		
B8h	Active PM Timer	RW	L1_idle_time_required							
B9h		RW	L0s_idle_time_required							
BAh		RW	0	0	0	0	0	0	L1_scale	L0s_scale
BBh		R	Attn_ind_state		Power_ind_state		0	0	0	0
BCh-BFh	Aux Header Log	R	Aux Header Log 1							
C0h-C3h		R	Aux Header Log 2							
C4h-C7h		R	Aux Header Log 3							
C8h-CBh		R	Aux Header Log 4							
CCh	Aux Error Type/ Report	R	Error Type Indicator							
CDh-CFh		R	Reserved							
D0h-FFh	Reserved									

4. PXE Parameters

Table 11. PXE Parameters

Bit	Symbol	RW	Description
7:6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5:4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3	Show Config Message	RW	0: Enable 1: Disable
2	Shift+F10 Menu Entry	RW	0: Enable 1: Disable
1:0	Show Config Time	RW	00: 3 Seconds 01: 5 Seconds 10: 1 Seconds 11: 0 Seconds

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