RTL8111C-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

EEPROM-Less APPLICATION NOTES

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/03/07	First release.
1.1	2007/04/13	Revised section 2 Design Considerations, page 1. Revised section 8 Other Drivers, page 7.
1.2	2007/10/11	Remove section 4 DID/VID Programming Modify content of new section 4 SID/SVID Programming, page 2. Add section 6 Serial Number, page 6. Modify content of section 7 PXE Driver, page 6.

Table of Contents

1. INTRODUCTION 1

2. DESIGN CONSIDERATIONS 1

3. LAN MAC ADDRESS PROGRAMMING 1

4. SID/SVID PROGRAMMING (IF NECESSARY) 2

5. LED MODE CONFIGURATION 2

5.1. LINK MONITOR 2
5.2. RX LED 3
5.3. TX LED 3
5.4. LINK/ACT LED 4
5.5. TX/RX LED 5
5.6. LED MODE CONFIGURATION 5

6. SERIAL NUMBER 6

7. PXE DRIVER 6

8. OTHER DRIVERS 7

List of Tables

TABLE 1. LEDS 2
TABLE 2. PXE PARAMETERS 6

List of Figures

FIGURE 1. RX LED 3
FIGURE 2. TX LED 3
FIGURE 3. LINK/ACT LED 4
FIGURE 4. TX/RX LED 5

1. Introduction

This application note helps board designers to implement an EEPROM-less Realtek PCI-E RTL8111C-GR gigabit Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered while designing an EEPROM-less feature for Realtek's single chip PCI-E RTL8111C-GR gigabit Ethernet controller. Those points are listed below and are detailed in the following sections.

- LAN MAC Address Programming
- SDID/SVID Programming (If Necessary)
- LED Mode Configuration
- Serial Number
- PXE Driver
- Other Drivers

3. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8111C-GR. The BIOS must provide the MAC address to the RTL8111C-GR each boot time. The RTL8111C-GR will hold the MAC address until AC power off (pulling PCI reset low will not release the MAC address).

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'

4. SID/SVID Programming (If Necessary)

The default RTL8111C-GR SID/SVID value is 8168/10EC. If the board layer designer wants to change the value, please follow the steps below:

If SID=8168h, SVID=10ECh:

Step1: Write 816810ECh to I/O register offset 0x64 via double word access.

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Note: When the RTL8111C-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

5. LED Mode Configuration

The RTL8111C-GR supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

5.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists. The LEDS1-0 are I/O register 0x52 bit7:6.

Table 1. LEDs

Symbol	Type	Pin No	Description
LED0	O	57	
LED1	O	56	
LED2	O	55	
LED3	O	54	

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED1	LINK100	LINK10/100/ 1000	LINK	LINK100/ ACT
LED2	LINK10	LINK10/100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000/ ACT

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the 93C46.
If there is no 93C46, the default value of the (LEDS1, LEDS0) = (1, 1).

5.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

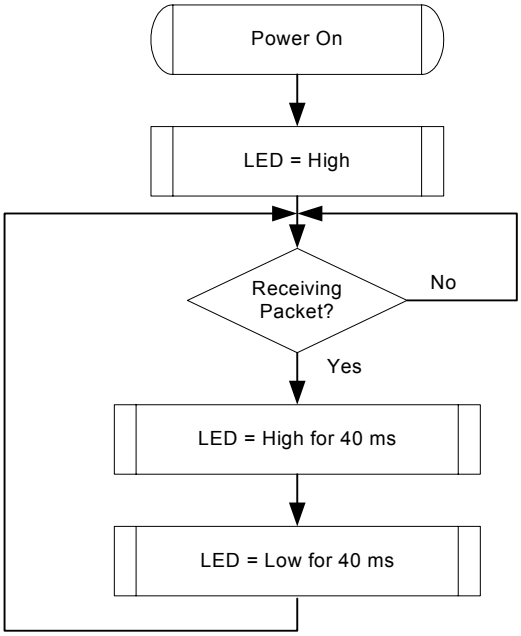

Figure 1. Rx LED

5.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

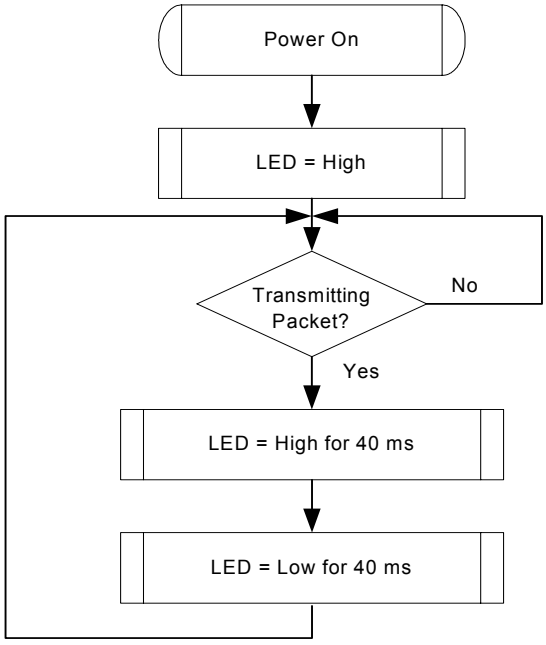

Figure 2. Tx LED

5.4. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111C-GR is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

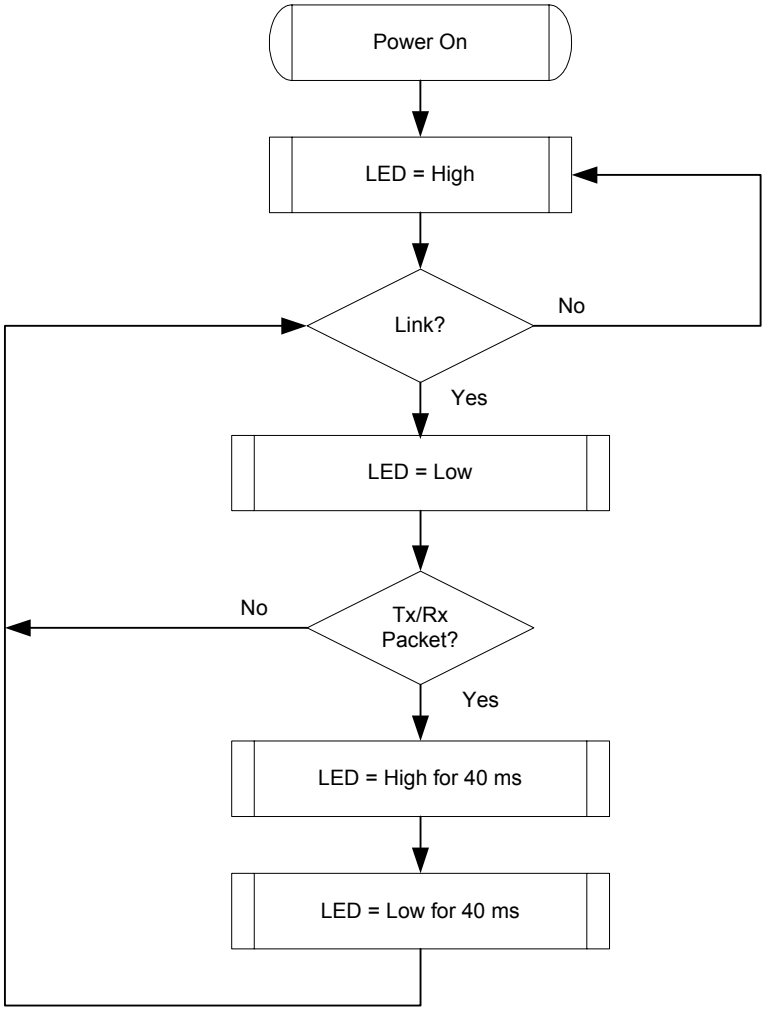

Figure 3. LINK/ACT LED

5.5. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

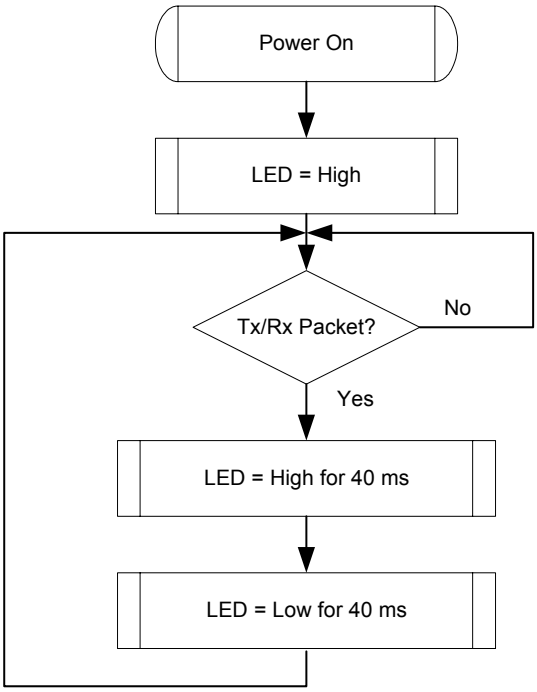

Figure 4. Tx/Rx LED

5.6. LED Mode Configuration

The default value of the RTL8111C-GR LEDS1-0 is 11b. If the board layer designer wishes to change the value, please follow the steps below:

Step1: Write C0h to I/O register offset 0x50 via byte access to disable 'register protection'.

Step2: Write xx001111b to I/O register offset 0x52 via byte access (bit7 is LEDS1 and bit6 is LEDS0; refer to the datasheet to find which mode you need).

Step3: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'.

6. Serial Number

Due to the EEPROM-less design goal, the serial number cannot be loaded from EEPROM and stored in the RTL8111C-GR. The BIOS must provide the serial number to the RTL8111C-GR each boot time.

If the serial number is 00E04C6812345678h:

Step1: Write 684CE000h to I/O register offset 0x64 via double word access.

Step2: Write 8000F164h to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Step4: Write 78563412h to I/O register offset 0x64 via double word access.

Step5: Write 8000F168h to I/O register offset 0x68 via double word access.

Step6: Wait for 1ms.

Note: When the RTL8111C-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

7. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below:

Table 2. PXE Parameters

Bit	Symbol	RW	Description
7:6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5:4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV(BBS)
3:0	-	-	Reserved

Note1: When the EEPROM-less feature is implemented, the RTL8111C-GR cannot WOL from '1st AC power-on'.
Note2: When the RTL8111C-GR resumes from S3, S4, or S5, the BIOS must complete the steps given above.

8. Other Drivers

Other drivers that support the RTL8111C-GR EEPROM-less feature are listed below:

- Windows Vista: V6.192 and later
- Windows XP: V5.668 and later
- Linux: V8.001.00 and later
- NDIS2: V1.15 and later
- PXE Driver: V2.06 and later
- Novell Server: V1.10 and later
- ODI Driver: V1.15 and later
- Packet Driver: V2.00 and later
- SCO Driver: V1.01 and later
- FreeBSD driver: V1.72 and later

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