RTL8111C-GR
RTL8111D-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

Rev. 1.5
02 September 2008
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

LICENSE

This product is covered by one or more of the following patents: US5,307,459, US5,434,872, US5,732,094, US6,570,884, US6,115,776, and US6,327,625.

USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the RTL8111C/D-GR Gigabit Ethernet controller.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/02/09	First release.
1.1	2007/07/04	Add section 7 Switching Regulator, page 16.
1.2	2008/03/14	Revised section 7.2 Inductor and Capacitor Parts List, page 17. Added section 7.5 Efficiency Measurement, page 23. Added section 7.6 Power Sequence, page 24. Revised section 8.6 Power Inductor, page 26.
1.3	2008/05/06	Revised section 7.4 Typical Switching Regulator PCB Layout, page 22.
1.4	2008/08/13	Updated licensing information.
1.5	2008/09/02	Expanded power and ground plane layout sections.

Table of Contents

List of Figures

1. Introduction

The Realtek RTL8111C/D-GR Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111C/D-GR offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.1 bus interface for host communications with power management and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™, Re-LinkOk, and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111C/D -GR.

The RTL8111C/D-GR is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The device also features next-generation interconnect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111C/D-GR is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8111C/D-GR. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8111C/D-GR.

(3) Simplify the task of routing signal traces.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8111C/D-GR, good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV)
- Verify that critical components such as the clock source and transformer meet application requirements
- Keep power and ground noise levels below 50mV
- Use bulk capacitors (10µF-22µF) between the power and ground planes
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep de-coupling capacitors as close as possible to the RTL8111C/D-GR
- Provide termination on all high-speed switching signals
- Route the signal trace as short as possible
- Use a smaller package for the capacitor to reduce the package inductance

Use the following signal integrity techniques to reduce crosstalk.

- Shorter parallel routes
- Wider ground plane spacing between GMII signal wires
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane

2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location
- Avoid vias and layer changes if possible
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane if possible
- 0.1µF common mode noise filter capacitors should be placed near the RTL8111C/D-GR chip
- Ninety-degree trace angles should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts

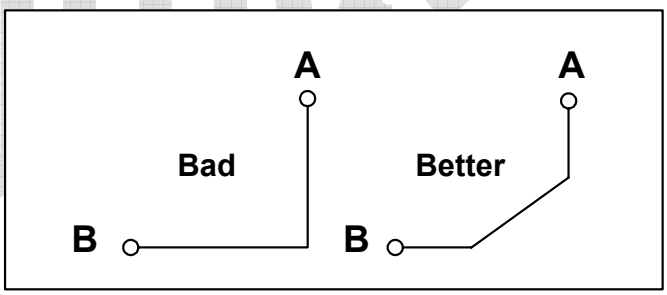

Figure 1. Signal Trace Angles

2.3. Placing the RTL8111C/D-GR

- The RTL8111C/D-GR should be placed as close as possible to the magnetics.

2.4. Magnetics

- The 10/100/1000M magnetics should be placed as close as possible to the RJ-45 connector.
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other

2.5. Crystal

- The Crystal should be placed away from I/O ports, important or high frequency signal traces (Tx, Rx, power), magnetics, and board edges.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI.
- The retaining straps of the OSC, if any, need good grounding.

2.6. Termination Resistors and Capacitors

The RTL8111C/D-GR does not require any termination resistors. The V_DAC voltage of the transformer should be left floating. Figure 2 shows the layout of the RTL8111C/D-GR.

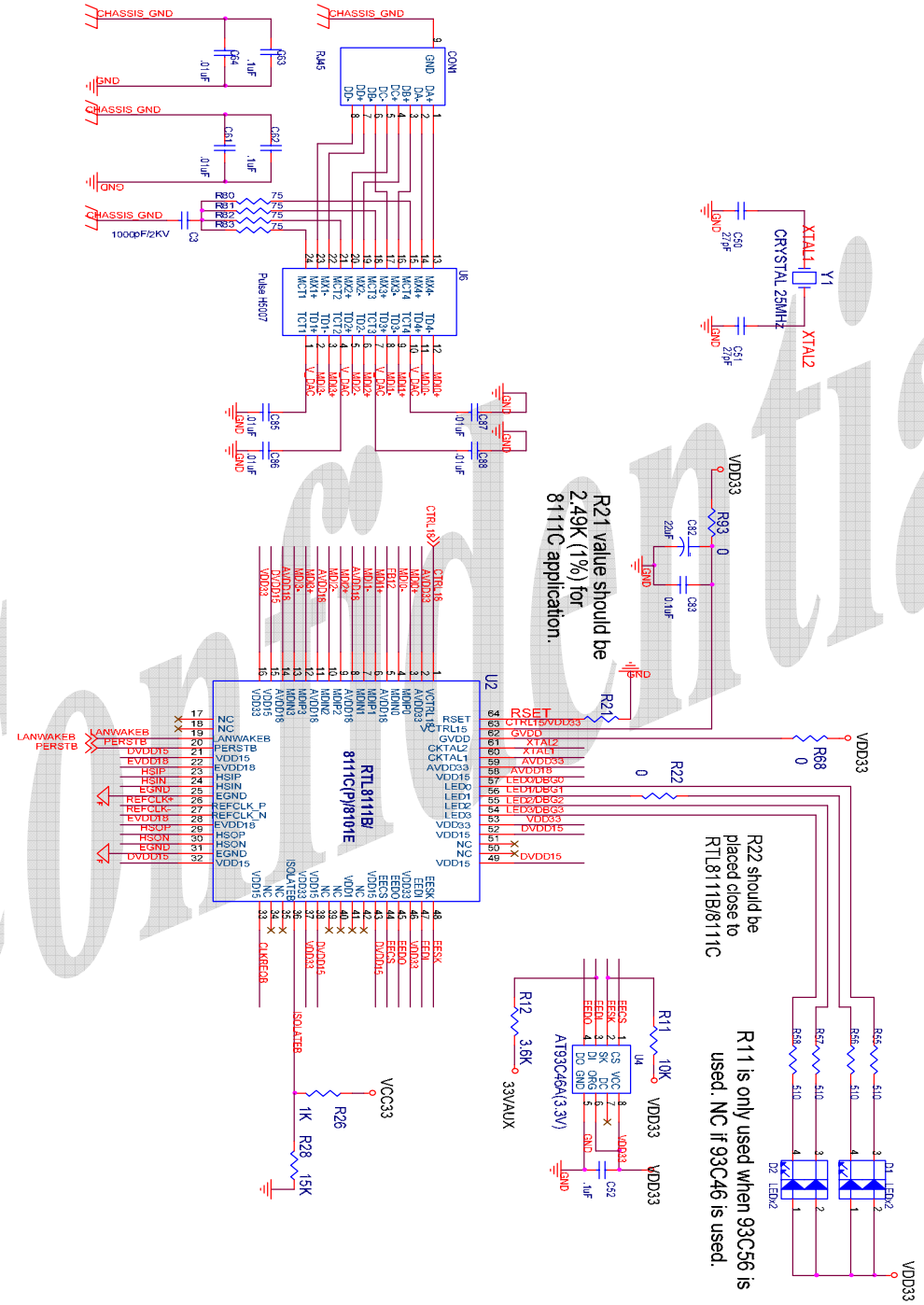

Figure 2. Layout

2.7. Ferrite Beads and De-Coupling Capacitors

Each PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors (Z5U, Y5V types are recommended) should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

3. Signal and Trace Routing

Noise, ringing, and data lines should be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Traces routed from the RTL8111C/D-GR to the 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8111C/D-GR and magnetics is achievable only when there is no interference. It is also very important to keep all four differential pair signal traces (MDI0+/-, MDI1+/-, MDI2+/-, MDI3+/-) equal in length. The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong canceling effect on noise. The width of D1 should be calculated to have 100Ω impedance (Figure 3).

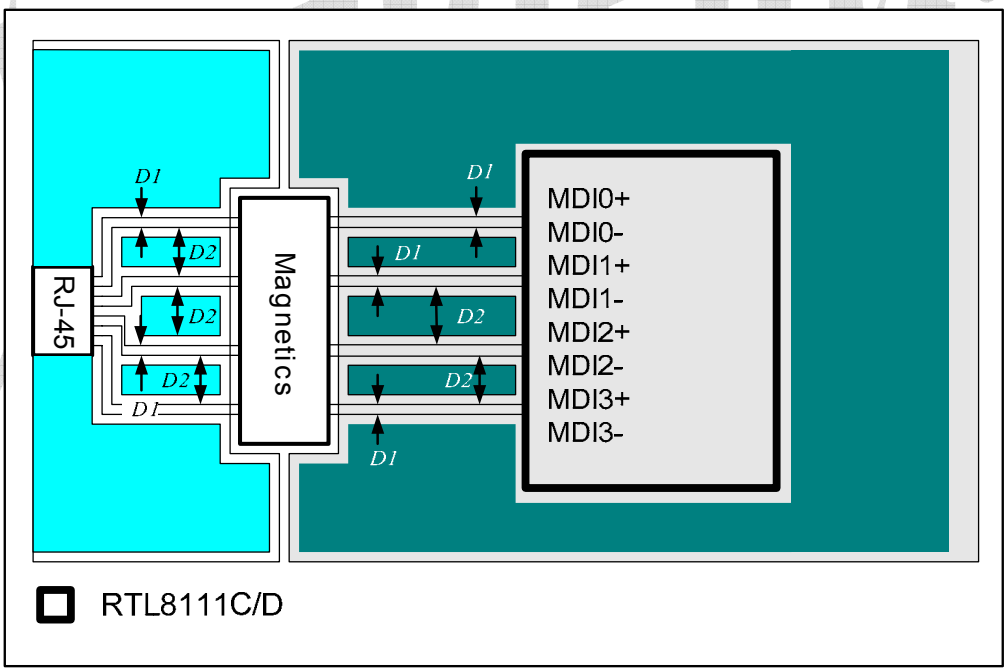

Figure 3. Signal & Trace Routing

- We suggest that there should be more than 50 mil spacing between different differential pairs to minimize cross-talk coupled from other pairs (D2 in Figure 3). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, we recommend not to use vias on the four differential pairs
- Avoid right angle signal traces. Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1 , page 3. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.
- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them.
- It is important to separate Digital Signals (e.g., BROM, Flash, EESK) from Analog Signals (e.g., MDI0+/-, MDI1+/-, MDI2+/-, and MDI3+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles.
- The power into the RTL8111C/D-GR digital power pins can be improved with de-coupling capacitors. The Power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8111C/D-GR need to be de-coupled with a capacitor. The de-coupling capacitors should be placed as close to the IC as possible and the traces should be kept short.
- The PCI-Express signal differential pairs should be 5mils wide, with a spacing of 7mils between them (REFCLK+ & REFCLK-, HSOP & HSON, HSIP & HSIN). The length difference of the signals in a pair should not exceed 5 mils. For example, if HSON is 900 mils and HSOP is 890mils, it may result in data transmit error.

4. Ground Plane Layout

There is only one ground plane for analog power (AVDDH & AVDDL), digital power (VDD33, DVDD15) and PCI-Express power (EVDD18). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 5.6mm x 5.6mm. The PCB layout requires 9 vias to connect the EPAD to the lower layer ground plane (see Figure 4).

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

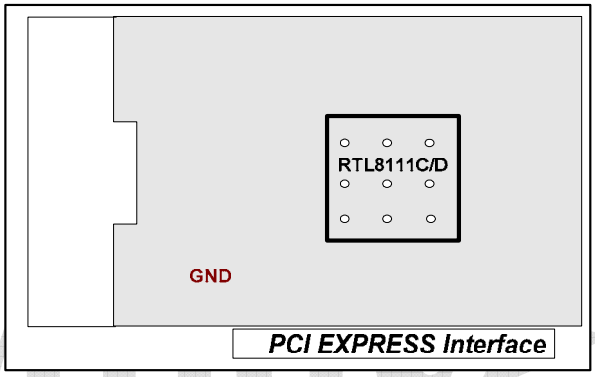

Figure 4. Ground Plane Layout-1

To achieve better ground plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 5 illustrates a not so good (left) and a good ground plane layout (right).

Figure 5. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer induced noise away from the power and system ground planes (Figure 6).

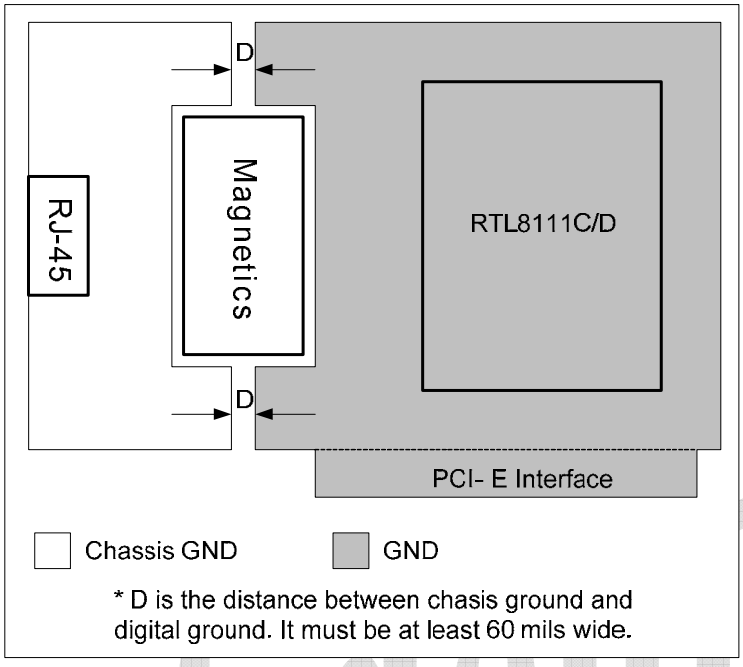

Figure 6. Ground Plane Separation

The Chassis Ground as shown in Figure 6 is known as an "Isolated Ground". It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is also important to keep the gap (D in Figure 6) between Chassis GND and System GND wider than 60 mils for better isolation.

4.1. Four-Layer Board Ground Plane Layout (Typical Application)

1. Signal 1 (top layer)

2. Power (Keep GND area for RTL8111C)

3. GND

4. Signal 2 (bottom)

4.1.1. Ground Plane Layer 1 Layout

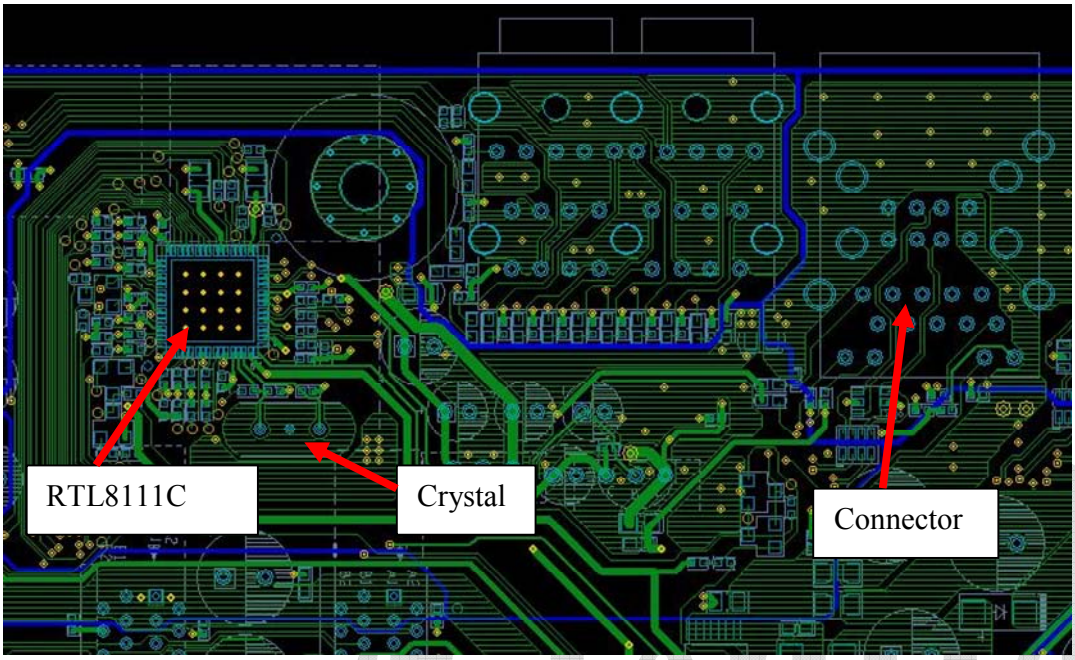

Figure 7. Ground Plane Layer 1 Layout

4.1.2. Ground Plane Layer 2 Layout

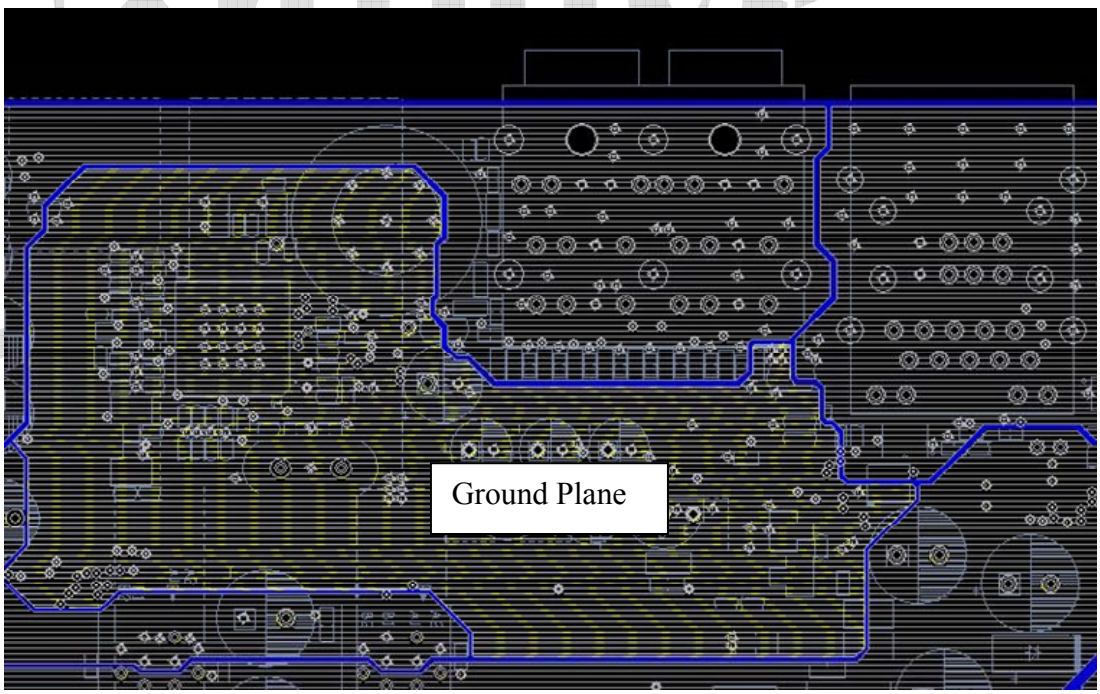

Figure 8. Ground Plane Layer 2 Layout

4.1.3. Ground Plane Layer 3 Layout

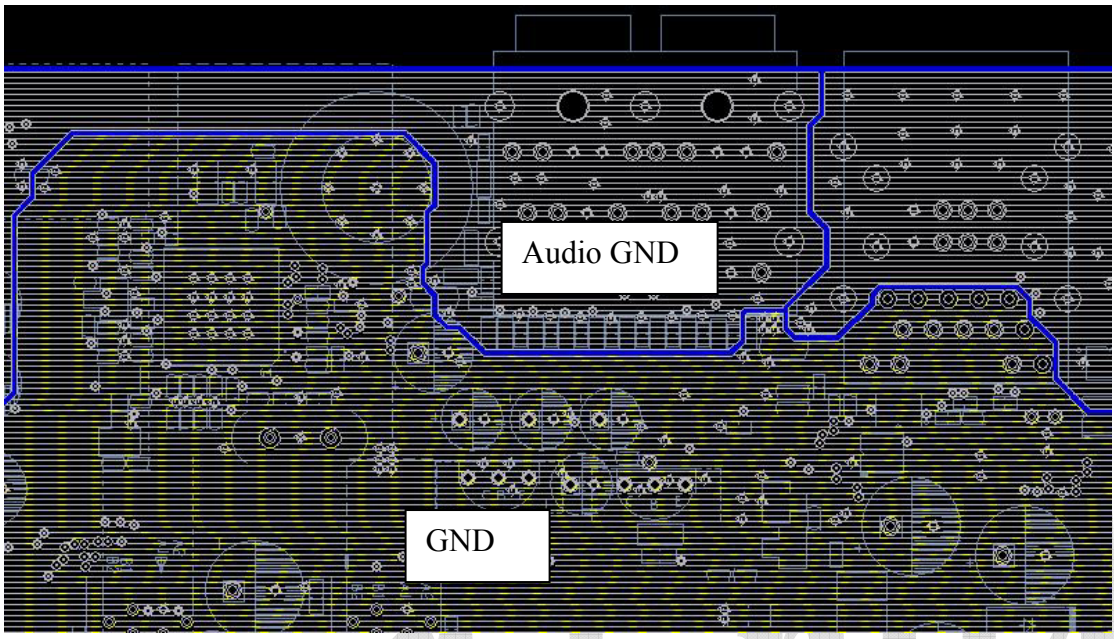

Figure 9. Ground Plane Layer 3 Layout

4.1.4. Ground Plane Layer 4 Layout

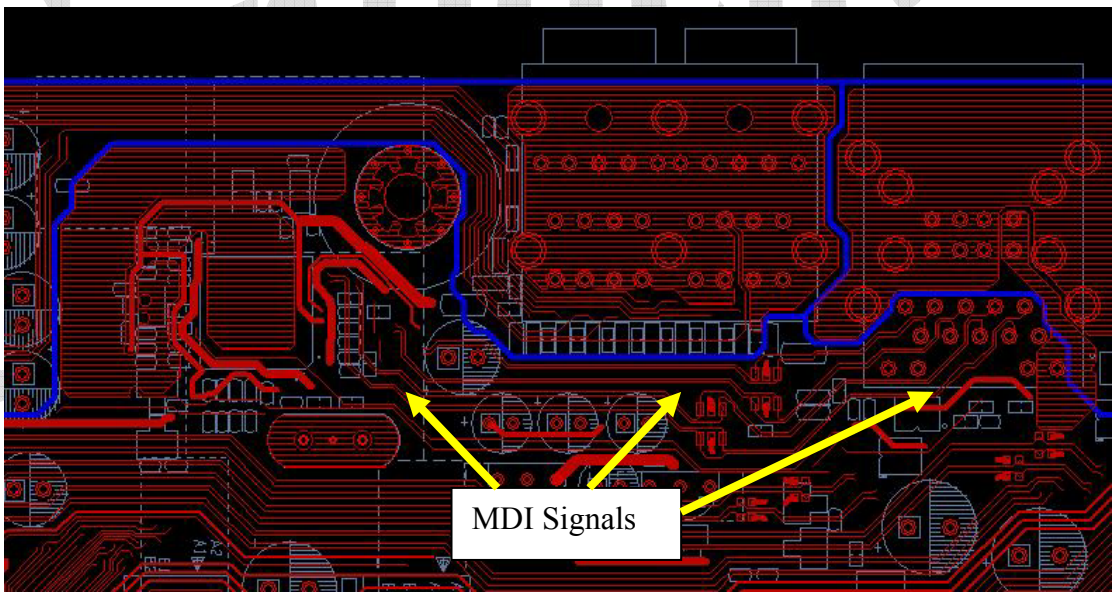

Figure 10. Ground Plane Layer 4 Layout

5. Power Plane Layout

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. It is recommended to use at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8111C/D-GR. If it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

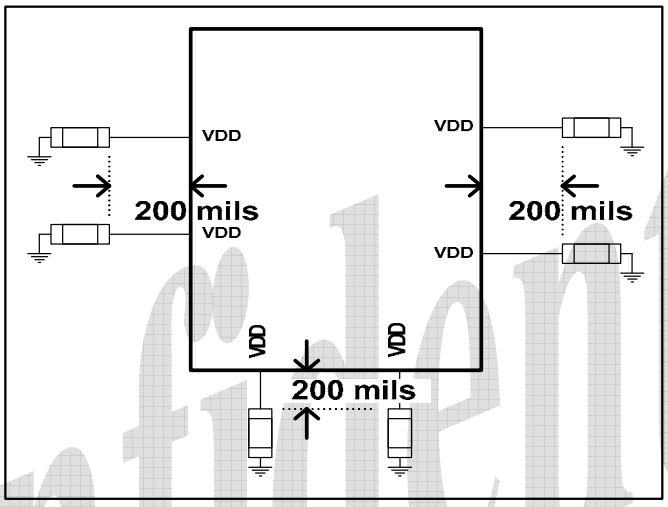

Figure 11. Decoupled Capacitor Example

(b) Use a Ferrite Bead to connect Digital and Analog Power

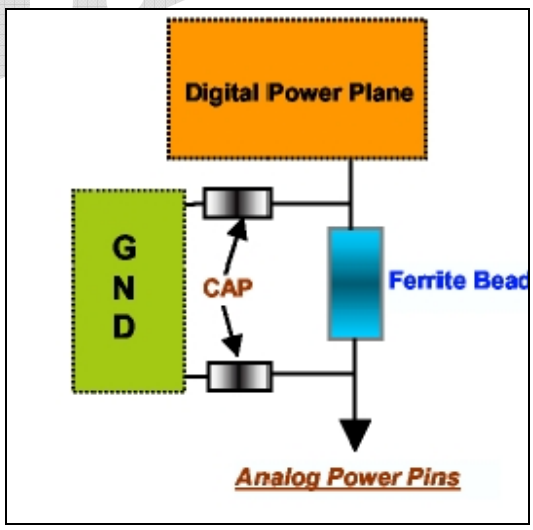

Figure 12. Ferrite Bead

To further improve the performance of the power plane, try to keep the contact area between the RTL8111C/D-GR VDD pins and power plane as large as possible rather than using small narrow traces (Figure 13).

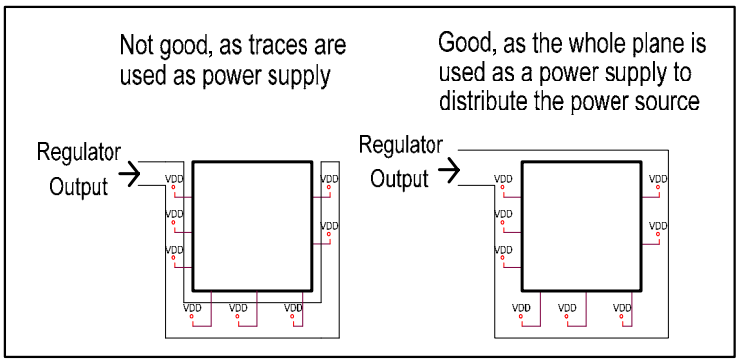

Figure 13. Power Source Distribution

- Keep power noise levels below 100mV in gigabit mode.
- All 3.3V/1.2V decoupling capacitors shown in the reference schematic should be used in all designs.
- Keep the analog power (1.2V) plane as whole and as large as possible.

5.1. Power Plane Layer 1 Layout

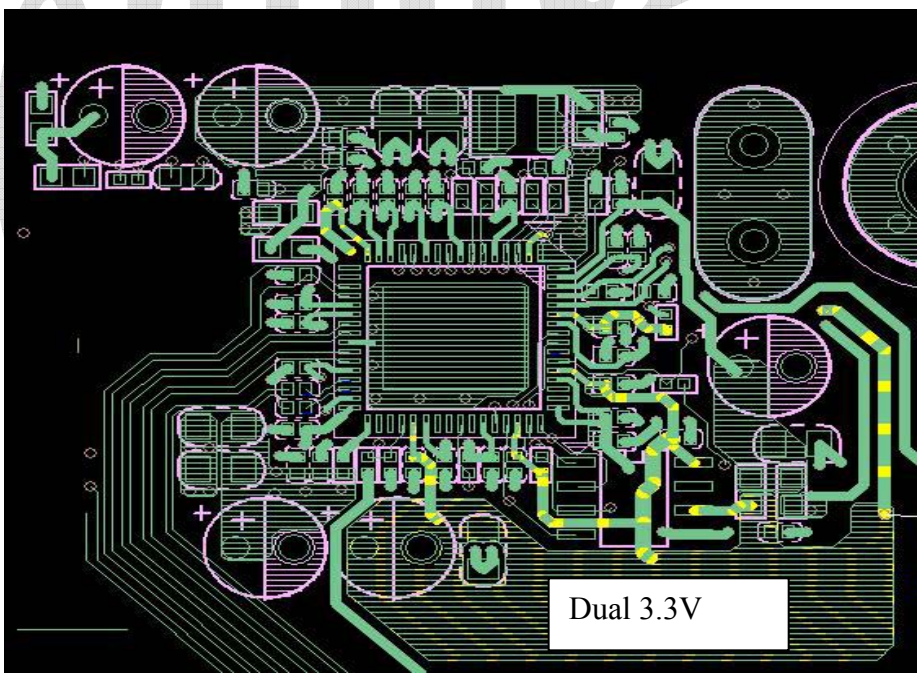

Figure 14. Power Plane Layer 1 Layout

5.2. Power Plane Layer 4 Layout

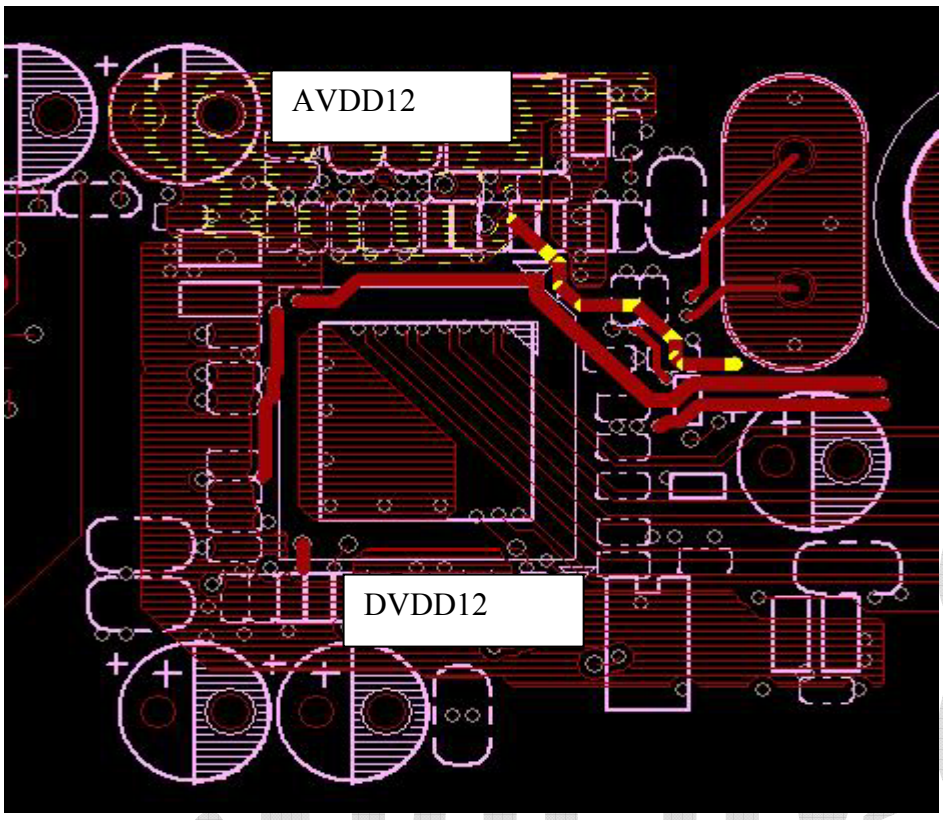

Figure 15. Power Plane Layer 4 Layout

6. Center-Tapping

- A center-tapped fine-tuned capacitor (C1 Value: 0.1µF~10pF) can improve EMI for single tone noise. The capacitor default is NC.
- Changing the R1 resistor to a capacitor (Value: 0.1µF~10pF), and fine-tuning the connection to GND can improve EMI for single tone noise. The resistor default is 0 ohm.

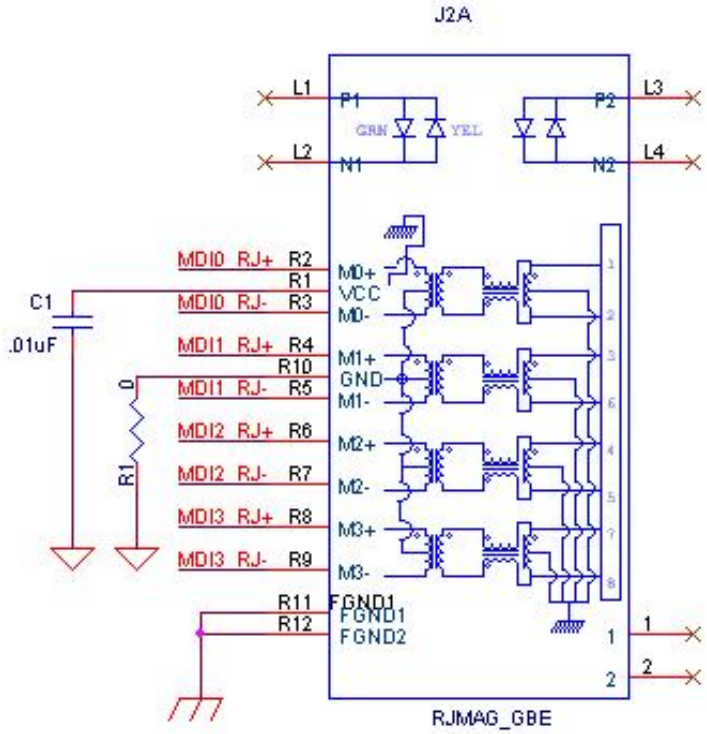

Figure 16. Center-Tapping

7. Switching Regulator

The RTL8111C/D-GR incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot.

7.1. PCB Layout

- The input 3.3V power trace connected to pin 63 (VDDSR) should be wider than 40 mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200 mils (0.5cm) of pin 63 to prevent input voltage overshoot.
- The output power trace out of pin 1 (SROUT12) should be wider than 60 mils.
- Keep L20 within 200 mils (0.5cm) of pin1.
- Keep C18 and C19 within 200 mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.

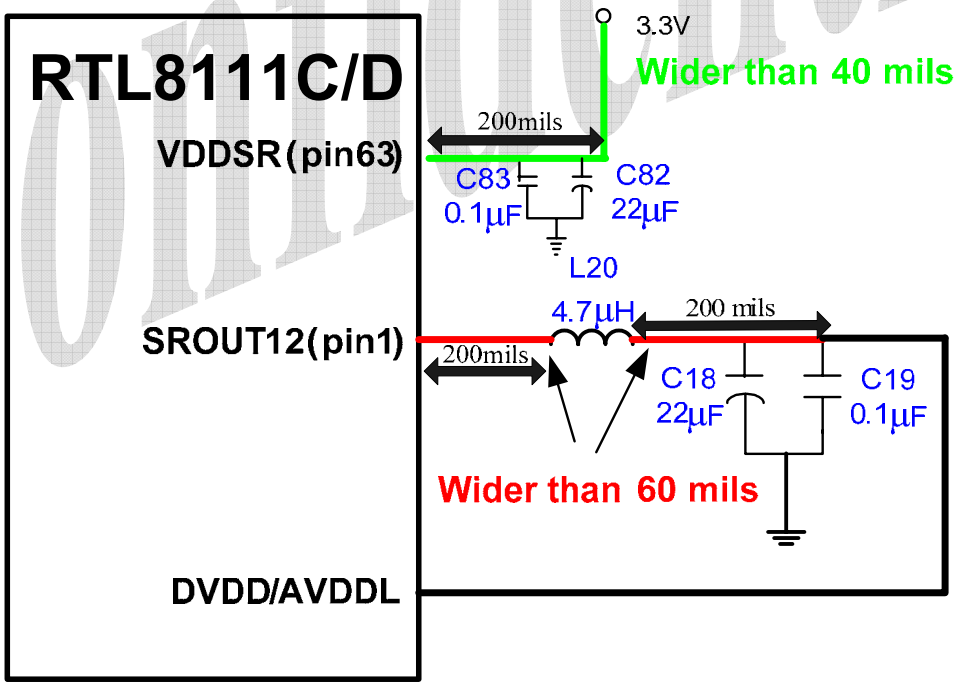

Figure 17. Switching Regulator Illustration

7.2. Inductor and Capacitor Parts List

Table 1. Inductor and Capacitor Parts List

Inductor Type	Inductance	ESR at 1MHz (mΩ)	Max IDC (mA)	Output Ripple (mV)
4R7GTSD32	4.7µH	712	1100	12.6
6R8GTSD32	6.8µH	784	900	12
6R8GTSD53	6.8µH	737	1510	10.4

Note 1: The ESR is equivalent to RDC or DCR.. Lower ESR inductor values will promote a higher efficiency switching regulator.

Note 2: The power inductor used by the switching regulator should be able to withstand 600mA of current.

Note 3: Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 7.5 Efficiency Measurement, page 23.

Capacitor Type	Capacitance	ESR at 1MHz (mΩ)	Output Ripple (mV)
22µF 1210 TDK	21.5µF	33.53	9.6
22µF 1210 X5R	22.15µF	34.11	10.4

Note: Capacitors (C18 & C82) are suggested to be ceramic due to their low ESR value. Lower ESR values will yield lower output voltage ripple.

7.3. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at Pin 63, not at the capacitor. In order to reduce the input voltage overshoot, C82 and C83 must be placed close to Pin 63. The following figures show what a good input voltage and a bad one look like.

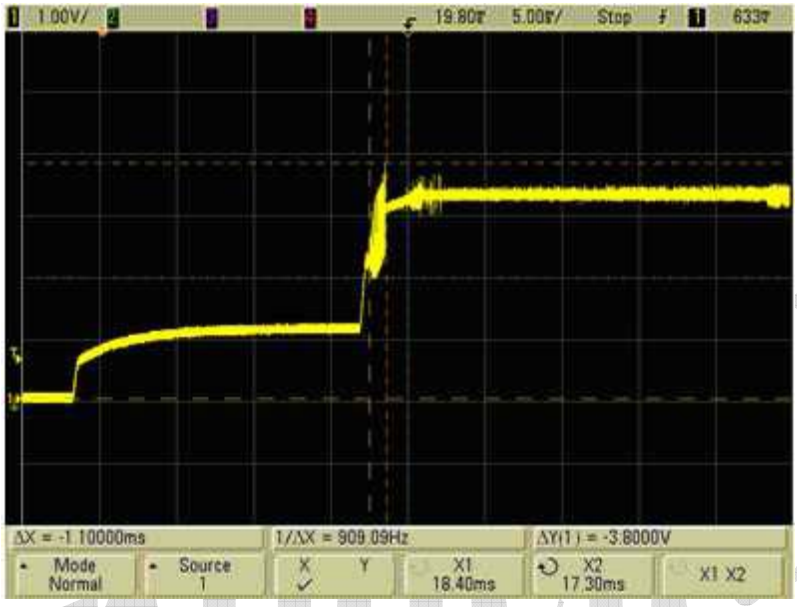

Figure 18. Input Voltage Overshoot <4V (Good)

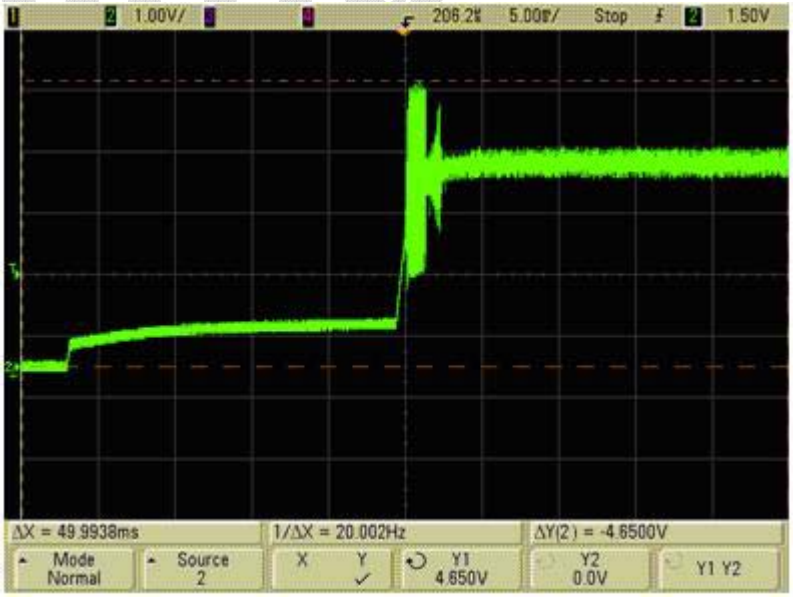

Figure 19. Input Voltage Overshoot >4V (Bad)

From the output side measured at Pin 1, the voltage ripple must be within 100mV. Choosing different types and values of output capacitor (C18, C19) and power inductor (L1) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of SROUT12 (Pin1) before the power inductor (L1). The yellow signal (second row) is measured after the power inductor (L1), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at gigabit speed.

Figure 20. Ceramic 22µF 1210(X5R) (Good)

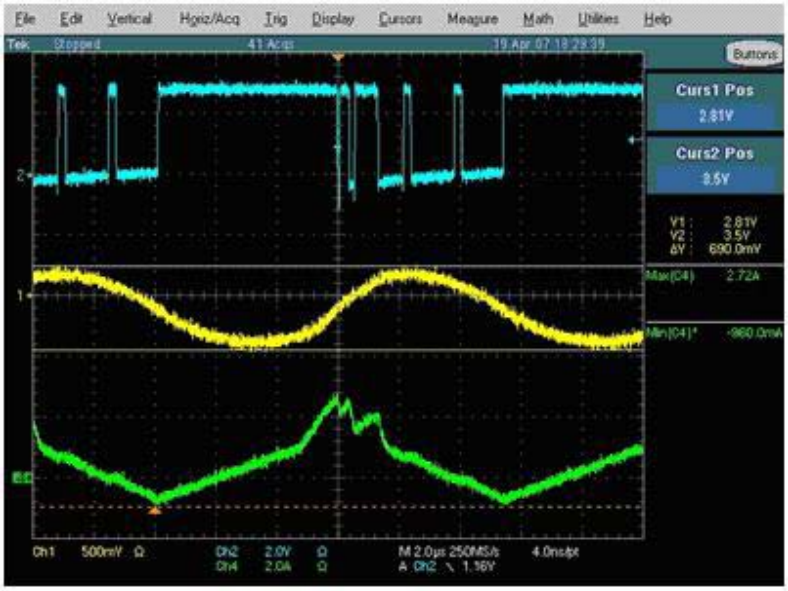

Figure 21. Ceramic 22µF 0805(Y5V) (Bad)

A ceramic 22µF (X5R) will have a lower voltage ripple compared to an electrolytic 100µF. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 22µF 0805 (Y5V) in this case will cause malfunction of the switching regulator. Placing several Electrolytic capacitors in parallel will help lower the output voltage ripple.

Figure 22. Electrolytic 100µF (Ripple Too High)

The following figures show how different inductors affect the PIN 1 output waveform. The typical waveform should look like Figure 23, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 24, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed.

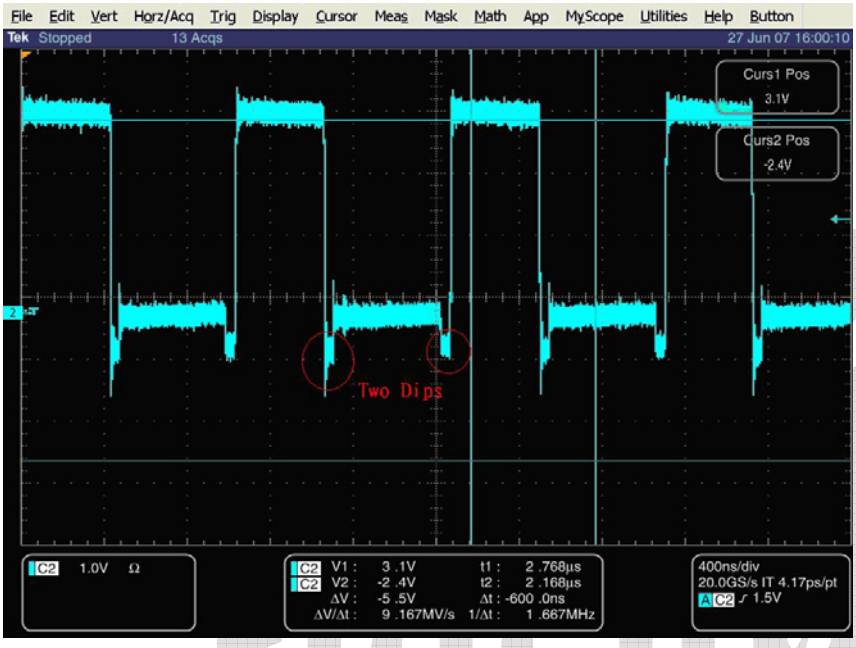

Figure 23. 4R7GTSD32 (Good)

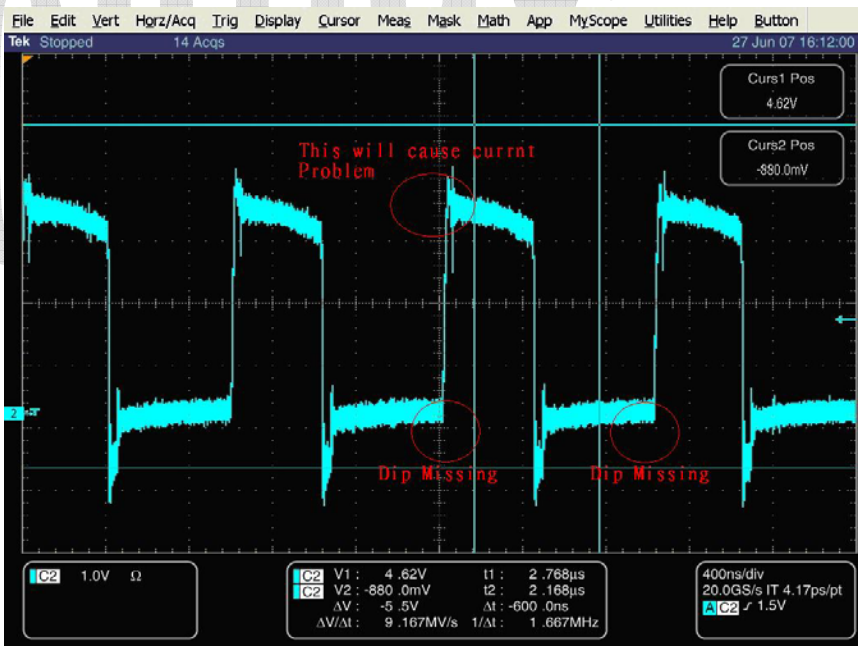

Figure 24. 1µH Bead (Bad)

7.4. Typical Switching Regulator PCB Layout

The typical layout of Figure 25 and Figure 26 are similar. The trace from Pin 64 should pass through a via to the lower layer, and the trace should be protected by a ground trace. The width of the ground trace should be more than 5 mils.

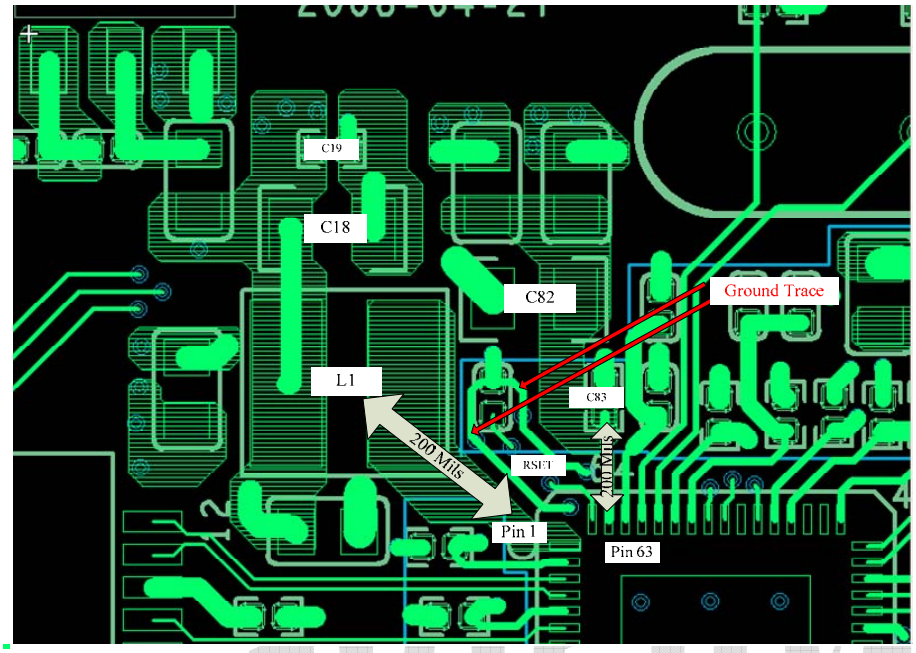

Figure 25. Typical Switching Regulator PCB Layout (Top Layer)

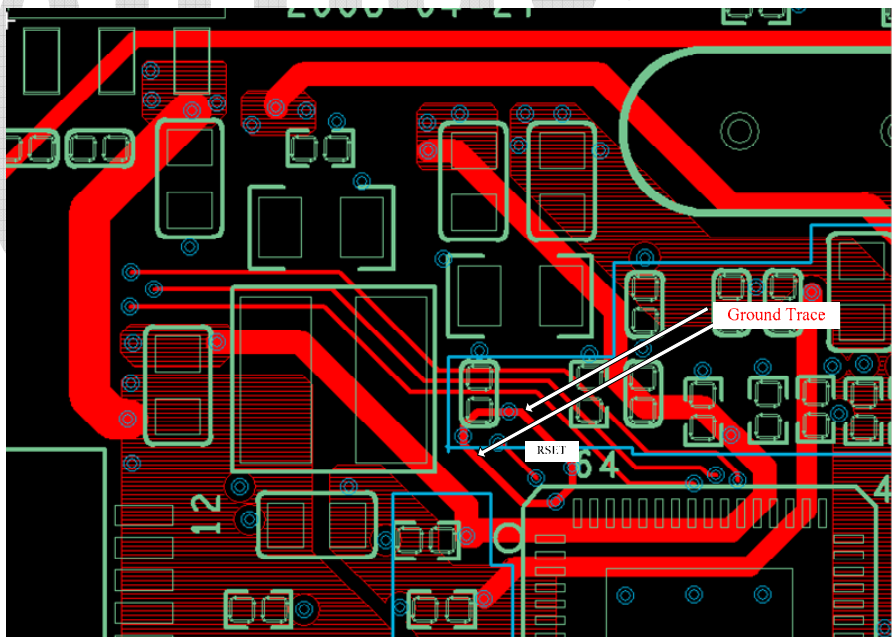

Figure 26. Typical Switching Regulator PCB Layout (Bottom Layer)

7.5. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 27, page 24, shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

Efficiency = Vcpb*Icpb / Vcpa*Icpa

Where Vcpb is 1.2V; Vcpa is 3.3V. The measurements should be performed in gigabit traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

- The ESR value @ 1MHz is approximately 0.712ohm
- The measured Icpa is 160mA at CP_A
- The measured Icpb is 352mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

Efficiency = (1.2V*352mA) / (3.3V*160mA) = 0.8 = 80%.

We strongly recommend that when choosing an inductor for the switching regulator, the efficiency should be measured, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability in the long run.

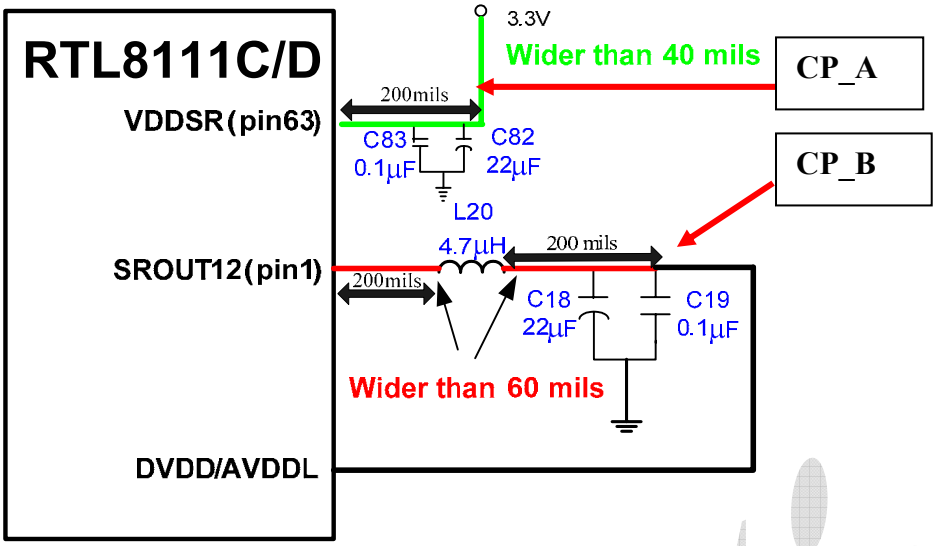

Figure 27. Switching Regulator Efficiency Measurement Checkpoint

7.6. Power Sequence

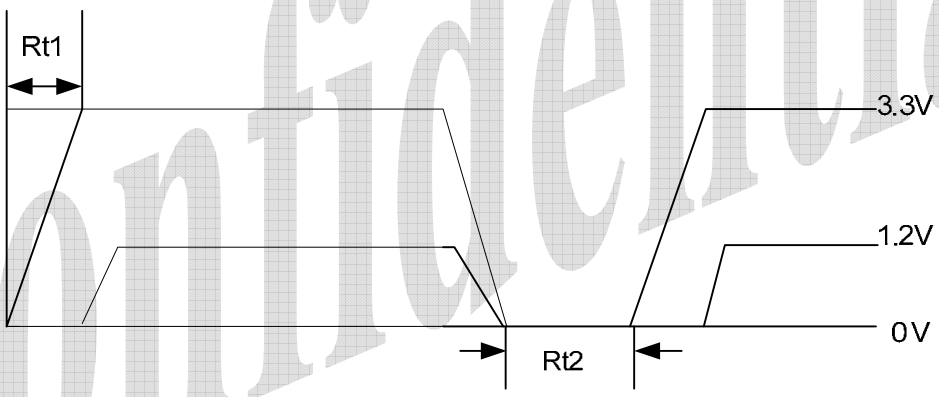

Figure 28. Power Sequence

Table 2. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	1	-	100	ms
Rt2	3.3V Fall Time	200	-	-	ms

Note 1: The RTL8111x does not support fast 3.3V rising. The 3.3V rise time must be controlled over 1ms. If the rise time is too short it will induce a peak voltage in PIN63, which may cause permanent damage to the switching regulator.

Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.2V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 200ms.

8. Parts Recommendations

8.1. 10/100/1000M Magnetic

Turn Ratio Tx/Rx: 1:1

Primary Inductance: 350µH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Pulse H5007 or similar

8.2. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to XTAL1 (Pin121) and XTAL2 (Pin122). Shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz
Temperature Stability	±10ppm
Duty Cycle	50%±10%
Tolerance	±50ppm
ESR	Max 30Ω
Aging	5ppm/year, max.

8.3. Resistors

Resistors that have tolerance requirements within 1%, are strongly recommended. Refer to the provided BOM for suggested schematics.

8.4. Capacitors

- Use X7R capacitors for small value and high frequency de-coupling. Use Y5V capacitors for critical temperature requirements
- For switching regulator power filtering, X5R Ceramic capacitors are recommended for the power circuit. Use X7R dielectric capacitors of several µF to reduce power ripple significantly. See section 7.2 Inductor and Capacitor Parts List, page 17, for the recommended parts list.

8.5. Ferrite Bead

The ferrite bead used should be of at least 100Ω@100MHz impedance with a rated current of 300mA or over.

8.6. Power Inductor

The power inductor used by the switching regulator should be able to withstand 600mA of current, and the resistance value should be as small as possible to achieve the expected switching regulator efficiency which must be higher than 75%.

Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 7.5 Efficiency Measurement, page 23.

8.7. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

9. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for Gigabit Ethernet applications.

- If it is found that there is a serious EMI issue, some de-coupling capacitors (0.047µF, 22µF) can be added between the system GND and power planes
- When using the oscillator as the clock source for 25MHz, avoid connecting any capacitors to the clock circuitry
- To achieve proper skew rate requirements, the digital bus traces for BOOTROM and EEPROM should have lengths as equal as possible
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com