RTL8111DP-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/11/25	First release.
1.1	2008/12/15	Revised section 6.10 DASH, page 23. Changed Table 19 Crystal Requirements, page 27. Changed Table 20 Oscillator Requirements, page 28.

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1. General Description

The Realtek RTL8111DP-GR Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111DP offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111DP is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™ and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111DP.

The RTL8111DP is fully compliant with Microsoft® NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8111DP supports four Receive Side Scaling (RSS) queues to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions/connections per second, for increased network throughput.

Alert Specification Format (ASF 2.0) is also supported to provide system manageability in OS-absent environments. The ASF defines remote control and alerting interfaces that serve managed PCs in OS-absent states. With the ASF capability, we are able to minimize on-site I/T maintenance, to improve system availability, and also to control power management remotely.

The Desktop and mobile Architecture for System Hardware (DASH) Initiative is a suite of specifications that takes full advantage of the DMTF's Web Services for Management (WS-Management) specification – delivering standards-based Web services management for desktop and mobile client systems. Through the DASH Initiative, the RTL8111DP provides the next generation of standards for secure out-of-band and remote management of desktop and mobile systems.

The RTL8111DP supports Internet Protocol security (IPSEC). The IPSec protocol suite is based on powerful encryption technologies, and adds security services to the IP layer that are compatible with both IPv4 and IPv6. With IPSec, users can create a secure VPN on demand.

The RTL8111DP also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. The device embeds an adaptive equalizer in the PCI-E PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 40 inches.

The RTL8111DP is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-On-LAN and remote wake-up support
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IP Security Offload
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Embedded OTP memory can replace an external EEPROM
- Serial EEPROM
- Transmit/Receive on-chip buffer support
- Supports power down/link down power saving
- Built-in switching regulator
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports Alert Specification Format 2.0 (ASF2.0)
- Supports Desktop and mobile Architecture for System Hardware (DASH)
- Supports Receive-Side Scaling (RSS)
- 64-pin QFN package (Green package)
- Embeds an adaptive equalizer in PCI Express PHY (PCB traces can reach up to 40 inches)
- Supports Four Customizable LEDs

3. System Applications

- PCI Express Gigabit Ethernet on Motherboard, Notebook, or Embedded system

4. Pin Assignments

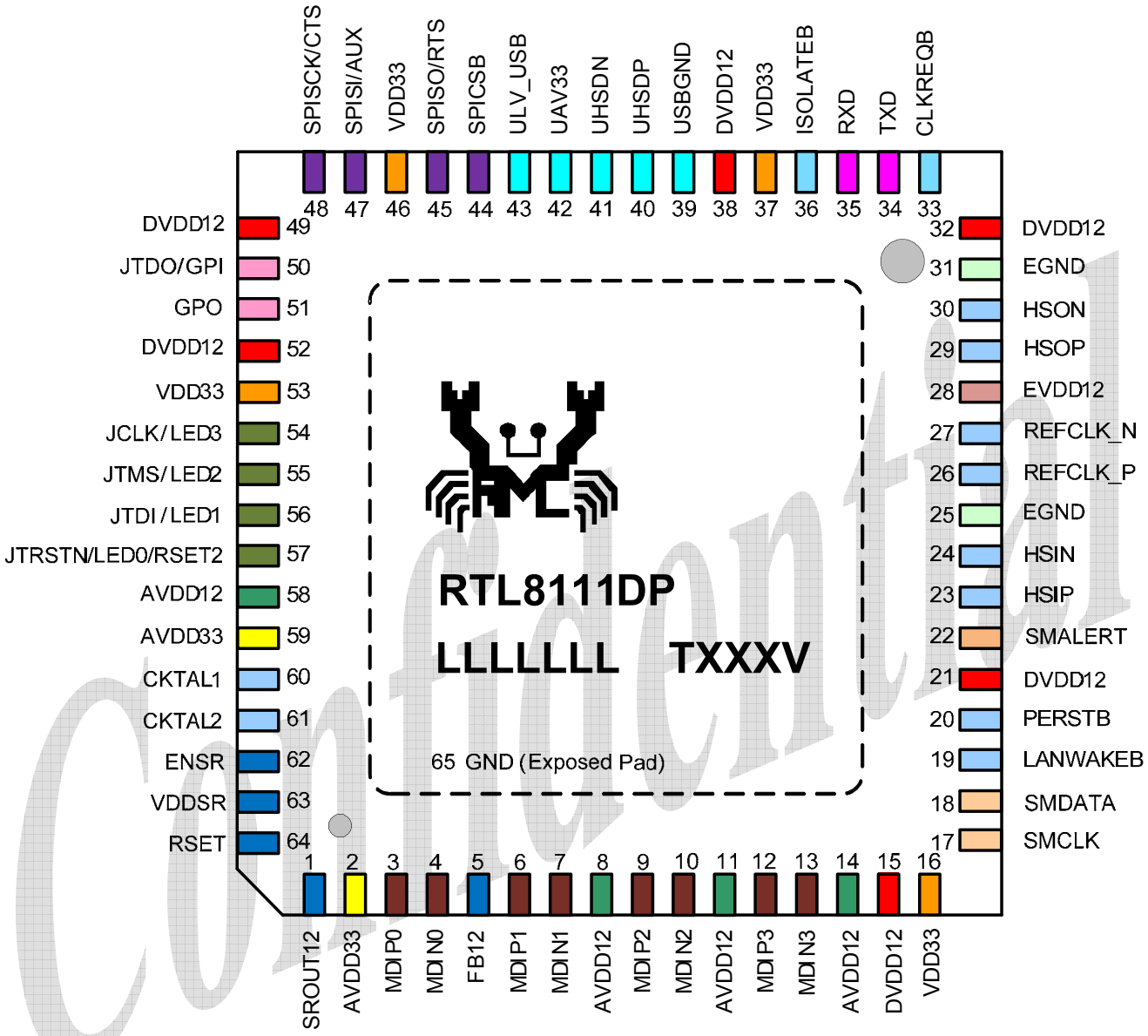


Figure 1. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 1. The version number is shown in the location marked 'V'.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	O:	Output
P:	Power	G:	Ground
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain		

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	19	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	36	Isolate Pin: Active low. Used to isolate the RTL8111DP from the PCI Express bus. The RTL8111DP will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	26	PCI Express Differential Reference Clock Source: 100MHz ±300ppm.
REFCLK_N	I	27	
HSOP	O	29	PCI Express Transmit Differential Pair.
HSON	O	30	
HSIP	I	23	PCI Express Receive Differential Pair.
HSIN	I	24	
PERSTB	I	20	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8111DP returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	33	Reference Clock Request Signal. This signal is used by the RTL8111DP to request starting of the PCI Express reference clock.

5.3. SPI (Serial Peripheral Interface) Flash Pins

Table 3. SPI Flash Pins

Symbol	Type	Pin No	Description
SPICSB	O	44	SPI Flash Chip Select.
SPISO	I	45	Input from SPI Flash Serial Data Output Pin.
SPISI/AUX	O	47	SPISI: Output to SPI Flash serial data input pin. AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111DP assumes that no Aux. Power exists.
SPISCK	O	48	SPI Flash Serial Data Clock.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	3	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	4	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	6	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	7	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIP2	IO	9	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair.
MDIN2	IO	10	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIP3	IO	12	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair.
MDIN3	IO	13	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No	Description
CKTAL1	I	60	Input of 25MHz Clock Reference.
CKTAL2	O	61	Output of 25MHz Clock Reference.

5.6. Regulator and Reference

Table 6. Regulator and Reference

Symbol	Type	Pin No	Description
SROUT12	O	1	Switching Regulator 1.2V Output. Connect to 5µH inductor.
FB12	I	5	Feedback Pin for Switching Regulator.
ENSR	I	62	3.3V: Enable switching regulator. 0V: Disable switching regulator.
VDDSR	P	63	Digital 3.3V Power Supply for Switching Regulator.
RSET	I	64	Reference. External resistor reference.
RSET2	I	57	Reference. External resistor reference.

Note: Refer to RTL8111DP-GR Layout Guide for switching regulator layout.

5.7. LEDs

Table 7. LEDs

Symbol	Type	Pin No	Description

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED1	LINK100	LINK10/100/1000	LINK	LINK100/ACT
LED2	LINK10	LINK10/100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000/ACT

Symbol	Type	Pin No
LED0	O	57
LED1	O	56
LED2	O	55
LED3	O	54

Note1: During power down mode, the LED signals are logic high.
Note2: LEDS1-0's initial value comes from the 93C46. If there is no 93C46, the default value of the (LEDS1, LEDS0) = (1, 1).

5.8. Power and Ground

Table 8. Power and Ground

Symbol	Type	Pin No	Description
VDD33	P	16, 37, 46, 53	Digital 3.3V Power Supply.
DVDD12	P	15, 21, 32, 38, 49, 52	Digital 1.2V Power Supply.
AVDD12	P	8, 11, 14, 58	Analog 1.2V Power Supply.
EVDD12	P	28	Analog 1.2V Power Supply.
AVDD33	P	2, 59	Analog 3.3V Power Supply.
EGND	G	25, 31	Analog Ground.
GND	G	65	Ground (Exposed Pad).

Note: Refer to the most updated schematic circuit for correct configuration.

5.9. GPIO Pins

Table 9. GPIO Pins

Symbol	Type	Pin No	Description
GPI	I	50	General Purpose Input Pin.
GPO	O	51	General Purpose Output Pin. This pin reflects the link up or link down state. High: Link up Low: Link down

5.10. USB Interface

Table 10. USB Interface

Symbol	Type	Pin No	Description
USBGND	I	39	USB Signal Ground.
UHSDP	IO	40	USB High-Speed D+.
UHSDN	IO	41	USB High-Speed D-.
UAV33	I	42	USB Analog Voltage 3.3V Input.
ULV_USB	I	43	USB Logic Voltage 1.2V Input.

5.11. UART Interface

Table 11. UART Interface

Symbol	Type	Pin No	Description
TXD	O	34	UART Data Transmit.
RXD	I	35	UART Data Receive.
RTS	O	45	Request to Send for UART.
CTS	I	48	Clear to Send for UART.

5.12. SMBus

Table 12. SMBus

Symbol	Type	Pin No	Description
SMCLK	IO	17	SMBus Clock.
SMDATA	IO	18	SMBus Data.
SMALERT	I	22	SMBus Assert Signal Input.

5.13. JTag

Table 13. JTag

Symbol	Type	Pin No	Description
JTDO	IO	50	Test Data Out.
JTDI	IO	56	Test Data In.
JCLK	I	54	Test Clock.
JTMS	I	55	Test Mode Select.
JTRSTN	I	57	Test Reset (Low Active).

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8111DP is compliant with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8111DP supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported.

6.1.1. PCI Express Transmitter

The RTL8111DP's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8111DP's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8111DP's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8111DP supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

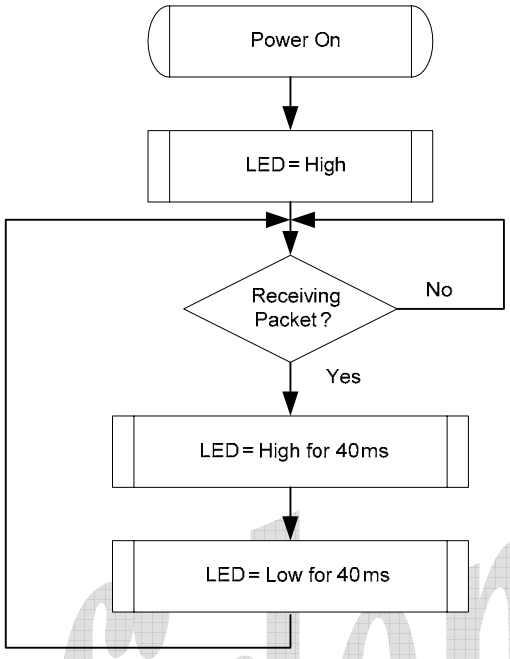


Figure 2. Rx LED

6.2.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

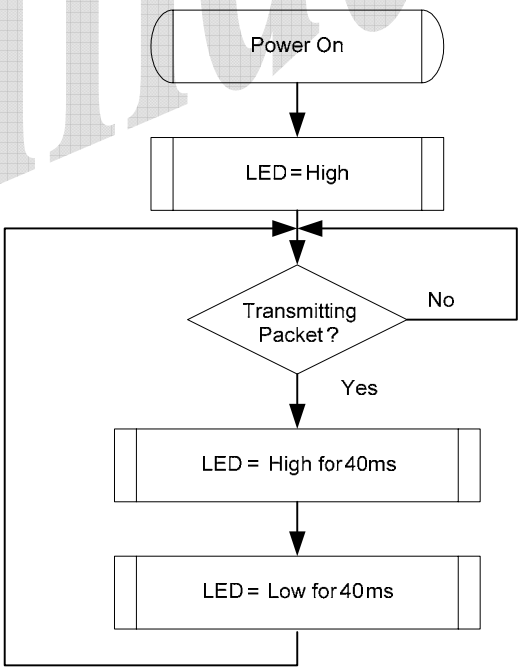


Figure 3. Tx LED

6.2.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

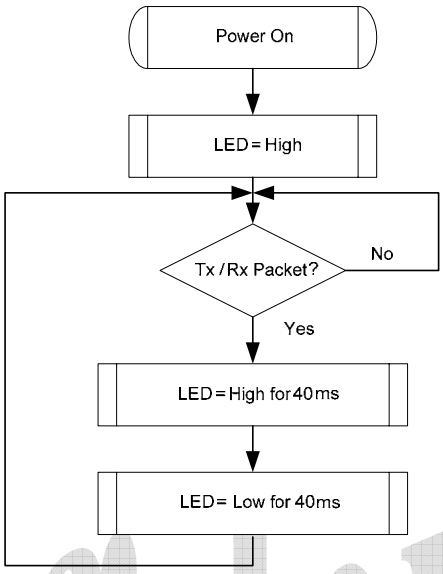


Figure 4. Tx/Rx LED

6.2.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111DP is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

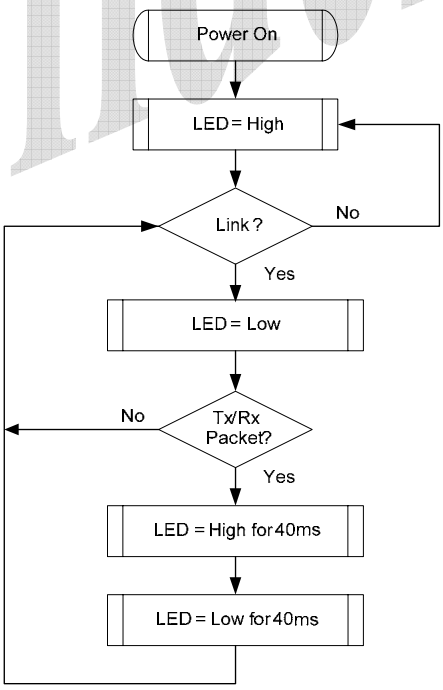


Figure 5. LINK/ACT LED

6.2.6. Customized LED Configuration

The RTL8111DP supports customizable LED operation modes via IO register offset 17h~18h. Table 14 describes the different LED actions.

Table 14. LED Select (IO Register Offset 17h~18h)

Bit	Symbol	RW	Description
15:12	LEDSEL3	RW	LED Select for PINLED3
11:8	LEDSEL2	RW	LED Select for PINLED2
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

1. Set IO register offset 0x55 bit 6 to 1h to enable the customized LED function.

2. Configure IO register offset 17h~18h to support your own LED signals. For example, if the value in the IO offset 0x17 is 0x8CA1h (1000110010100001b), the LED actions are:

- LED 0 is only on in 10M mode, with no blinking of TX/RX
- LED 1 is only on and with TX/RX blinking in 100M mode
- LED 2 is only on and with TX/RX blinking in 1000M mode
- LED 3 is only on in full duplex mode

Table 15. Customized LED

	LINK			ACT
Speed	Link 10M	Link100M	Link1000M	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 2	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	LED blinking in all speed TX/RX
LINK>0	LED on when selected speed link	LED blinking when selected speed TX/RX

Note1: ACT means blinking of TX and RX, and LINK indicates Link 10M, Link 100M, and Link 1000M.
Note2: There are four special modes
(Mode A) LED OFF Mode → Set all bits to 0.
(Mode B) Full Duplex LED Mode → Set LED 0=0, and either LED 1 or LED 2 or LED 3 >0.
LED 0=Full Duplex *LED 1=Follow Customized LED rule*
LED 2=Follow Customized LED rule *LED 3=Follow Customized LED rule*
(Mode C) Separated TX/RX LED Mode → Set LED0=0, LED1=0, LED2=X, LED3=1 (X mean any value).
LED 0=TX *LED 1=RX*
LED 2=Follow Customized LED rule by using value X *LED 3=LINK*
(Mode D) Separated Speed ACT Mode → Set LED0=0, LED1=1, LED2=X, LED3=1 (X mean any value).
LED 0=10ACT *LED 1=100ACT*
LED 2=Follow Customized LED rule by using value X *LED 3=1000ACT*

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8111DP operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), and CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8111DP's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.5. EEPROM Interface

The RTL8111DP requires the attachment of an external EEPROM. The 93C46/93C56 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8111DP to read from, and write data to, an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8111DP will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8111DP initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The interface consists of EESK, EECS, EEDO, and EEDI.

The correct EEPROM (i.e., 93C46/93C56) must be used in order to ensure proper LAN function.

Table 16. EEPROM Interface

EEPROM	Description
EECS	93C46/93C56 Chip Select.
EESK	EEPROM Serial Data Clock.
EEDI/Aux	Input Data Bus/Input Pin to Detect Whether Aux. Power Exists on Initial Power-On. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111DP assumes that no Aux. Power exists.
EEDO	Output Data Bus.

6.6. Power Management

The RTL8111DP is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8111DP can monitor the network for a Wakeup Frame, a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, or LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8111DP is in power down mode (D1 ~ D3):

- The Rx state machine is stopped. The RTL8111DP monitors the network for wakeup events such as a Magic Packet and Wakeup Frame in order to wake up the system. When in power down mode, the RTL8111DP will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx on-chip buffer.
- The on-chip buffer status and packets that have already been received into the Rx on-chip buffer before entering power down mode are held by the RTL8111DP.
- Transmission is stopped. PCI Express transactions are stopped. The Tx on-chip buffer is held.
- After being restored to D0 state, the RTL8111DP transmits data that was not moved into the Tx on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The $D3_{cold}$_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 FF, then PCI PMC = C3 FF)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 FF, then PCI PMC = 03 7E)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C3 FF (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 7F, then PCI PMC = C3 7F)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 7F, then PCI PMC = 03 7E)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 7E.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8111DP, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8111DP adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8111DP, e.g., a broadcast, multicast, or unicast address to the current RTL8111DP adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC[A] of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8111DP is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8111DP supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding wake-up method (message or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8111DP may assert the corresponding wake-up method (message or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8111DP to stop asserting the corresponding wake-up method (message or LANWAKEB) (if enabled).

When the RTL8111DP is in power down mode, e.g., D1-D3, the IO and MEM accesses to the RTL8111DP are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.7. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8111DP's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56/93C66 has completed or not.

Write VPD register: (write data to the 93C46/93C56/93C66)
Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8111DP, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46/93C56/93C66)
Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8111DP, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.3 Specifications for further information.

Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.

Note4: The VPD function of the RTL8111DP is designed to be able to access the full range of the 93C46/93C56/93C66 EEPROM.

6.8. Receive-Side Scaling (RSS)

The RTL8111DP is compliant with the new Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi CPU platforms.

6.8.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8111DP to store the following parameters: Hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port.
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address *(Note: The RTL8111DP does not support the IPv6 extension header hash type in RSS).*

Hash Bits

Hash bits are used to index the hash result into the indirection table

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.8.2. RSS Operation

After the parameters are set, the RTL8111DP will start hash calculation on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8111DP uses three methods to inform the system of incoming packets: Inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

6.9. Alert Specification Format (ASF)

ASF (Alert Standard Format) is a standard developed by the Pre-OS Working Group under DMTF (Distributed Management Task Force). ASF helps network management through capabilities such as system health monitoring, asset protection, and remote control.

IT departments have many choices regarding network management, but not all network management can operate in low-power and OS-absent states. ASF allows IT managers to manage and access the managed clients in an OS-absent environment.

From a technological point of view, an ASF managed client can provide advance warnings and system failure indications to the remote management console. The Ethernet controller sits on the motherboard or a plug-in network adapter card (NIC) in the local system. It collects information from various components in the system, including the CPU, chipset, BIOS, and sensors on the motherboard. It sends collected information to the management console running on a remote server.

6.9.1. Security-Extensions

RMCP Security-Extensions Protocol (RSP) provides integrity and anti-replay services for RMCP messages. When RSP is used, an entire RMCP message is encapsulated in an RSP header and trailer.

- An RSP header is inserted between the UDP header and the RMCP header and its presence is identified by the use of the RMCP security extensions UDP port number (0298h). The RSP header contains two fields: Session ID and Sequence Number. A Session ID is an arbitrary number used to identify the particular session state (algorithms, keys, etc). A Sequence Number is a unique monotonically increasing number which is used for the 32-bit sliding window anti-replay mechanism.
- An RSP trailer is located following the end of the RMCP message's Data block (i.e., security extensions are applied above the UDP layer). An RSP trailer contains 4 fields: Pad, Pad Length, Next Header, and Integrity Data, An integrity algorithm (e.g., HMAC-SHA1-96 defined in [RFC2404]) is performed over the specific fields of the RSP Header, RMCP Message, and RSP trailer, the result is placed in the Integrity Data field in the RSP trailer.

6.9.2. ASF (Alert Standard Format) 2.0 Support

Watchdog Timer

The RTL8111DP-GR supports two sets of start/stop watchdog timer. One is a software watchdog timer. The other is a firmware watchdog timer counter. The system BIOS supports an SMBus interface running SMBus Messages. The system initiating a 'power on' state enables the firmware watchdog timer of the RTL8111DP-GR.

ARP Ethernet

The RTL8111DP-GR supports auto-response ARP Ethernet packets in an OS-absent environment.

System Heartbeat and Alert PET

The RTL8111DP-GR supports system heartbeat and Platform Event Trap (PET) Alert packets. System heartbeat is a periodic message sent by the managed client indicating its presence to the management console. A PET alert is an alert message regarding environment, system firmware, and OS events sent by the managed client to the management console.

RMCP and Remote Control

The RTL8111DP-GR supports RMCP messages and remote control packets.

- RMCP Messages
  - Presence of ping/pong packets (80h/40h)
    Used to identify the presence of an ASF-RMCP-aware managed client on the network.
  - System state request/response packet (81h/41h)
    Used to identify the state of the managed client.
  - Capability request/response (82h/42h)
    Used to identify the client system's ASF capability.
  - Open session request/response (83h/43h)
    Used to establish a protected session between the management console and the managed client.
  - Close session request/response (84h/44h)
    Used to close a protected session.
- Support for four sets of remote control actions
  - Reset (10h), Power on (11h), Power off (12h), Power cycle reset (13h) (Refer to the ASF 2.0 specifications for more details)

ASF SMBus Messages

The RTL8111DP-GR supports a SMBus interface that is capable of operating in master or slave mode. (Refer to the SMBus 2.0 and ASF 2.0 specifications for more details about ASF SMBus Messages).

The RTL8111DP-GR's ASF SMBus Messages are listed below:

- SMBus ARP Messages
  The RTL8111DP-GR gets a SMBus Address from system firmware.
- ASF-Sensor Poll Messages (Get Event Status and Get Event Data)
  The RTL8111DP-GR monitors the system state through Get Event Status and Get Event Data messages, which poll ASF-sensors for individual events and present event status. The RTL8111DP-GR sends Platform Event Trap (PET) alerts to the management console when it observes abnormal events.
- Legacy Sensor Device Poll Message
  The RTL8111DP-GR monitors 8 sets of legacy sensors in the motherboard.
- Start Watchdog Timer
  The system firmware starts the RTL8111DP-GR's watchdog timer with a start watchdog timer message. If the watchdog timer times out, the RTL8111DP-GR will send a PET alert.
- Stop Watchdog Timer
  The system firmware stops the RTL8111DP-GR's watchdog timer with a stop watchdog timer message.
- Push Alert Messages (Message with/without retransmission)
  This message is used when the system firmware and sensors notify the RTL8111DP-GR to send a PET alert.
- Set System State Message
  This message is used by the managed client's firmware to record the client's current System State into the RTL8111DP-GR.
- Device Type Poll Message
  Allows a SMBus master to further determine the characteristics of a SMBus 2.0 device that responds to an ARP cycle with the ASF bit of its interface byte set to 1.
- Remote-Control Device Action Message
  The RTL8111DP-GR forces a remote control action to the managed client via a Remote-Control Device Action message.
- Boot Option Messages
  This message uses the SMBus Block Read Protocol. The managed client's firmware uses this message to retrieve the options sent over the network to the RTL8111DP-GR via the RMCP commands: Reset (10h), Power-up (11h), and Power Cycle Reset (13h).

6.10. DASH

The RTL8111DP is compliant with the DMTF's Desktop and mobile Architecture for System Hardware (DASH 1.1) Initiative. The DASH initiative is the next generation management standards proposed by the DMTF organization. It contains a set of specifications to achieve web services management for remote desktop and mobile systems over a secure out-of-band channel (Refer to *DASH Implementation Requirements (DSP0232)* for more details).

6.10.1. DASH Profile Support

The RTL8111DP firmware supports profiles as follows.

- Sensors Profile (DSP1009)
- Record Log Profile (DSP1010)
- Physical Asset Profile (DSP1011)
- Boot Control Profile (DSP1012)
- Fan Profile (DSP1013)
- Ethernet Port Profile (DSP1014)
- Power Supply Profile (DSP1015)
- Telnet Service Profile (DSP1016)
- SSH Service Profile (DSP1017)
- CPU Profile (DSP1022)
- Software Inventory Profile (DSP1023)
- Text Console Redirection Profile (DSP1024)
- System Memory Profile (DSP1026)
- Power State Management Profile (DSP1027)
- OS Status Profile (DSP1029)
- Battery Profile (DSP1030)
- Profile Registration (DSP1033)
- Simple Identity Management Profile (DSP1034)
- Host LAN Network Port Profile (DSP1035)
- IP Interface Profile (DSP1036)
- DHCP Client Profile (DSP1037)
- DNS Client Profile (DSP1038)
- Role Based Authorization Profile (DSP1039)
- Computer System Profile (DSP1052)

- Indications Profile (DSP1054)
- Base Desktop and Mobile Profile (DSP1058)
- USB Redirection Profile (DSP1077)

6.10.2. Protocol Implementation Requirements

DASH uses a CIM-based data model for representing managed resources and services that consists of Management Protocol and Transport Protocol layers.

Management Protocol

DASH uses the protocol defined in Web Services for Management Specification (DSP226) as the management protocol for supporting operations. Web Services for Management (WS-MAN) includes the following operations: WS-Transfer, WS-Enumeration, and WS-Eventing. WS-Transfer consists of GET and PUT actions; WS-Enumeration is used to get the CIM instances in the management system; WS-Eventing is used for alert events subscription and delivery.

Transport Protocol

DASH uses the HTTP 1.1 as the SOAP transport, TCP and IP as Transport Protocol to transfer web service packets.

All the CIM profiles, Management Protocol, and Transport Protocol are written in firmware.

6.10.3. Security Implementation Requirement

This section describes transport requirements, roles and authorization, and user account management.

Transport Requirements

The RTL8111DP defines two security classes for HTTP 1.1 transport:

Class A: Requires HTTP digest authentication for the user authentication. For this class, no encryption capabilities are required beyond the encryption of the password during the digest authentication exchange.

Class B: Defines two security profiles that are based on TLS (Transport Layer Security) with specifically selected modes and cryptographic algorithms.

Roles and Authorization

The RTL8111DP supports the Operational Roles as follows:

- Read-only User
- Operator
- Administrator

User Account Management

The RTL8111DP supports the operations for user account management and the respective DASH requirements as follows:

- Create an account
- Delete an account
- Modify the privileges of an account
- Modify the password of an account
- Change the role of an account

6.10.4. Discovery Requirements

Multiple discovery stages are required to accumulate the necessary information from the managed system.

Network Endpoint Discovery Stage

The RTL8111DP supports the endpoint discovery methods that described in the *Desktop and Mobile Systems Management White Paper* (DSP2014).

Management Access Point (MAP) Discovery Stage

The RTL8111DP supports the following phase process for MAP discovery:

Phase 1: RMCP Presence Ping/Pong.

Phase 2: WS-Management Identify method.

6.11. IP Security Offload

The Internet Protocol security (IPSEC) protocol suite is based on powerful encryption technologies, and adds security services to the IP layer that are compatible with both IPv4 and IPv6. With IPSec, users can create a secure VPN on demand.

6.11.1. IP Security Offload Crypto Engine

Using simple Source Address (SA) management, the IPSec Offload Crypto Engine is a partial 'bump-in-the-wire' implementation that handles only the encryption, decryption, and Integrity Check Value (ICV) calculation and check of the packet.

On the transmit side, it requires the TCP/IP stack to form the IPSec format before the engine calculates the ICV and encrypts the packet. The receive side requires TCP/IP stack to handle the sequence number check and parse through the AH/ESP protocol.

6.11.2. IP Security Offload Features

The RTL8111DP supports IP security offload features as follows:

- Modes
  - IPv4 AH/ESP protocol with AH&ESP combined mode. Processing of IP option is not supported
  - IPv6 AH/ESP extension Headers with AH&ESP combined mode. Processing of Non-IPSec extension header is not supported
- Supports Transport mode
- Up to 16 SAs both in TX and RX. Combined mode IPSec connection will handle two SAs per connection
- Crypto algorithm
  - Line speed guaranteed
  - Algorithm for AH: HMAC-sha1, AES-GMAC-128/192/256
  - Algorithm for ESP: HMAC-sha1, AES-GMAC-128/192/256, AES-GCM-128/192/256
- Compatible with Windows IPSec Offload V2 function. Supports combination LSOv2 + IPsecV2 (IPSecV2 Offload is supported under NDIS 6.1 and later versions)

7. Characteristics

7.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 17. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.3	+0.30	V
AVDD12, DVDD12	Supply Voltage 1.2V	-0.3	+0.12	V
EVDD12	Supply Voltage 1.2V	-0.3	+0.12	V
DCinput	Input Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

7.2. Recommended Operating Conditions

Table 18. Recommended Operating Conditions

Description	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD33, AVDD33	2.97	3.3	3.63	V
	AVDD12, DVDD12	1.1	1.2	1.32	V
	EVDD12	1.14	1.2	1.26	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

7.3. Crystal Requirements

Table 19. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.	-	25	-	MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a = 0°C ~ +70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a = 25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.5	mW

Note: The CLK source can come from other places in the system, but it must accord with the parameters above.

7.4. Oscillator Requirements

Table 20. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~+70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Jitter	-	-	-	50	ps
Vp-p	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note: The CLK source can come from other places in the system, but it must accord with the parameters above.

7.5. Thermal Characteristics

Table 21. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

7.6. DC Characteristics

Table 22. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
DVDD12, AVDD12	1.2V Supply Voltage	-	1.1	1.2	1.32	V
EVDD12	1.2V Supply Voltage	-	1.14	1.2	1.26	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage	-	1.8	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc33	Average Operating Supply Current from 3.3V	At 1Gbps with heavy network traffic	-	TBD	-	mA
Icc12	Average Operating Supply Current from 1.2V	At 1Gbps with heavy network traffic	-	TBD	-	mA

Note: Refer to the most updated schematic circuit for correct configuration.

7.7. AC Characteristics

7.7.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)

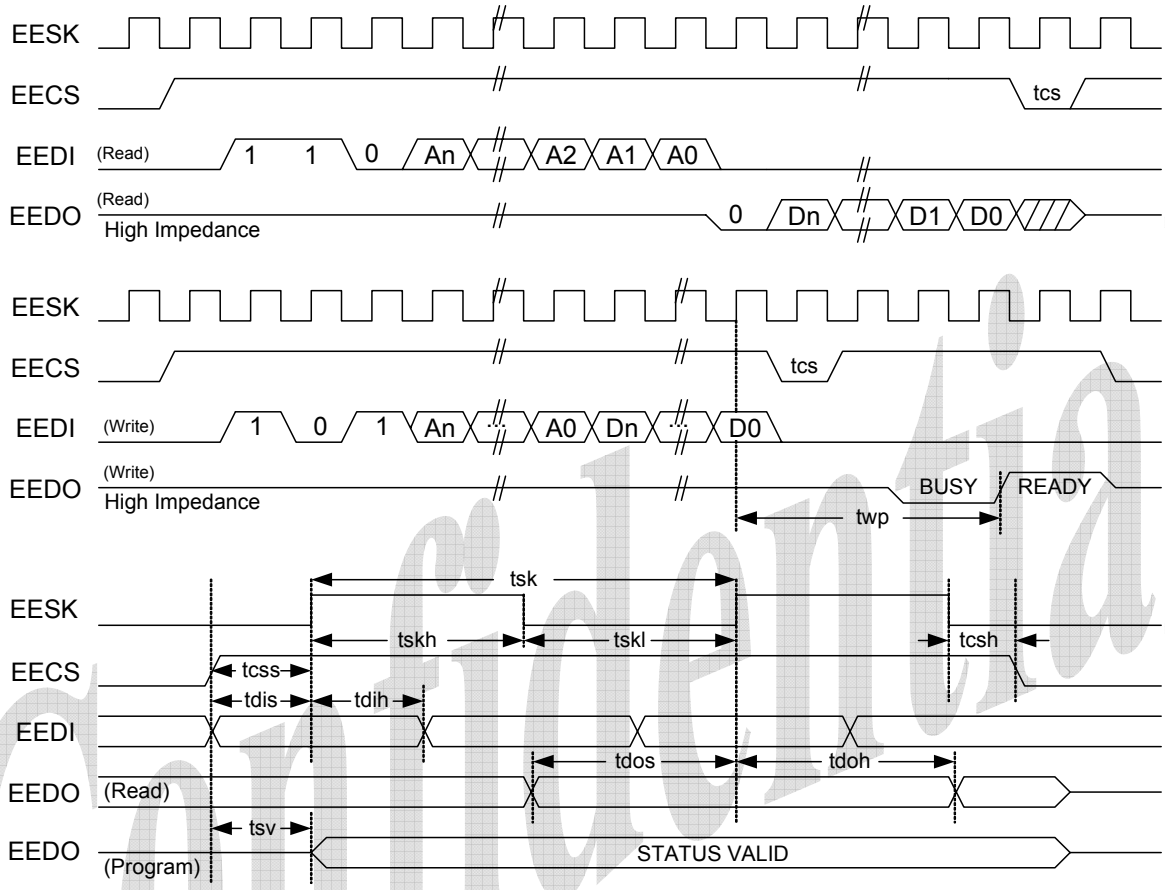


Figure 6. Serial EEPROM Interface Timing

Table 23. EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346	1000	-	ns
twp	Write Cycle Time	9346	-	10	ms
tsk	SK Clock Cycle Time	9346	4	-	µs
tskh	SK High Time	9346	1000	-	ns
tskl	SK Low Time	9346	1000	-	ns
tcss	CS Setup Time	9346	200	-	ns
tcsh	CS Hold Time	9346	0	-	ns
tdis	DI Setup Time	9346	400	-	ns
tdih	DI Hold Time	9346	400	-	ns
tdos	DO Setup Time	9346	2000	-	ns
tdoh	DO Hold Time	9346	-	2000	ns
tsv	CS to Status Valid	9346	-	1000	ns

7.8. PCI Express Bus Parameters

7.8.1. Differential Transmitter Parameters

Table 24. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum Tx Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The Tx DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid Tx Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

7.8.2. Differential Receiver Parameters

Table 25. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between The Jitter Median and Maximum Deviation from The Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

7.8.3. REFCLK Parameters

Table 26. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time Before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 10, page 34.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 7, page 33.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 7, page 33.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 9, page 33.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 7, page 33.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 7, page 33.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 7, page 33.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 13, page 35. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 12, page 34.

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8, page 33.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

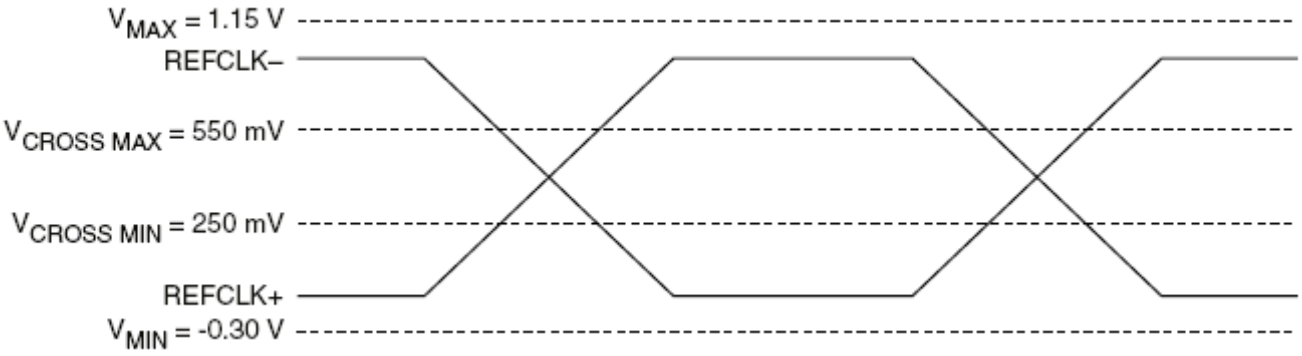


Figure 7. Single-Ended Measurement Points for Absolute Cross Point and Swing

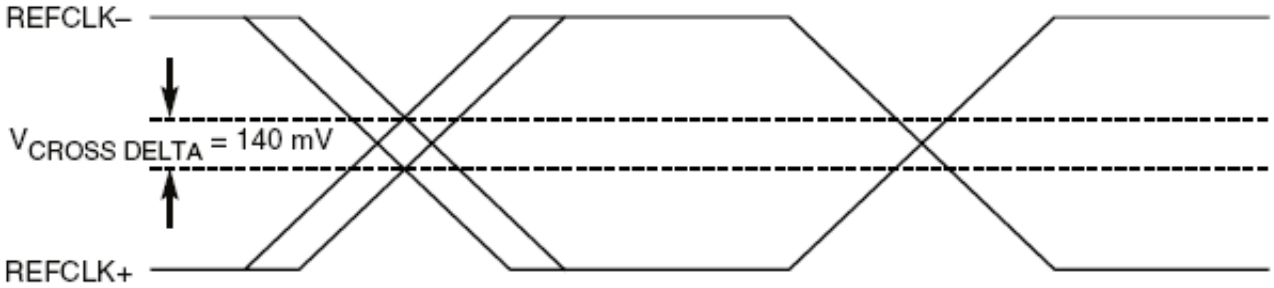


Figure 8. Single-Ended Measurement Points for Delta Cross Point

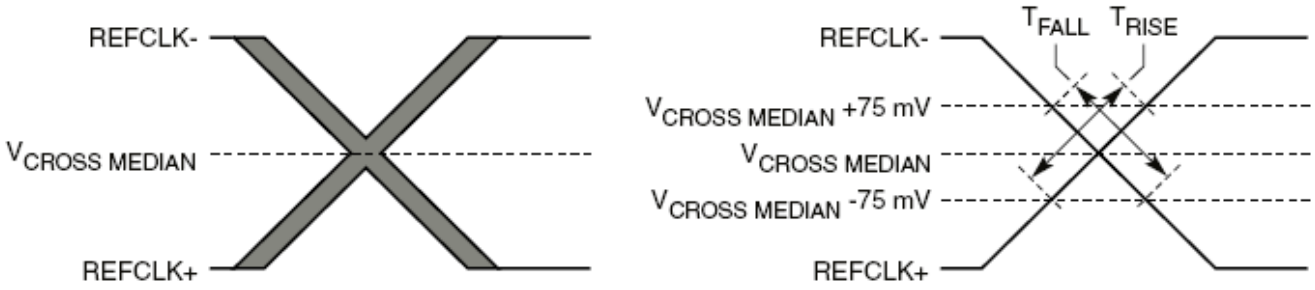


Figure 9. Single-Ended Measurement Points for Rise and Fall Time Matching

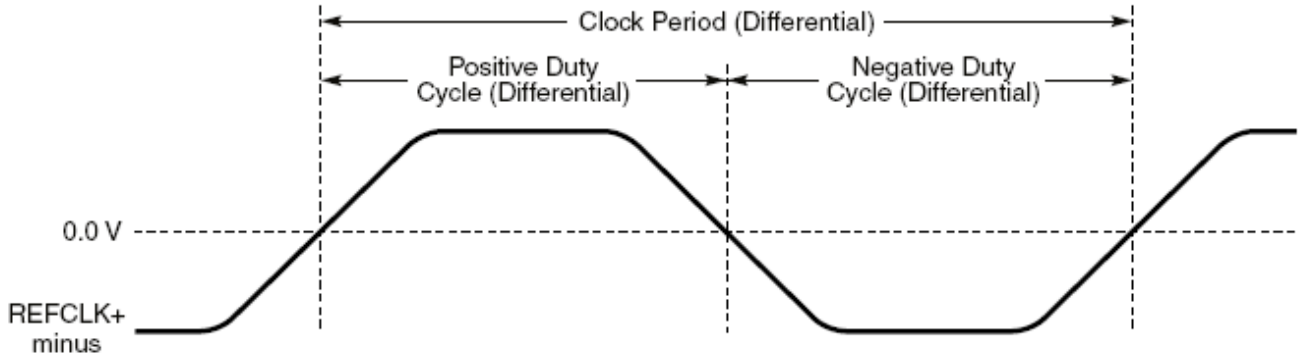


Figure 10. Differential Measurement Points for Duty Cycle and Period

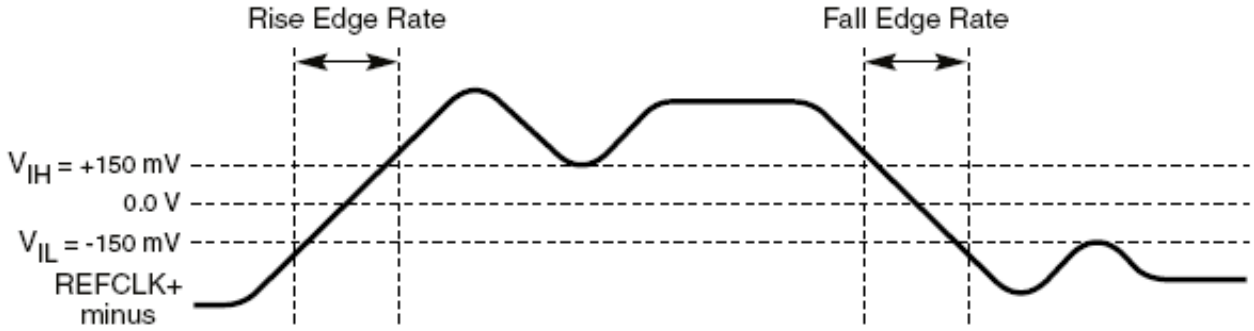


Figure 11. Differential Measurement Points for Rise and Fall Time

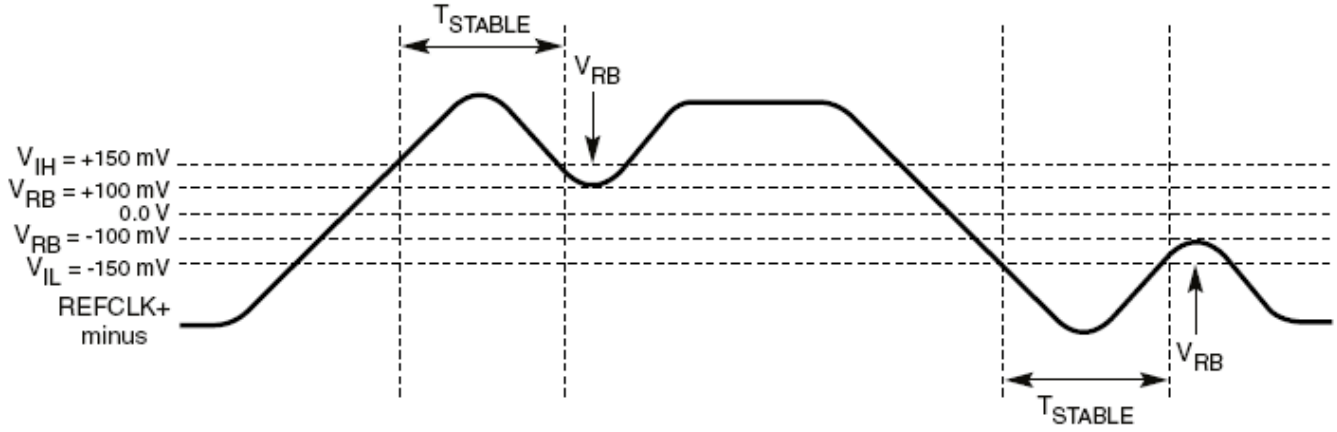


Figure 12. Differential Measurement Points for Ringback

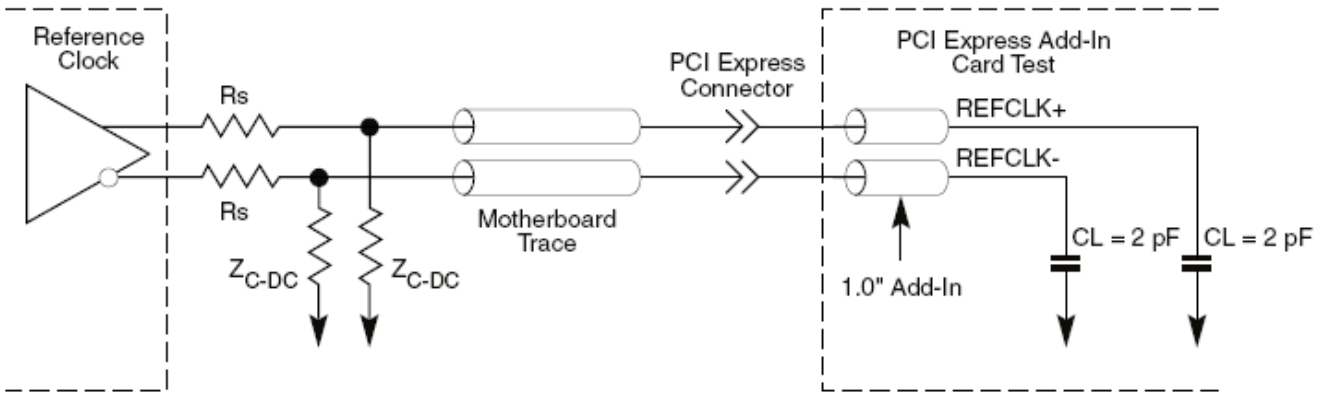


Figure 13. Reference Clock System Measurement Point and Loading

7.8.4. Auxiliary Signal Timing Parameters

Table 27. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable Before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
T_{FAIL}	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{WKRF}	LANWAKEB Rise – Fall Time	-	100	ns

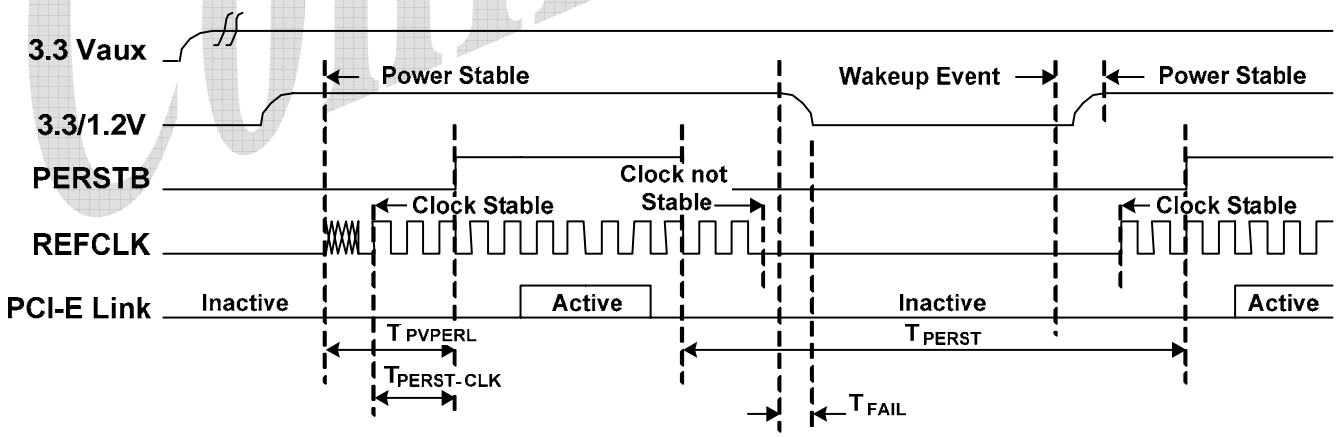
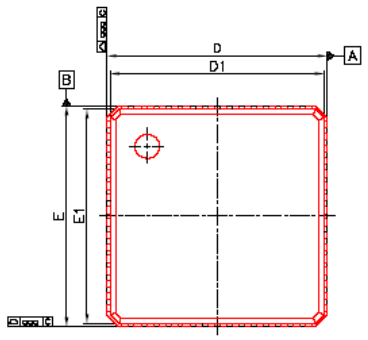
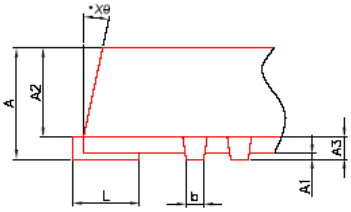


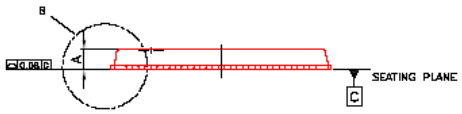
Figure 14. Auxiliary Signal Timing

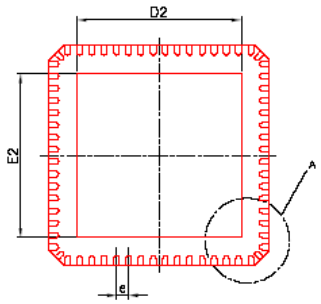
8. Mechanical Dimensions

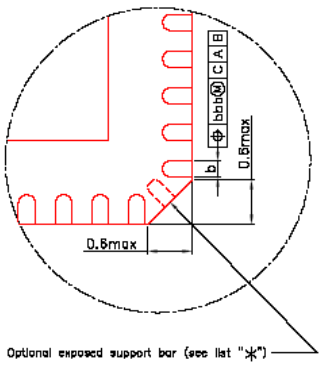




DETAIL : B







Optional exposed support bar (see list "*")

DETAIL : A

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3		0.20 REF			0.008 REF	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		9.00 BSC			0.354 BSC	
D1		8.75 BSC			0.344 BSC	
E		9.00 BSC			0.354 BSC	
E1		8.75 BSC			0.344 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table							
L/F	D2 (mm)			E2 (mm)			*
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.78	3.94	NO

Note: RTL8111DP's exposed pad size is L/F 3

OVER MOLD

TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chen	DWG NO.	CE064-SW1
ENG.	C.Y.Horng	REV NO.	C
QM.	S.T.Liao	PRODUCT CODE	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02
DWG.	R.K.Wang	SHT No.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	Add Exposed Pad Size & Support bar table	06/17/02

9. Ordering Information

Table 28. Ordering Information

Part Number	Package	Status
RTL8111DP-GR	64-Pin QFN 'Green' Package	

Note: See page 4 for package ID information.

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