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RTL8111G-CG
RTL8111GS-CG

INTEGRATED 10/100/1000M ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/10/07	First release.
1.1	2011/12/01	Revised Figure 1 RTL8111G Pin Assignments, page 4. Revised Table 7 Power and Ground, page 8. Revised Table 16 Power Sequence Parameter, page 20. Added Table 25 Reflow Profile Recommendations, page 24.
1.2	2012/02/24	Revised section 4 Pin Assignments, page 4. Added section 9.1 Power Sequence Parameters, page 21. Removed RealWOW!, SecureON Magic Packet Wake-Up, XTAL-Less, and LAN disable descriptions.
1.3	2012/04/06	Revised section 11 Mechanical Dimensions, page 31.
1.4	2012/05/30	Removed Header Data Split (HDS) information.
1.5	2012/08/24	Removed Virtual Machine Queue (VMQ) information. Revised Table 19 RTL8111G Electrostatic Discharge Performance, page 22. Added Table 20 RTL8111GS Electrostatic Discharge Performance, page 23.

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1. General Description

The Realtek RTL8111G-CG/RTL8111GS-CG 10/100/1000M Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111G/RTL8111GS offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111G/RTL8111GS supports the PCI Express 1.1 bus interface for host communications with power management, and complies with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8111G/RTL8111GS features embedded One-Time-Programmable (OTP) memory. The RTL8111G/RTL8111GS provides a built-in switching regulator (RTL8111GS) or LDO regulator (RTL8111G).

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111G/RTL8111GS.

The RTL8111G/RTL8111GS supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8111G/RTL8111GS can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8111G/RTL8111GS supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8111G/RTL8111GS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8111G/RTL8111GS is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8111G/RTL8111GS supports Receive-Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111G/RTL8111GS is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

Hardware

- Integrated 10/100/1000M transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Supports 1-Lane 2.5Gbps PCI Express Bus
- Embedded OTP memory
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function
- Transmit/Receive on-chip buffer support
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports 25MHz or 48MHz Oscillator
- Built-in switching regulator (RTL8111GS) and LDO regulator (RTL8111G)
- Supports power down/link down power saving/PHY disable mode
- Customized LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- 32-pin QFN 'Green' package
- Supports EMAC-393 ECMA ProxZzzy Standard for sleeping hosts
- Supports LTR (Latency Tolerance Reporting) and OBFF (Optimized Buffer Flush/Fill)
- Supports 16-set 128-byte Wake-Up Frame pattern exact matching
- Supports Microsoft WPD (Wake Packet Detection)

IEEE

- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)
- Supports Full Duplex flow control (IEEE 802.3x)

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports jumbo frame to 9K bytes
- Supports quad core Receive-Side Scaling (RSS)
- Supports Protocol Offload (ARP & NS)

3. System Applications

- PCI Express 10/100/1000M Ethernet on Motherboard, Notebook, or Embedded systems

4. Pin Assignments

4.1. RTL8111G Pin Assignments

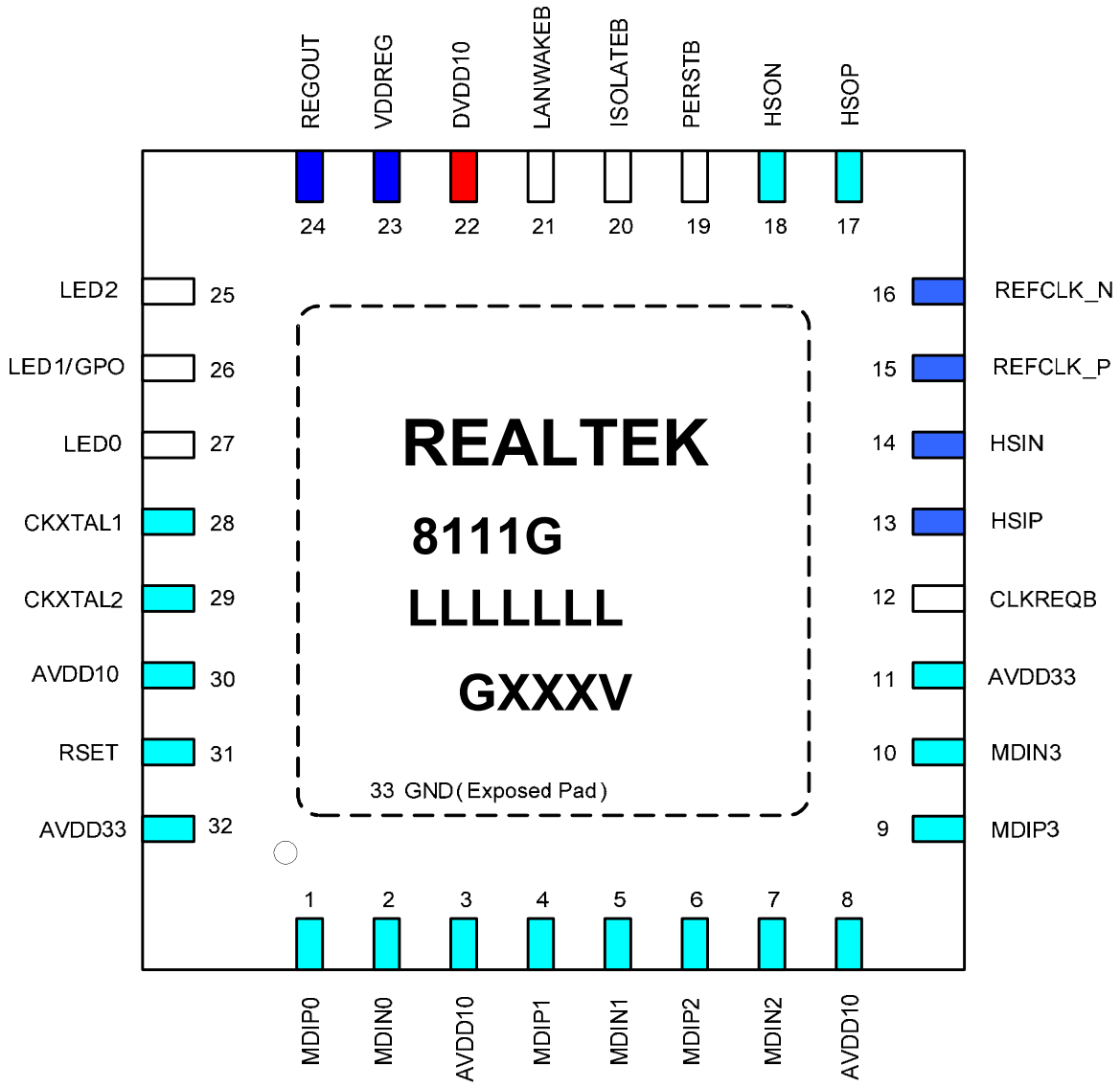


Figure 1. RTL8111G Pin Assignments

4.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 1).

4.3. RTL8111GS Pin Assignments

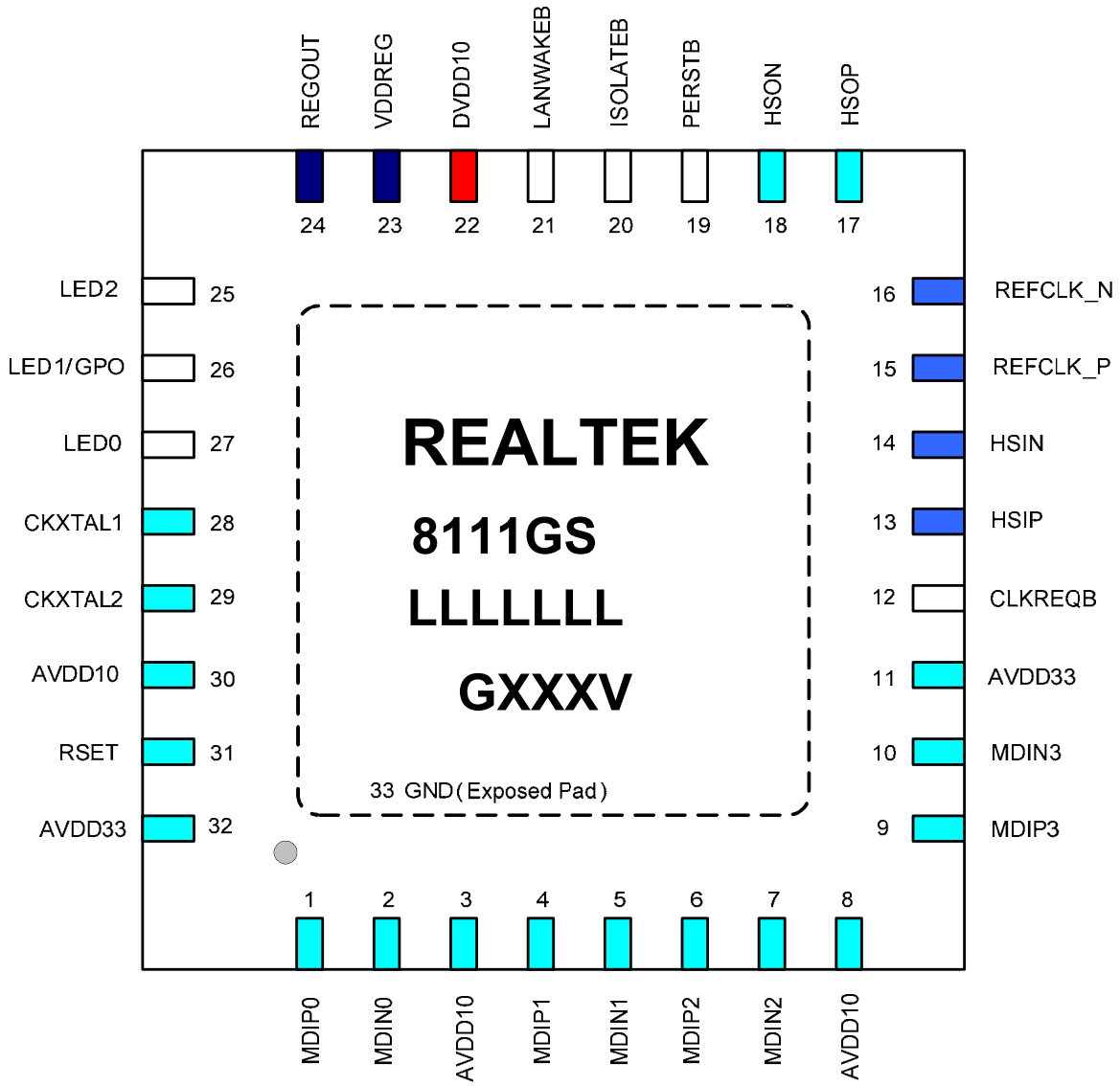


Figure 2. RTL8111GS Pin Assignments

4.4. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 2).

5. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State Bi-Directional Input/Output Pin	P:	Power

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	21	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	20	Isolate Pin: Active low. Used to isolate the RTL8111G/RTL8111GS from the PCI Express bus. The RTL8111G/RTL8111GS will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	15	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	16	
HSOP	O	17	PCI Express Transmit Differential Pair.
HSON	O	18	
HSIP	I	13	PCI Express Receive Differential Pair.
HSIN	I	14	
PERSTB	I	19	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8111G/RTL8111GS returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	12	Reference Clock Request Signal. This signal is used by the RTL8111G/RTL8111GS to request starting of the PCI Express reference clock.

5.3. Transceiver Interface

Table 3. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	1	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN0	IO	2	
MDIP1	IO	4	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	
MDIP2	IO	6	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIN2	IO	7	
MDIP3	IO	9	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
MDIN3	IO	10	

5.4. Clock

Table 4. Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	28	Input of 25MHz or 48MHz Clock Reference.
CKXTAL2	IO	29	Input of External Clock Source. Output of 25MHz or 48MHz Clock Reference.

5.5. Regulator and Reference

Table 5. Regulator and Reference

Symbol	Type	Pin No	Description
REGOUT	O	24	RTL8111GS: Switching Regulator 1.0V Output RTL8111G: LDO Regulator 1.0V Output
VDDREG	P	23	Digital 3.3V Power Supply for Switching/LDO Regulator.
RSET	I	31	Reference. External resistor reference.

Note: See section 7 Switching Regulator, page 19 for additional information.

5.6. LEDs

Table 6. LEDs

Symbol	Type	Pin No	Description
LED0	O	27	See section 6.2 Customizable LED Configuration, page 10 for details.
LED1/GPO	O	26	
LED2	O	25	

Note 1: During power down mode, the LED signals are logic high.
Note 2: The default value of the (LEDS1, LEDS0)=(1, 1).
Note 3: The LED1 pin can be changed to a GPO pin. The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (Default: LED1). For GPO function details, see section 5.8 GPO Pin, page 8.

5.7. Power and Ground

Table 7. Power and Ground

Symbol	Type	Pin No	Description
AVDD10	P	3, 8, 30	Analog 1.0V Power Supply.
DVDD10	P	22	1.0V Power Supply.
GND	P	33	Ground (Exposed Pad).
AVDD33	P	11, 32	3.3V Power Supply.

Note: Refer to the latest schematic circuit for correct configuration.

5.8. GPO Pin

Table 8. GPO Pin

Symbol	Type	Pin No	Description
GPO/LED1	I/O	26	General Purpose Input/Output Pin. The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (Default: LED1). 1. Power Saving Feature: Output pin 2. Link OK Feature: Output pin 3. PHY Disable mode (active low): Input pin

Note: The LED1 pin can be changed to a GPO pin. The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (Default: LED1).

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8111G/RTL8111GS complies with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8111G/RTL8111GS supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal is supported.

6.1.1. PCI Express Transmitter

The RTL8111G/RTL8111GS's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of two extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8111G/RTL8111GS's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8111G/RTL8111GS's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. Customizable LED Configuration

The RTL8111G/RTL8111GS supports customizable LED operation modes via IO register offset 18h~19h. Table 9 describes the different LED actions.

Table 9. LED Select (IO Register Offset 18h~19h)

Bit	Symbol	RW	Description
15:12	LEDCntl	RW	LED Feature Control
11:8	LEDSEL2	RW	LED Select for PINLED2
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 2: On only in 1000M mode, with blinking during TX/RX

Table 10. Customized LEDs

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 2	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

Note: There are two special modes:
LED OFF Mode: Set all bits to 0. All LED pin output become floating (power saving).
Fixed LED Mode: Set Option 1 LED table Mode: LED0=LED1=LED2=1 or 2 (see Table 11).

Table 11. Fixed LED Mode

Bit31~Bit0 Value	LED0	LED1	LED2
1XXX 0001 0001 0001	ACT	LINK	Full Duplex + Collision
1XXX 0010 0010 0010	Transmit	LINK	Receive

Note: 'X' indicates 'irrelevant'.

Table 12. LED Feature Control-1

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	LED2 Low Active	Indicates Option 1 of Table 14 is selected
1	LED0 High Active	LED1 High Active	LED2 High Active	Indicates Option 2 of Table 14 is selected

Table 13. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 14): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 14): Selected Speed LINK+ All Speed ACT

Table 14. LED Option 1 & Option 2 Settings

Link Bit			Active Bit	Description		
10	100	1000		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	LED Off		
0	0	0	1	-	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
0	0	1	0	$Link_{1000}$	-	-
0	0	1	1	$Link_{1000}$	Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
0	1	0	0	$Link_{100}$	-	-
0	1	0	1	$Link_{100}$	Act_{100}	Act_{10}+Act_{100}+Act_{1000}
0	1	1	0	$Link_{100}$+$Link_{1000}$	-	-
0	1	1	1	$Link_{100}$+$Link_{1000}$	Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
1	0	0	0	$Link_{10}$	-	-
1	0	0	1	$Link_{10}$	Act_{10}	Act_{10}+Act_{100}+Act_{1000}
1	0	1	0	$Link_{10}$+$Link_{1000}$	-	-
1	0	1	1	$Link_{10}$+$Link_{1000}$	Act_{10}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}
1	1	0	0	$Link_{10}$+$Link_{100}$	-	-
1	1	0	1	$Link_{10}$+$Link_{100}$	Act_{10}+Act_{100}	Act_{10}+Act_{100}+Act_{1000}
1	1	1	0	$Link_{10}$+$Link_{100}$+$Link_{1000}$	-	-
1	1	1	1	$Link_{10}$+$Link_{100}$+$Link_{1000}$	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}

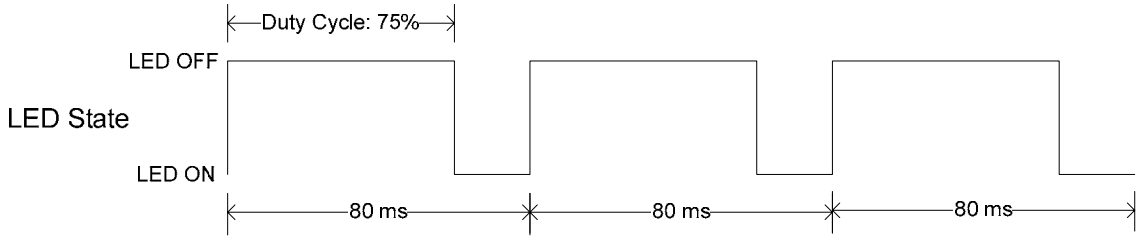
Note:
Act_{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act_{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act_{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
$Link_{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link_{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link_{1000}$ = LED lit when Ethernet connection established at 1000Mbps.

6.2.1. LED Blinking Frequency Control

The RTL8111G/RTL8111GS supports LED blinking frequency control via IO register offset 1Ah to control user's LED blinking frequency and duty cycle (see Table 15). If the IO offset 0x1A is 0x0B (00001011b), the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 3.

Table 15. LED Blinking Frequency Control (IO Offset 1Ah)

Bit	RW	Description
3:2	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
1:0	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assumes the LED is in low active.

Figure 3. LED Blinking Frequency Example

6.3. PHY Transceiver

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8111G/RTL8111GS operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), or CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8111G/RTL8111GS's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3.3. Link Down Power Saving Mode

The RTL8111G/RTL8111GS implements link-down power saving, greatly cutting power consumption when the network cable is disconnected. The RTL8111G/RTL8111GS automatically enters link down power saving mode ten seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6.3.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.4. Power Management

The RTL8111G/RTL8111GS complies with ACPI (Rev 1.0, 1.0b, 2.0, 3.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8111G/RTL8111GS can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or the LANWAKEB pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs.

When the RTL8111G/RTL8111GS is in power down mode (D1~D3):

- The RX state machine is stopped. The RTL8111G/RTL8111GS monitors the network for wake-up events such as a Magic Packet and Wake-Up Frame in order to wake-up the system. When in power down mode, the RTL8111G/RTL8111GS will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8111G/RTL8111GS.
- Transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held.
- After being restored to D0 state, the RTL8111G/RTL8111GS transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The $D3_{cold}$_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8111G/RTL8111GS, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8111G/RTL8111GS.
- The received Magic Packet does not contain a CRC error.
- The RTL8111G/RTL8111GS driver has set up the needed registers (automatically set), and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8111G/RTL8111GS, e.g., a broadcast, multicast, or unicast address to the current RTL8111G/RTL8111GS.
- The received Wake-Up Frame does not contain a CRC error.
- The RTL8111G/RTL8111GS driver has set up the needed registers (automatically set).
- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8111G/RTL8111GS is configured to allow direct packet wake-up, e.g., a broadcast, multicast, or unicast network packet.
- The 128 bytes of the received Wake-Up Frame exactly matches the 128 bytes of the sample Wake-Up Frame pattern given by the local machine's OS.

Note 1: 16-bit CRC: The RTL8111G/RTL8111GS supports 16-set 16-bit CRC wake-up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^{5}+1$.

Note 2: 128-byte Wake-Up Frame: The RTL8111G/RTL8111GS supports 16-set 128-byte wake-up frames. If enabled, the 16-bit CRC wake-up match will be disabled.

The corresponding wake-up method (message or LANWAKEB) is asserted only when the following conditions are met:

- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8111G/RTL8111GS may assert the corresponding wake-up method (message or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15~11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wake-Up Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8111G/RTL8111GS to stop asserting the corresponding wake-up method (message or LANWAKEB) (if enabled).

When the RTL8111G/RTL8111GS is in power down mode, e.g., D1~D3, the IO, and MEM accesses to the RTL8111G/RTL8111GS are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting). The setting may be changed from the eFUSE, if required.

6.5. Receive-Side Scaling (RSS)

The RTL8111G/RTL8111GS complies with the Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi-CPU platforms.

6.5.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8111G/RTL8111GS that it should store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port.

- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address
  (Note: The RTL8111G/RTL8111GS does not support the IPv6 extension header hash type in RSS).

Hash Bits

Hash bits are used to index the hash result into the indirection table.

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.5.2. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It maintains a network presence for a sleeping higher power host. Protocol offload prevents spurious wake-up and further reduces power consumption. It maintains connectivity while hosts are asleep, including receiving requests from other nodes on the network, ignoring packets, generating packets while in the sleep state (e.g., the Ethernet Controller will generate ARP responses if the same MAC and IPv4 address are provided in the configuration data), and intelligently waking up host systems. The RTL8111G/RTL8111GS supports the ECMA (European Computer Manufacturers Association) specification including proxy configuration and management, IPv4 ARP, IPv6 NDP, and wake-up packets. The RTL8111G/RTL8111GS also supports optional ECMA items such as QoS tagged packets and duplicate address detection.

6.5.3. RSS Operation

After the parameters are set, the RTL8111G/RTL8111GS will start hash calculations on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8111G/RTL8111GS uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

6.6. Energy Efficient Ethernet (EEE)

The RTL8111G/RTL8111GS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.7. PHY Disable Mode

The RTL8111G/RTL8111GS can power down the PHY using board-level control signals.

6.8. Latency Tolerance Reporting (LTR)

The RTL8111G/RTL8111GS supports PCIe 3.0 LTR (Latency Tolerance Reporting).

The LTR mechanism enables Endpoints to report service latency requirements for Memory Reads/Writes. The CPU utilizes LTR to determine transfers from low power (C7) to high power (C0) mode. See the PCIe 3.0 specification for details.

6.9. Optimized Buffer Flush/Fill (OBFF)

The RTL8111G/RTL8111GS supports OBFF (Optimized Buffer Flush/Fill).

The RTL8111G/RTL8111GS OBFF uses the LANWAKEB pin or a PCIe message to request a Buffer Flush/Fill. Once initiated the platform should not be returned to the idle state for a minimum of 10µs.

The RTL8111G/RTL8111GS LANWAKEB pin operates in both in-band and out-of-band OBFF modes (input pin in in-band mode, and output pin in out-of-band mode). See the PCIe 3.0 specification for details.

6.10. Wake Packet Detection (WPD)

The RTL8111G/RTL8111GS supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

7. Switching Regulator (RTL8111GS Only)

The RTL8111GS incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. Note that the switching regulator 1.0V output pin (REGOUT) must be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

Note: Refer to the separate RTL8111G(S) layout guide for details.

8. LDO Regulator (RTL8111G Only)

The RTL8111G incorporates a linear Low-Dropout (LDO) regulator that features high power supply ripple rejection and low output noise. The RTL8111G embedded LDO regulator does not require power inductors on the PCB; only a 1.0V output capacitor between its 1.0V output and analog ground for phase compensation, which saves cost and PCB real estate. Use an X5R low-ESR ceramic capacitor, with a capacitance of at least 1µF, to enhance output voltage stability.

The output capacitors (and bypass capacitors) should be placed as close as possible to the power pins (AVDD10 and DVDD10) for adequate filtering.

Note that with regard to voltage conversion efficiency, LDO is inferior to a switching regulator. This balance between cost, size, and efficiency should be taken into consideration when choosing the regulator type.

Note: The embedded LDO is designed for the RTL8111G internal use only. Do not provide this power source to other devices.

9. Power Sequence

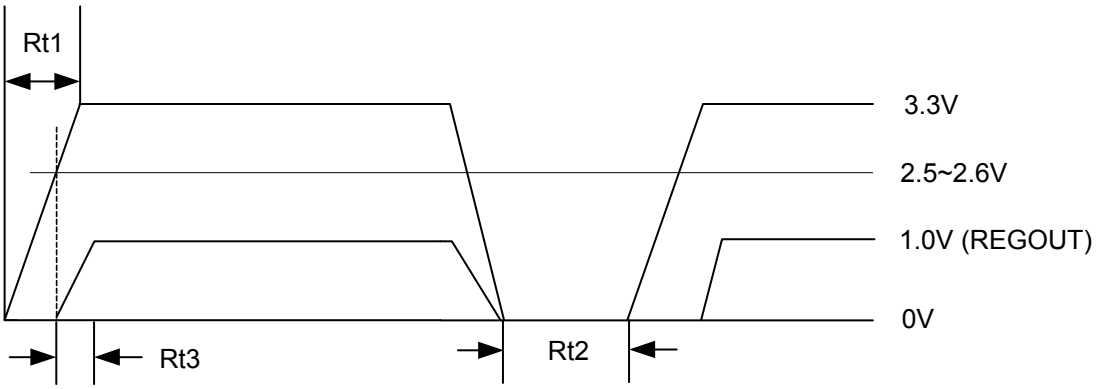


Figure 4. Power Sequence

Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

9.1. Power Sequence Parameters

The RTL8111G/RTL8111GS does not support fast 3.3V rising under normal circumstance. The 3.3V rise time must be controlled over 0.5ms.

Rise Time > 0.5ms

No action to take.

Rise Time 0.1ms~0.5ms

If the rise time is between 0.1ms and 0.5ms, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8111G/RTL8111GS so as to be safely under the system's 3.3V OCP threshold.

For example:

- Assume customer supply power rise time of the RTL8111G/RTL8111GS is 0.374ms
- The system 3.3V OCP is 9A
- The inrush current of other 3.3V devices is 5.64A

The inrush current to the RTL8111G/RTL8111GS must be less than 1.12A, otherwise an unanticipated system OCP may be triggered. It can be expressed in the following formula:

Inrush current to the RTL8111G/RTL8111GS < (System 3.3V OCP - inrush current of other 3.3V devices) / 3

Rise Time < 0.1ms

If the rise time is less than 0.1ms, there is risk of an unanticipated ESD trigger event, which may cause permanent damage to the RTL8111G/RTL8111GS.

If there is any action that involves consecutive ON/OFF toggling of the switching/LDO regulator source (3.3V), the design must make sure the OFF state of both the switching/LDO regulator source (3.3V) and output (1.0V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

10. Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 17. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33	Supply Voltage 3.3V	-0.3	3.6	V
AVDD10, DVDD10	Supply Voltage 1.0V	-0.3	1.2	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	-0.3	3.6	V
1.0V DCinput 1.0V DCoutput	Input Voltage Output Voltage	-0.3	1.2	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

10.2. Recommended Operating Conditions

Table 18. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	AVDD33	3.14	3.3	3.46	V
	AVDD10, DVDD10	0.95	1.0	1.05	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

10.3. RTL8111G Electrostatic Discharge Performance

Table 19. RTL8111G Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: |4KV|
MM ESD	All Pins: |150V|
CDM ESD	All Pins: |1KV|
Cable ESD	All MDI Pins: |5KV|
	All Pairs: |16KV|
Latch Up	I/O Pin: 400mA Power Pin: 1.5×VDD

Note: 'All MDI pins' means the ESD current is introduced to each MDI pin separately. 'All pairs' means the ESD current is introduced to the aggregated MDI pairs.

10.4. RTL8111GS Electrostatic Discharge Performance

Table 20. RTL8111GS Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: |3.5KV|
MM ESD	All Pins: |150V|
CDM ESD	All Pins: |1KV|
Cable ESD	All MDI Pins: |6KV|
	All Pairs: |16KV|
Latch Up	I/O Pin: 400mA Power Pin: 1.5×VDD

Note: 'All MDI pins' means the ESD current is introduced to each MDI pin separately. 'All pairs' means the ESD current is introduced to the aggregated MDI pairs.

10.5. Crystal Requirements

Table 21. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
Jitter	Broadband Peak-to-Peak Jitter[2]	-	-	200	ps
DL	Drive Level.	-	-	0.3	mW

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

10.6. Oscillator Requirements

Table 22. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/48	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[2]	-	-	-	200	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 48MHz RMS=3ps.

10.7. Environmental Characteristics

Table 23. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

10.8. DC Characteristics

Table 24. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
AVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
AVDD10, DVDD10	1.0V Supply Mean Voltage	-	0.95	1.0	1.05	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage	-	2.0	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc33	Average Operating Supply Current from 3.3V	At 1Gbps with heavy network traffic	-	70	-	mA
Icc10	Average Operating Supply Current from 1.0V	At 1Gbps with heavy network traffic	-	300	-	mA

Note 1: Refer to the latest schematic circuit for correct configuration.
Note 2: All Supply Mean Voltage power noise <±5% of Mean Voltage.

10.9. Reflow Profile Recommendations

Table 25. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time $(t_p)^2$ within 5°C of Peak T_P	20 seconds	20 seconds

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package body surface.
Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.
Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

10.10. PCI Express Bus Parameters

10.10.1. Differential Transmitter Parameters

Table 26. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.05	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note 1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note 2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

10.10.2. Differential Receiver Parameters

Table 27. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.05	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between The Jitter Median and Maximum Deviation from The Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

10.10.3. REFCLK Parameters

Table 28. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-0.3	-	V	1, 8

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note 1: Measurement taken from single-ended waveform.

Note 2: Measurement taken from differential waveform.

Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 8, page 29.

Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 5, page 28.

Note 5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 5, page 28.

Note 6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 7, page 28.

Note 7: Defined as the maximum instantaneous voltage including overshoot. See Figure 5, page 28.

Note 8: Defined as the minimum instantaneous voltage including undershoot. See Figure 5, page 28.

Note 9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 5, page 28.

Note 10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note 11: System board compliance measurements must use the test load card described in Figure 11, page 30. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note 12: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range. See Figure 10, page 29.

*Note 13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note 14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 6, page 28.

Note 15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

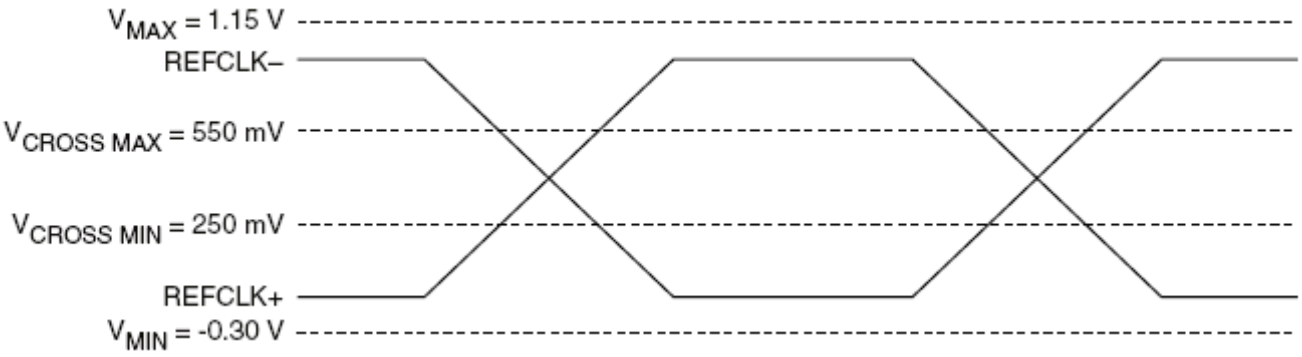


Figure 5. Single-Ended Measurement Points for Absolute Cross Point and Swing

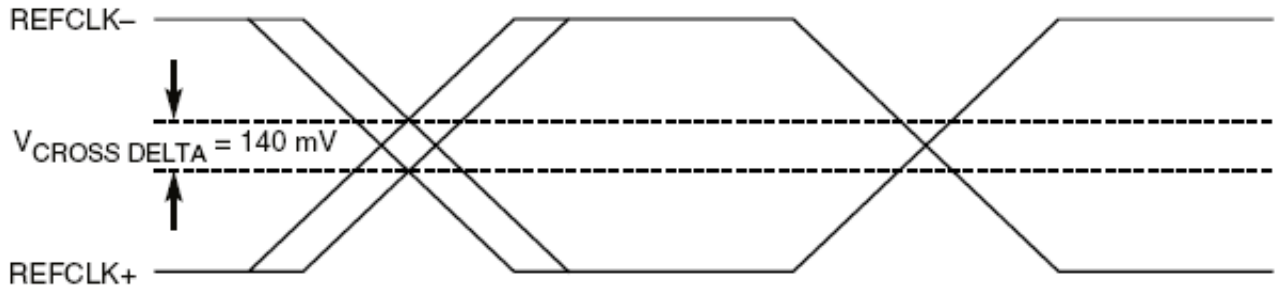


Figure 6. Single-Ended Measurement Points for Delta Cross Point

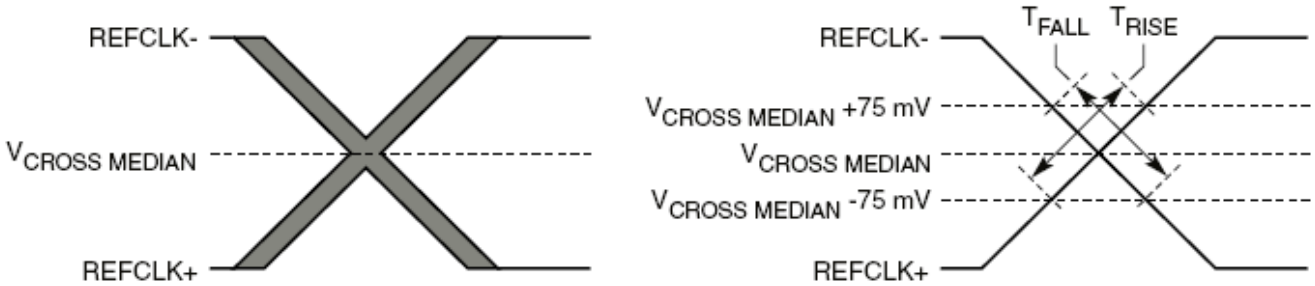


Figure 7. Single-Ended Measurement Points for Rise and Fall Time Matching

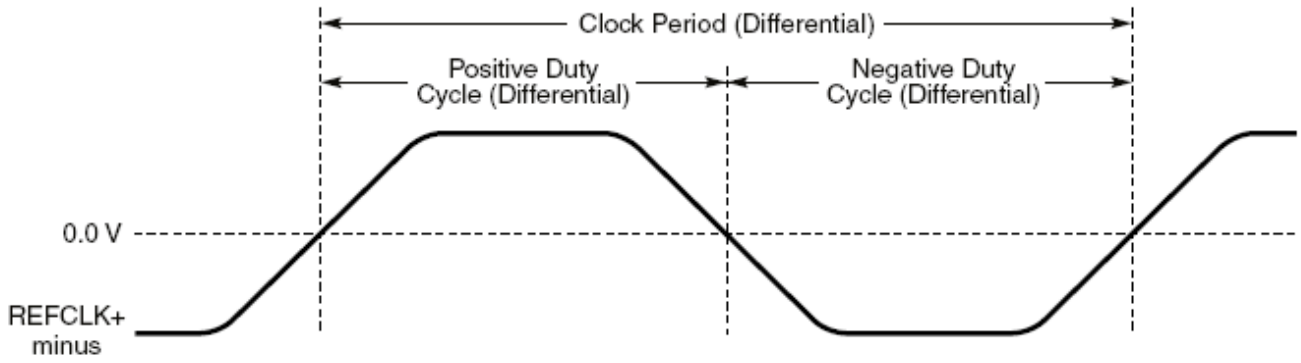


Figure 8. Differential Measurement Points for Duty Cycle and Period

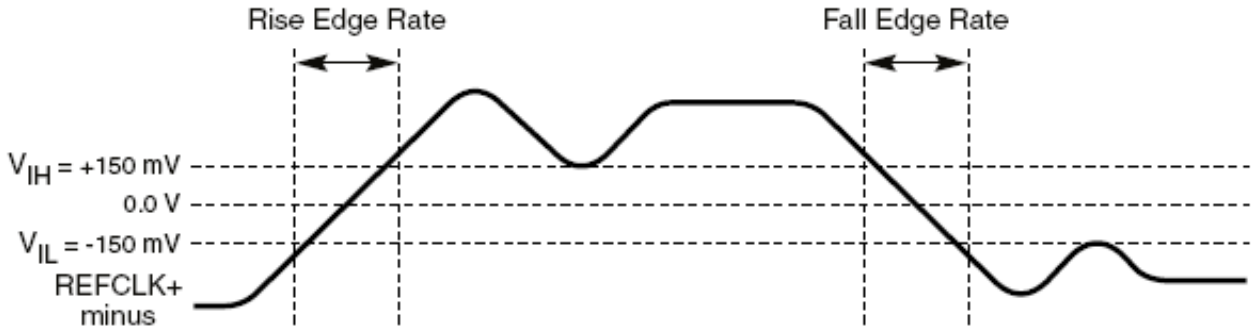


Figure 9. Differential Measurement Points for Rise and Fall Time

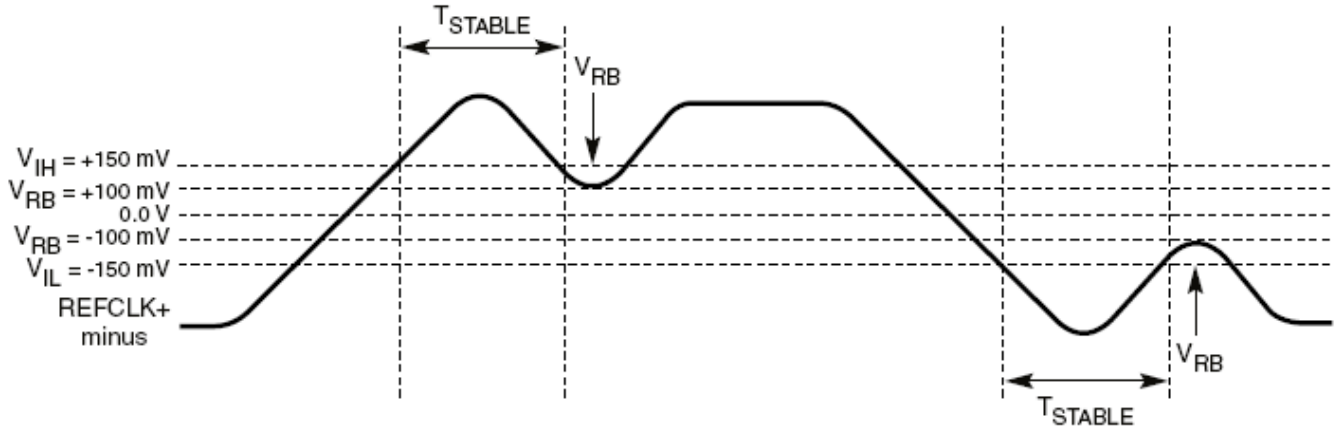


Figure 10. Differential Measurement Points for Ringback

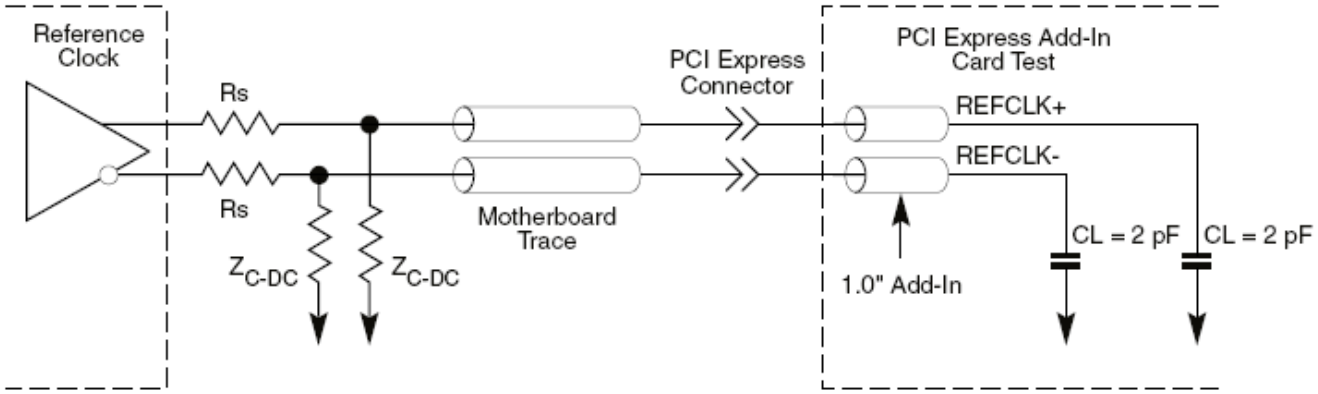


Figure 11. Reference Clock System Measurement Point and Loading

10.10.4. Auxiliary Signal Timing Parameters

Table 29. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{PERSTB-RTD}$	PERSTB Rising Time Duration	10	-	ms
T_{FAIL}	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PWRON}	3.3Vaux Power On Time (Refer to Section 9, Page 20)	-	-	ms

Note 1: T_{FAIL} means 500 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.
Note 2: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

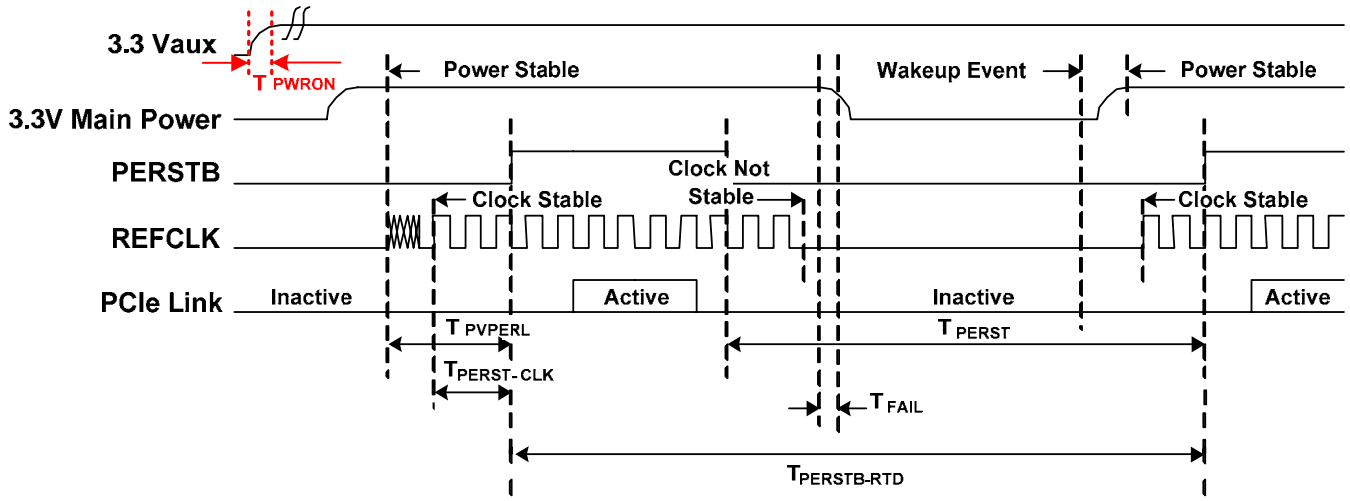
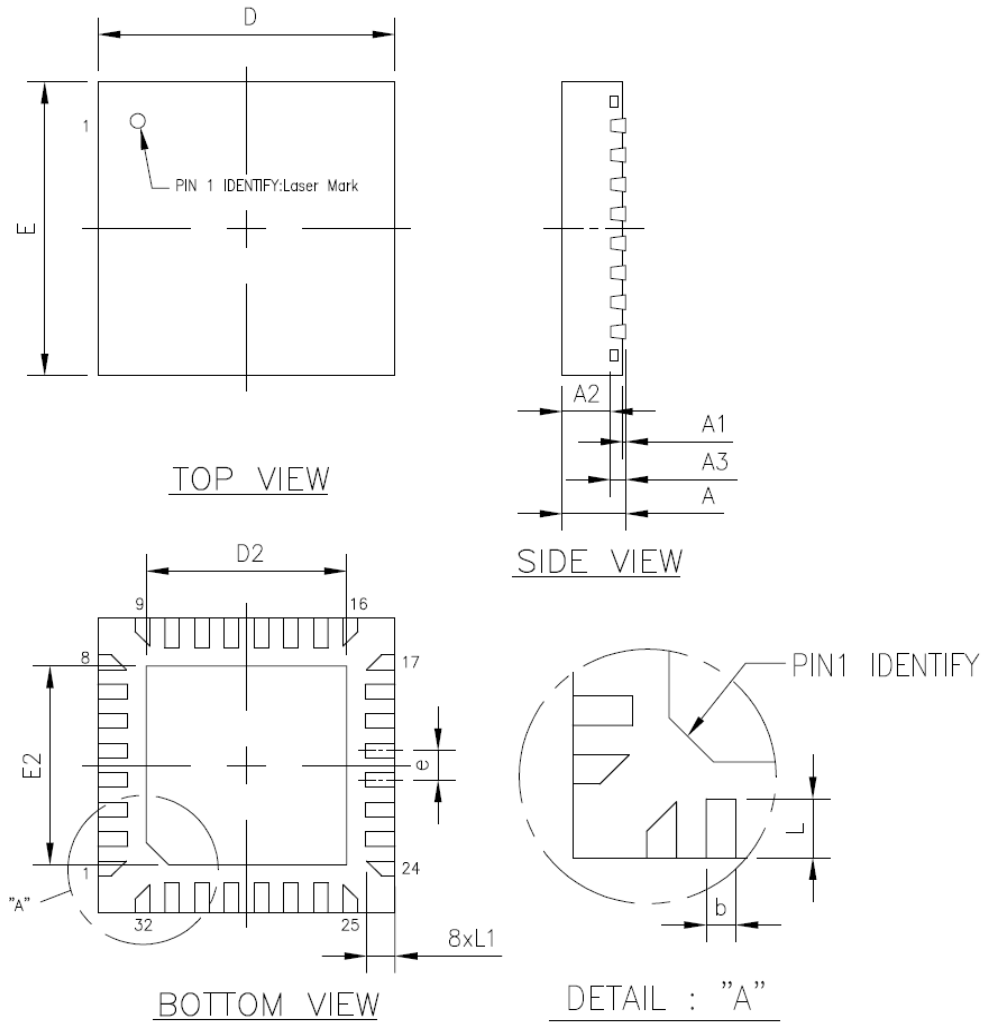


Figure 12. Auxiliary Signal Timing

11. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	-	0.65	0.70	-	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	4.00 BSC			0.157 BSC		
D2/E2	2.55	2.70	2.85	0.100	0.106	0.112
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 30. Ordering Information

Part Number	Package	Status
RTL8111GS-CG	32-Pin QFN 'Green' Package (switching regulator)	-
RTL8111G-CG	32-Pin QFN 'Green' Package (LDO regulator)	-

Note: See page 4 for package identification information.

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