RTL8111B-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

LAYOUT GUIDE

Rev. 1.1
12 June 2006
Track ID: JATR-1076-21

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw

COPYRIGHT

DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the RTL8111B-GR Gigabit Ethernet controller.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/07/27	First release.
1.1	2006/06/12	Modified section 4.2 Ground Plane Layout, page 9.

Table of Contents

List of Figures

1. Introduction

The Realtek RTL8111B-GR Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111B-GR offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.0a bus interface for host communications with power management and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™, Re-LinkOk, and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111B-GR.

The RTL8111B-GR is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The device also features next-generation inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8111B-GR is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8111B-GR. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8111B-GR.

(3) Simplify the task of routing signal traces.

In order to achieve maximum performance using the RTL8111B-GR, good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8111B-GR, good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify that critical components such as the clock source and transformer meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (10µF-22µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8111B-GR chip.
- Provide termination on all high-speed switching signals.
- Route the signal trace as short as possible.
- Use a smaller package for the capacitor to reduce the package inductance.

Use the following signal integrity techniques to reduce crosstalk.

- Shorter parallel route
- Wider ground plane spacing between GMII signal wires
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane

2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane if possible.
- 50-ohm impedance match resisters and 0.1uF common mode noise filter capacitors should be placed near the RTL8111B-GR chip.
- Avoid right angle signal traces. Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

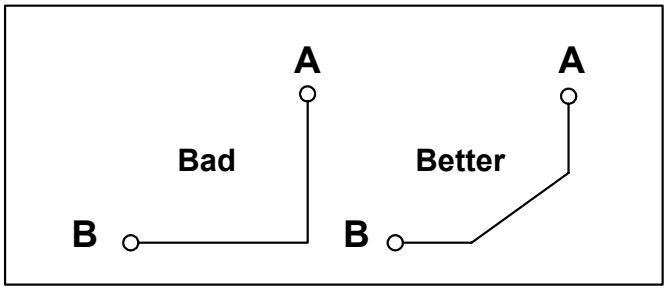

Figure 1. Signal Trace Angles

2.3. Placing the RTL8111B-GR

- The RTL8111B-GR should be placed as close as possible to the magnetics.

2.4. Magnetics

- The 10/100/1000M magnetics should be placed as close as possible to the RJ-45 connector.
- The magnetics device or devices with magnetic fields should be separated and mounted at 90 degrees to each other

2.5. Crystal

- The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx, power), magnetics, and board edges.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI.
- The retaining straps of the OSC, if any, need good grounding.

2.6. Termination Resistors & Capacitors

The RTL8111B-GR does not require any termination resistors and capacitors. Figure 2 shows the layout of the RTL8111B-GR.

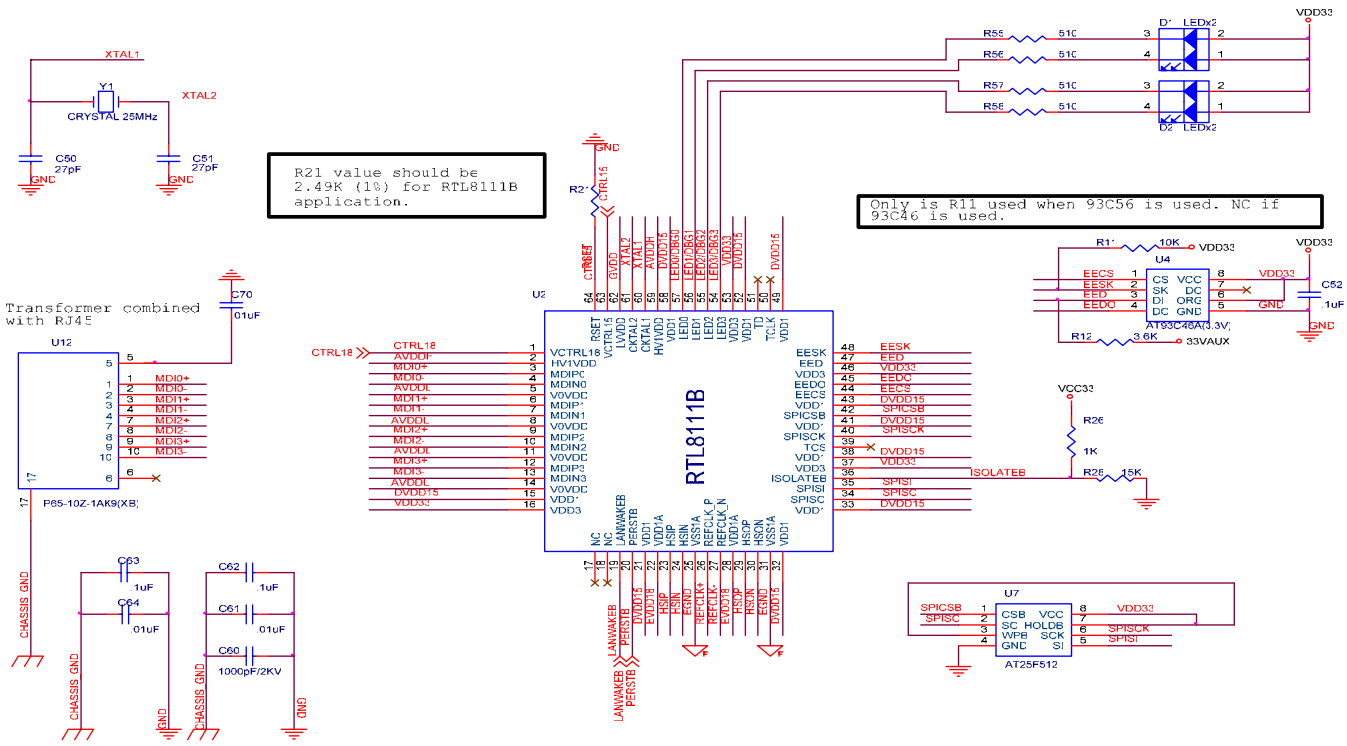

Figure 2. Layout

2.7. Ferrite Beads & De-Coupling Capacitors

- Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors (Z5U, Y5V types are recommended) should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

3. Signal & Trace Routing

Noise, ringing, and data lines have to be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, cross-talk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Traces routed from the RTL8111B-GR to the 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8111B-GR and magnetics is achievable only when there is no interference. It is also very important to keep all four differential pair signal traces (MDI0+/-, MDI1+/-, MDI2+/-, MDI3+/-) equal in length. The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong canceling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is eight mils, then D1 can be 8 mil wide (Figure 3).

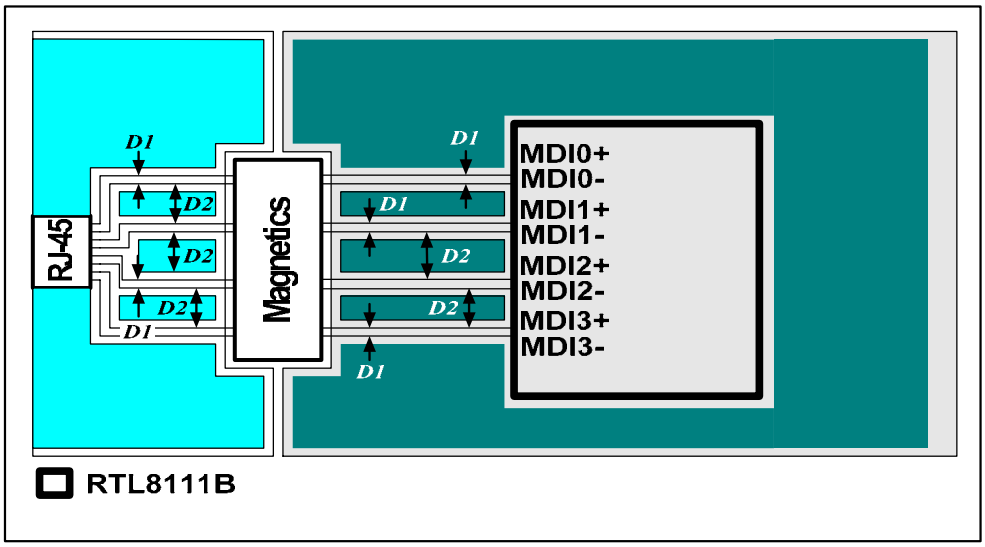

Figure 3. Signal & Trace Routing

- We suggest that there should be more than 50 mil spacing between different differential pairs to minimize cross-talk coupled from other pairs (D2 in Figure 3). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:

  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair

- To minimize impedance mismatch, we recommend not to use vias on the four differential pairs
- Avoid right angle signal traces. Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1, page 3. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them.
- It is important to separate Digital Signals (e. g., BROM, Flash, EESK) from Analog Signals (e. g., MDI0+/-, MDI1+/-, MDI2+/-, and MDI3+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles.
- The power into the RTL8111B-GR digital power pins can be improved with de-coupling capacitors. The Power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8111B-GR need to be de-coupled with a capacitor. The de-coupling capacitors should be placed as close to the IC as possible and the traces should be kept short.
- If the built-in regulators are used, the traces between each power transistor (Q1 and Q3) and the RTL8111B-GR for supplying 1.8Vand 1.5V power (i.e. Q1 to CTRL18 and AVDDL pins, and Q3 to CTRL15 and DVDD) should be kept as short and wide as possible to provide cleaner digital and analog power supplies. Keeping the bulk de-coupling capacitors (C18 and C19, C24 and C25, etc.) as close to the power outlet as possible is very important. It is strongly recommended to use tantalum capacitors for C18 and C24. Further details for the transistors Q1 and Q3 can be found in section 5.6 Power Transistors, page 11.

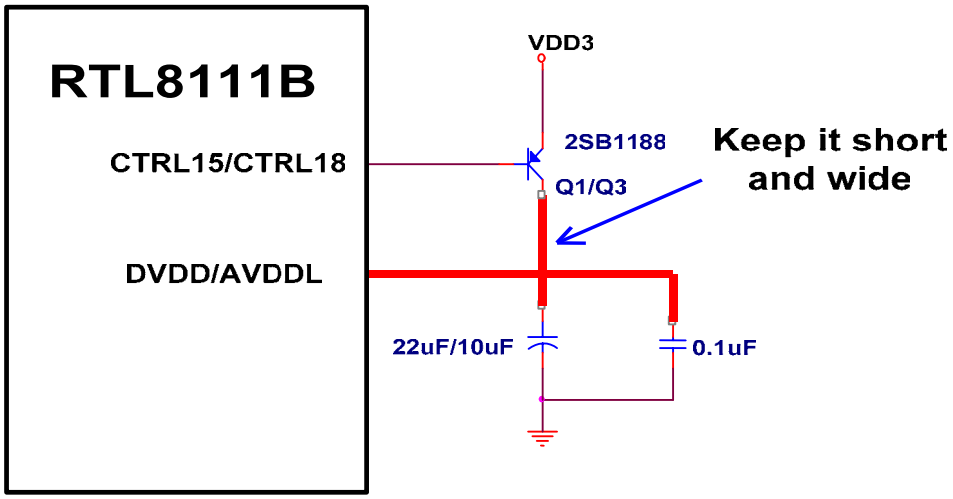

Figure 4. Power Transistor Traces

- The PCI-EXPRESS signal differential pairs should be 5mils wide, with a spacing of 7mils between them (REFCLK+ & REFCLK-, HSOP & HSON, HSIP & HSIN). The length difference of the signals in a pair should not exceed 5 mils. For example, if HSON is 900 mils and HSOP is 890mils, it may result in data transmit error.

4. Power Supply & Ground Plane

4.1. Power Plane Partition

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. It is recommended to use at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8111B-GR. If it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

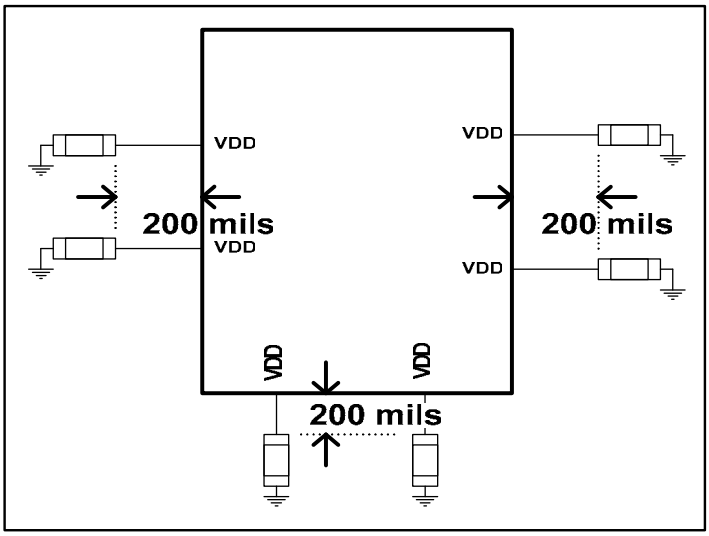

Figure 5. Decoupled Capacitor Example

(b) Use a Ferrite Bead to connect Digital & Analog Power

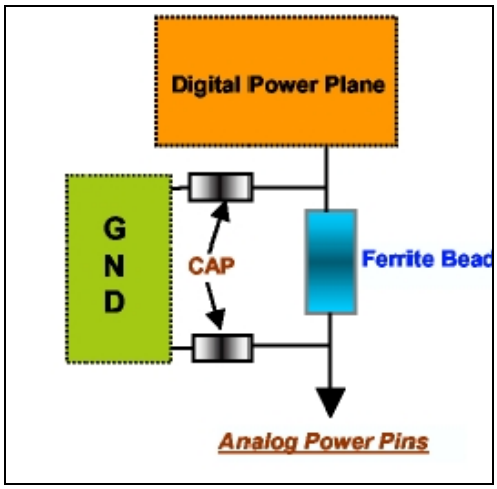

Figure 6. Ferrite Bead

To further improve the performance of the power plane, try to keep the contact area between the RTL8111B-GR VDD pins and power plane as large as possible rather than using small narrow traces (Figure 7).

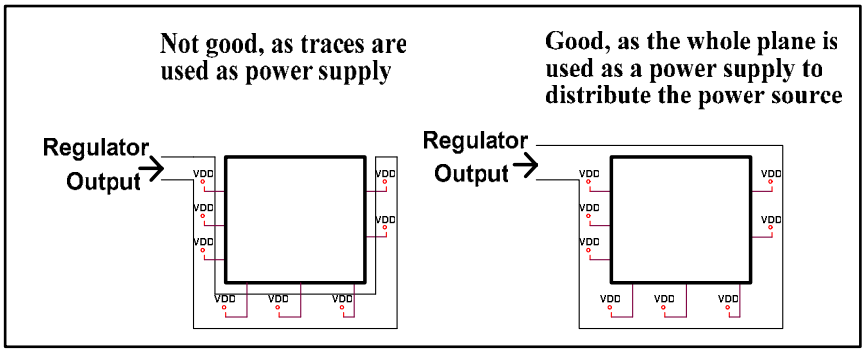

Figure 7. Power Source Distribution

4.2. Ground Plane Layout

There is only one ground plane for analog power (AVDDH & AVDDL), digital power (VDD33, DVDD15) and PCI-Express power (EVDD18). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 5.6mm x 5.6mm and the PCB layout needs to drill 9 vias to connect the EPAD to the ground plane (see Figure 8).

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

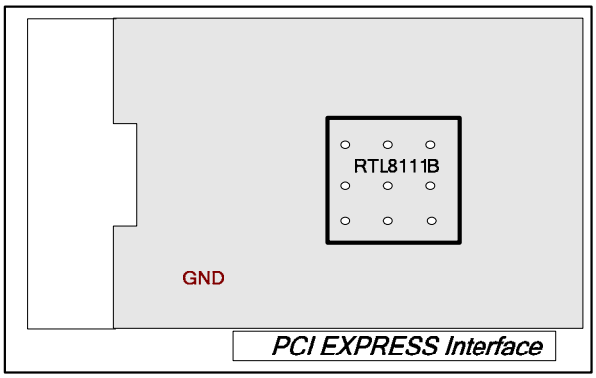

Figure 8. Ground Plane Layout-1

To achieve better GND plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 9 illustrates a not so good (left) and a good ground plane layout (right).

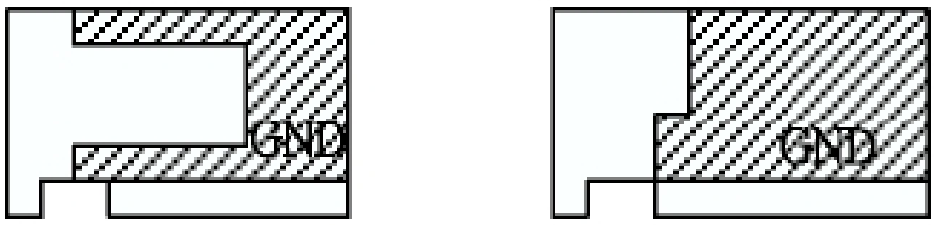

Figure 9. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer induced noise away from the power and system ground planes (Figure 10).

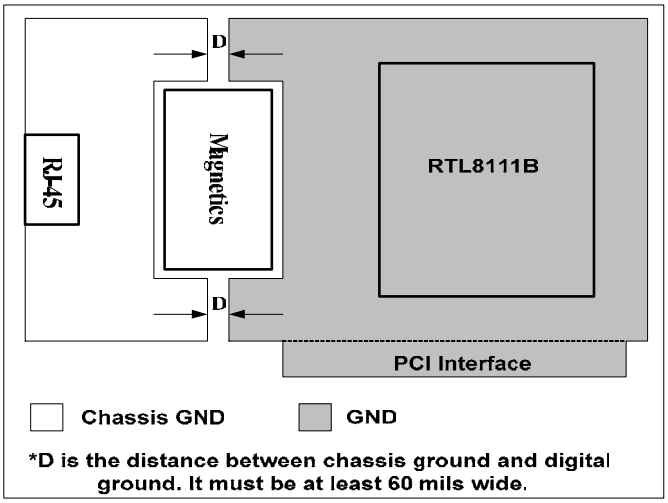

Figure 10. Ground Plane Separation

The Chassis Ground as shown in Figure 10 is known as an "Isolated Ground". It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is also important to keep the gap (D in Figure 10) between Chassis GND and System GND wider than 60 mils for better isolation.

5. Parts Recommendations

5.1. 10/100/1000M Magnetic

Turn Ratio Tx/Rx: 1:1

Primary Inductance: 350uH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18 dB Min @ 100Ω, 1 ~ 30MHz

-14 dB Min @ 100Ω, 30 ~ 60MHz

-12 dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40 dB Min @ 1 ~ 60MHz

-30 dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C.

Recommended Magnetics: Pulse H5007 or similar.

5.2. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to XTAL1 (Pin121) and XTAL2 (Pin122), and shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz
Temperature Stability	±10ppm
Duty Cycle	50% ±10%
Tolerance	±50ppm
Aging	5ppm/year, max.

5.3. Resistors

Resistors that have tolerance requirements within 1%, are strongly recommended. Refer to the provided BOM for suggested schematics.

5.4. Capacitors

- Use Electrolytic capacitors for large value and low frequency de-coupling
- Use X7R and C0G capacitors for small value and high frequency de-coupling and use Y5V capacitors for critical temperature requirements
- For power filtering, low ESR Tantalum capacitors are recommended for the power circuit and use X7R dielectric capacitors of several uF correspondingly to reduce the power ripple significantly. Refer to the provided BOM for suggested schematics.

5.5. Ferrite Bead

The ferrite bead used should be of at least 60Ω@100MHz impedance with a rated current of 1000mA or over.

5.6. Power Transistors

The RTL8111B-GR works with current rates of around 400mA and thus it is recommended to use components that have a current rate 3 times greater than this value. It is important to select a transistor that has sufficient current rate for this particular circuit. The beta (β) value should be as large as possible (i.e., $\beta > 150$)

5.7. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

6. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for Gigabit Ethernet applications.

- If it is found that there is a serious EMI issue during read/write operations from the PCI 33/66 MHz interface, some de-coupling capacitors (0.047uF, 22uF) can be added between the system GND and power planes.
- For legacy WOL applications, please note the WOL connector specification for the system. The WOL connector specification must match the WOL connector of the motherboard where the system will be used.
- When using the oscillator as the clock source for 25MHz, avoid connecting any capacitors to the clock circuitry.
- The digital bus traces for PCI, BOOTROM, and EEPROM should have lengths as equal as possible to achieve proper skew rate requirements, especially for PCI 66MHz/64-bit application.
- Routing the PCI clock trace longer than bus traces in order to gain some setup time is not recommended (though it can be done). The digital functionality of the IC is robust enough that there is no need to route the PCI clock in this manner.
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com.tw